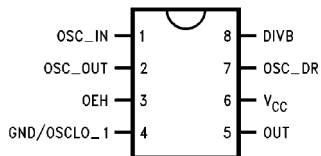
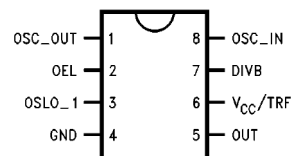


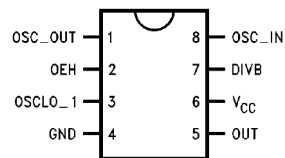
Connection Diagrams



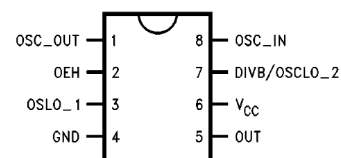
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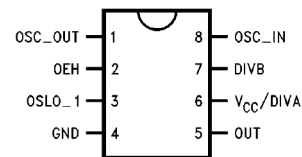
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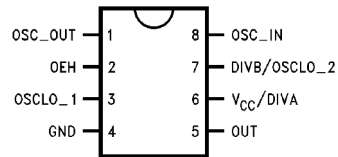
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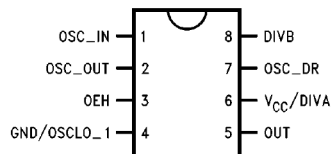
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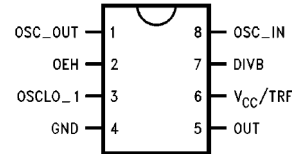
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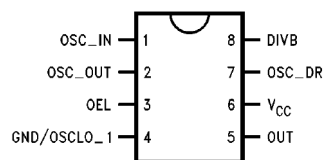
(G) 3317



(D) 3314



(H) 3318



(I) 3319

Truth Tables

Division Selection

DIVB	DIVA	OEL	OEH	Divider Output
F	0/F	X	X	Divide-by 1
1	0/F	0	1	Divide-by 2
0	0/F	0	1	Divide-by 4
F	1	0	1	Divide-by 8
1	1	0	1	Divide-by 16
0	1	0	1	Divide-by 32
X	X	1	X	Output Reset HIGH at Re-enable
X	X	X	0	Output Reset HIGH at Re-enable

Note: Actual value of the floating OSC_DR and DIVB input is $V_{CC/2}$

Rise and Fall Time Selection

OSC_DR	DIV	TRF	Rise/Fall Time (ns)
F	N	0/F	2
F	N	1	less than 2
F	Y	0/F	4
F	Y	1	2
0,1	X	0/F	4
0,1	X	1	2

Drive Selection

OSC_DR	Drive
0	Low
1	Medium
F	High

Note: Where "F" indicates floating the input.

Pin Descriptions

Note: Pin out varies for each device.

OSC_IN	Input to Oscillator Inverter. The output of the crystal would be connected here.	OEL	Active LOW 3-STATE enable pin. This pin pulls to a low value when left floating and 3-STATE the output when forced HIGH. This pin has TTL compatible input levels.
OSC_OUT	Resistive Buffered Output of the Oscillator Inverter	TRF	Rise and Fall time override pin. Available only for die form.
OSC_DR	3 Level input pin that selects Oscillator Drive Level	OUT	This pin is the main clock output on the device.
DIVA	Input used to select Binary Divide-by Option. This pin has CMOS compatible input levels.	OSCLO_1	The Oscillator LOW pin is the ground for the Oscillator.
OEH	Active HIGH 3-STATE enable pin. This pin pulls to a high value when left floating and 3-STATES the output when forced low. This pin has TTL compatible input levels.	OSCLO_2	This pin is the same signal as OSCLO_1. It has been provided as an alternate connection for OSCLO_1 for hybrid assemblies.
		V_{CC}	The power pin for the chip.
		GND	The ground pin for all sections of the circuitry except the oscillator and oscillator related circuitry.

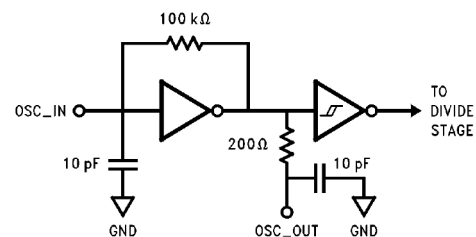
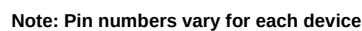
Functional Table

Summary of Device Options

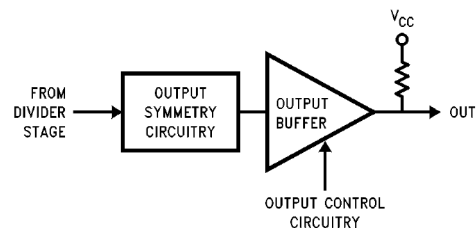
Device	Divide	Enable	Drive	Output Rise/Fall Time (ns)
3311	1, 2, 4	OEH	L, M, H	2, 4
3312	1, 2, 4	OEH	H	2, 4
3313	8, 16, 32	OEH	H	4
3314	8, 16, 32	OEH	L, M, H	4
3315	1, 2, 4	OEL	H	1, 2
3316	4	OEH	H	4
3317	32	OEH	H	4
3318	1, 2, 4	OEH	H	1, 2
3319	1, 2, 4	OEL	L, M, H	2, 4

Each drive has one output with the choices of selecting frequency divide, output enable, crystal drive and output rise and fall time. Crystal drive options are:

L = LOW Drive
M = MEDIUM Drive
H = HIGH Drive



The diagram shows a circuit labeled "INPSL". An "INPUT" terminal is connected to a pullup resistor (represented by a zigzag line) which is connected to "GND". The input terminal is also connected to the input of a buffer (represented by a triangle with a diagonal line). The output of the buffer is labeled "NEXT STAGE".



Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	-0.5V to 7.0V
DC Input Voltage Diode Current (I_{IK})	±9 mA
DC Input Voltage (V_I)	-0.5V to 7.0V
DC Output Diode Current (I_{OK})	±20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±70 mA
Storage Temperature (T_{STG})	-55°C to 150°C
Junction Temperature (T_J)	
SOIC	140°C/W

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC} V
Operating Temperature (T_A)	-40° to +85°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = −40° C to +85°C		Units	Conditions
			Typ	Guaranteed Limits		Min	Max		
				Min	Max				
V _{IHTTL}	Minimum HIGH Level Input Voltage, TTL Level Inputs (OE _H , OEL)	4.5		2.0		2.0		V	
		5.5		2.0		2.0			
V _{ILTTL}	Maximum LOW Level Input Voltage, TTL Level Inputs (OE _H , OEL)	4.5			0.8		0.8	V	
		5.5			0.8		0.8		
V _{IHCMOS}	Minimum HIGH Level Input Voltage. CMOS Level Inputs (DIVA)	4.5		3.15		3.15		V	
		5.5		3.85		3.85			
V _{ILCMOS}	Maximum LOW Level Input voltage. CMOS Level Inputs (DIVA)	4.5		1.35		1.35		V	
		5.5		1.65		1.65			
V _{IN3L_H}	Minimum Logic 1 Input for Three Level Input (DIVB, OSC_DR)	4.5		4.05		4.05		V	
		5.5		4.95		4.95			
V _{IN3L_1/2}	Minimum Logic 1/2 Input for Three Level Input (DIVB, OSC_DR)	4.5		1.8	2.7	1.8	2.7	V	
		5.5		2.2	3.3	2.2	3.3		
V _{IN3L_L}	Maximum Logic 0 Input Level Three Level Input (DIVB, OSC_DR)	4.5			0.45		0.45	V	
		5.5			0.45		0.45		
V _{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.40		4.40		V	I _{OUT} = −50μA
		5.5	5.49	5.40		5.40			
		4.5		3.86		3.76			
5.5		4.86		4.76			I _{OH} = −48 mA V _{IN} = V _{IH} or V _{IH}		
V _{OL}	Minimum LOW Level Output Voltage	4.5	0.001		0.1		0.1	V	I _{OUT} = 50μA
		5.5	0.001		0.1		0.1		
		4.5			0.44		0.44		
		5.5			0.44		0.44		
I _{IHRES}	Input Current for Pins DIVB, OSC_DR, and DIVA (Input is Logic HIGH)	5.5		220	360	200	380	μA	V _{IN} = 5.5V
I _{ILRES}	Input Current for Pins DIVB, OSC_DR, and DIVA (Input is Logic LOW)	5.5		−220	−360	−200	−380	μA	V _{IN} = 0.0V
I _{IHENAB}	Input Current for Enable Pin OEL	5.5		90	160	85	175	μA	V _{IN} = 5.5V
I _{ILENAB}	Input Current for Enable Pin OE _H	5.5		−90	−160	−85	−175	μA	V _{IN} = 0.0V
I _{IHOSC}	Input Current for OSC_IN Pin (Indicates Bias Resistance)	5.5		20	100	20	125	μA	V _{IN} = 5.5V
I _{ILOSC}	Input Current for OSC_IN Pin (Indicates Bias Resistance)	5.5		−20	−100	−20	−125	μA	V _{IN} = 0.0V
I _{OZH}	Output Disabled Current (Output HIGH)	4.5			3.0		5.0	μA	V _{OUT} = V _{CC}
		5.5			3.0		5.0		

DC Electrical Characteristics (Continued)

Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = −40° C to +85°C		Units	Conditions
			Typ	Guaranteed Limits					
				Min	Max	Min	Max		
I _{OZL}	Output Disabled Current (Output LOW)	4.5 5.5			−140 −170		−150 −180	μA	V _{OUT} = 0.0V
I _{OLD}	Minimum Dynamic Output Current	5.5	75		75			mA	V _{OLD} = 1.65v
I _{OHD}	Minimum Dynamic Output Current	5.5	−75		−75			mA	V _{OHD} = 3.85V
I _{CCOSC_L}	Additional I _{CC} with OSC_IN Floating. LOW Drive Mode	4.5 5.5	0.6		0.6		6.5	mA	OSC_IN = Float
I _{CCOSC_M}	Additional I _{CC} with OSC_IN Floating. LOW Drive Mode	4.5 5.5	1.7		1.7		12.4	mA	OSC_IN = Float
I _{CCOSC_H}	Additional I _{CC} with OSC_IN Floating. LOW Drive Mode	4.5 5.5	5.5		5.5		31.5	mA	OSC_IN = Float
I _{CC1}	Additional Maximum I _{CC} per Input (OE _H , OE _L Pins)	5.5		1.5		1.5		mA	V _{IN} = V _{CC} − 2.1V
I _{CC3L}	Additional Maximum I _{CC} per Input (DIVB, OSC_DR Inputs)	5.5		1.5		1.5		mA	DIVB, OSC_DR Inputs Equal to V _{CC/2}

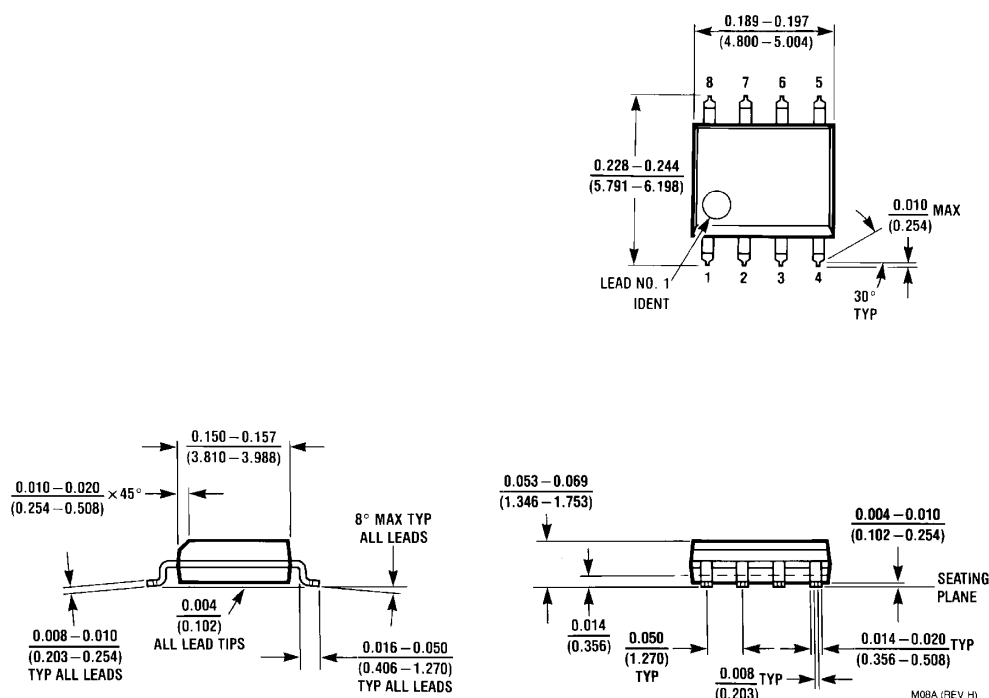
AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	V _{CC} (V) (Note 2)	T _A = -40°C to +85°C C _L = 50 pF			Units
			Min	Type	Max	
f _{MAX}	Frequency Maximum	5.0	100			ns
t _{PZH}	Output HIGH Enable Time	5.0	1.0		31.5	ns
t _{PZL}	Output LOW Enable Time	5.0	1.0		28.0	ns
t _{PHZ}	Output HIGH Disable Time	5.0	1.0		21.5	ns
t _{PLZ}	Output LOW Disable Time	5.0	1.0		16.0	ns
t _{RISE}	Rise/Fall Time	5.0		4.0		ns
t _{FALL}	30 pF (20% to 80%)					

Note 2: Voltage Range 5.0 is 5.0V ± 0.5V

Physical Dimensions inches (millimeters) unless otherwise noted



8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
Package Number M08A

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