Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	T_C=25 °C	27	W
		T_A=25 °C, R_{thJA}=50 K/W[2)]	2.5	
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}	bottom	-	-	4.6	K/W
		top	-	-	20	
Device on PCB	R_{thJA}	6 cm^2 cooling area[2)]	-	-	50	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	34	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250 µA	1.2	-	2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=34 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=34 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=16 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=15 A	-	9.4	11.8	mΩ
		V_{GS}=10 V, I_D=20 A	-	7.7	9.2	
Gate resistance	R_G		1.5	3	6.0	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=30 A	25	50	-	S

[2)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

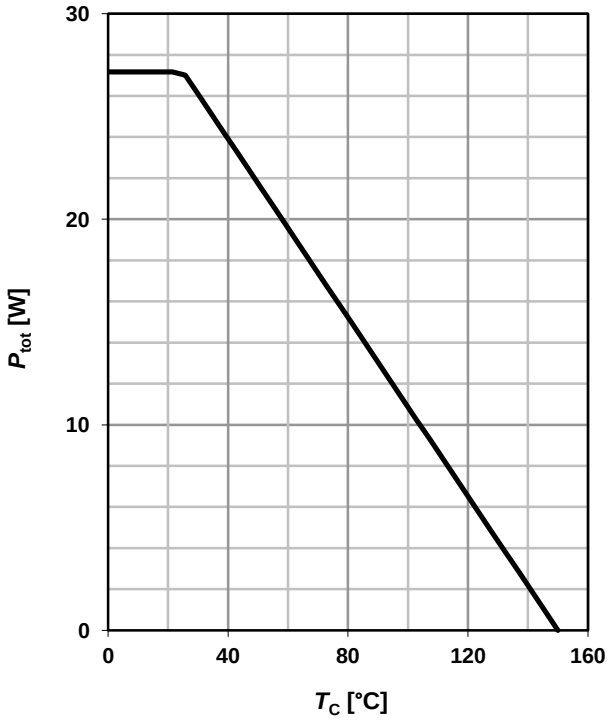
[3)] See figure 3 for more detailed information

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz	-	1100	1500	pF
Output capacitance	C_{oss}		-	390	520	
Reverse transfer capacitance	C_{rss}		-	25	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=15 V, V_{GS}=4.5 V, I_D=30 A, $R_{G,ext}$=1.6 Ω	-	9.6	-	ns
Rise time	t_r		-	4.4	-	
Turn-off delay time	$t_{d(off)}$		-	8.9	-	
Fall time	t_f		-	5.4	-	
Gate Charge Characteristics[5)]						
Gate to source charge	Q_{gs}	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V	-	3.8	5.1	nC
Gate charge at threshold	$Q_{g(th)}$		-	1.7	-	
Gate to drain charge	Q_{gd}		-	1.8	2.3	
Switching charge	Q_{sw}		-	3.8	-	
Gate charge total	Q_g		-	7.2	9.6	
Gate plateau voltage	$V_{plateau}$		-	3.3	-	V
Gate charge total	Q_g	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 10 V	-	15	20	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V	-	6.2	-	
Output charge	Q_{oss}	V_{DD}=15 V, V_{GS}=0 V	-	10	13	
Reverse Diode						
Diode continuous forward current	I_S	T_C=25 °C	-	-	25	A
Diode pulse current	$I_{S,pulse}$		-	-	176	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=30 A, T_j=25 °C	-	0.92	-	V
Reverse recovery charge	Q_{rr}	V_R=15 V, I_F=I_S, di_F/dt=400 A/µs	-	-	10	nC

[4)] See figure 13 for more detailed information
[5)] See figure 16 for gate charge parameter definition

1 Power dissipation

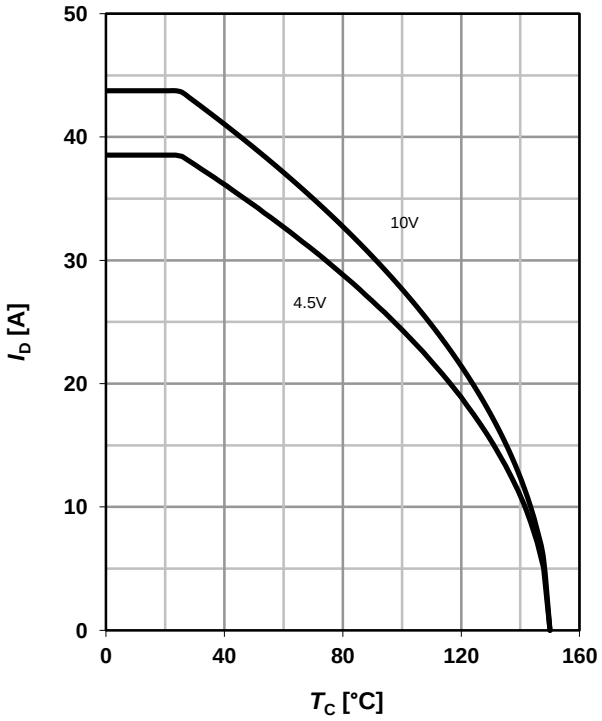
$P_{tot}=f(T_C)$



2 Drain current

$I_D=f(T_C)$

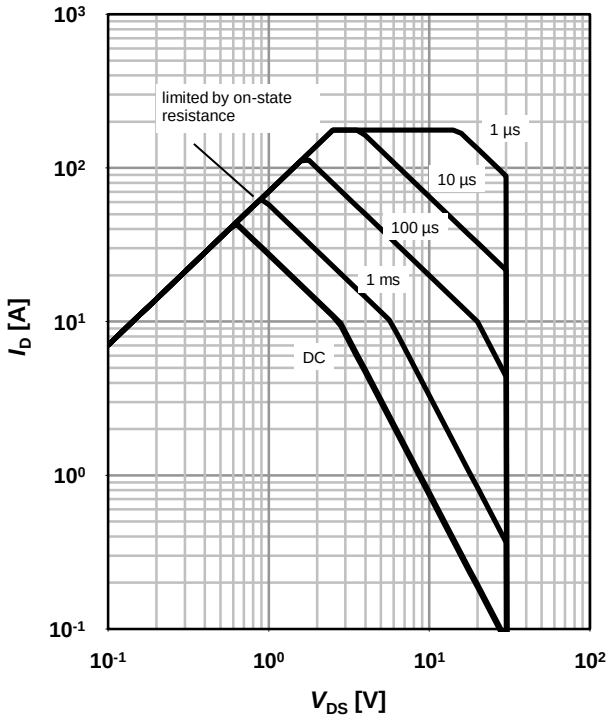
parameter: V_{GS}



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

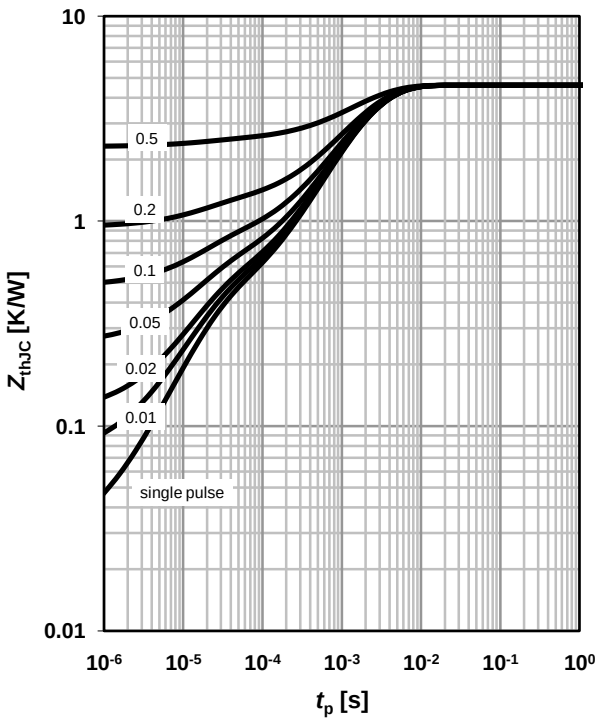
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

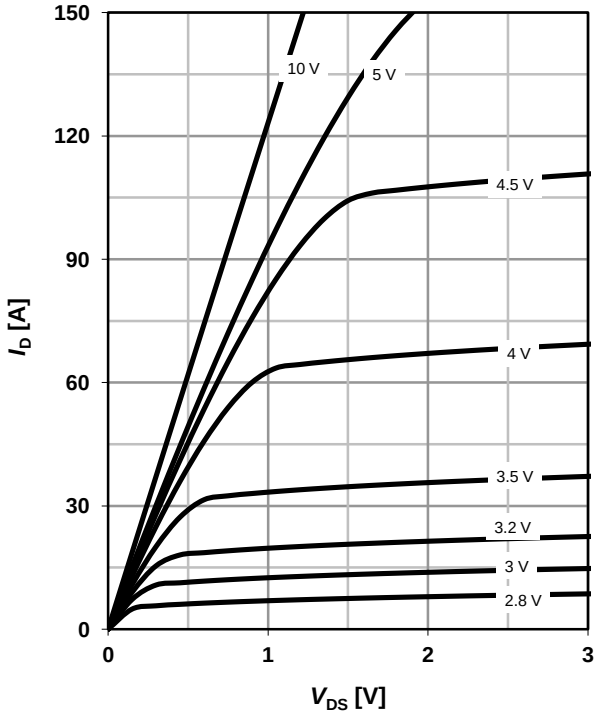
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=25$ °C

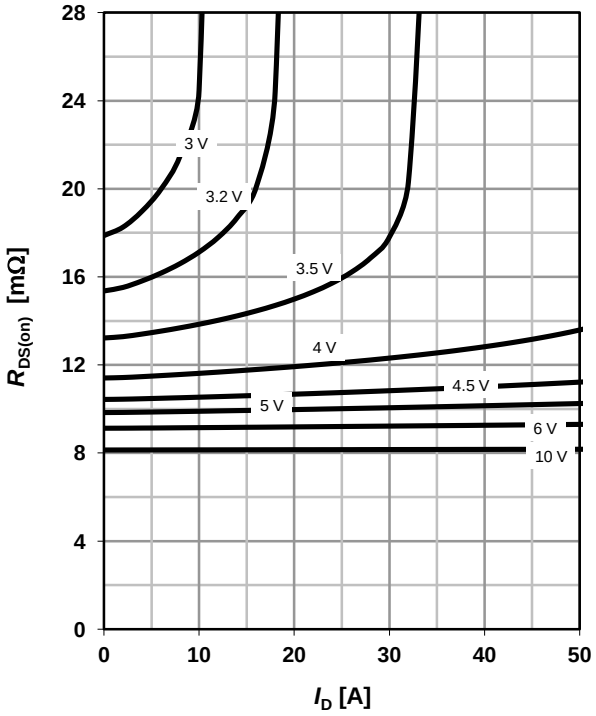
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}=f(I_D)$; $T_j=25$ °C

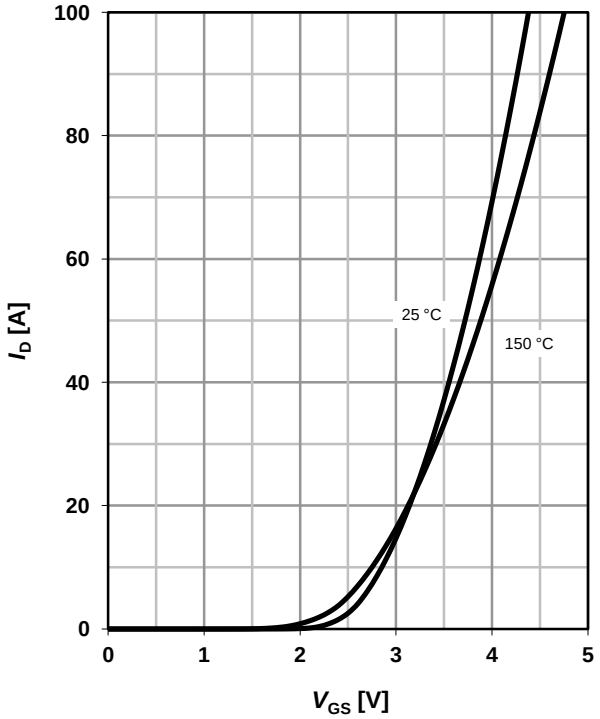
parameter: V_{GS}



7 Typ. transfer characteristics

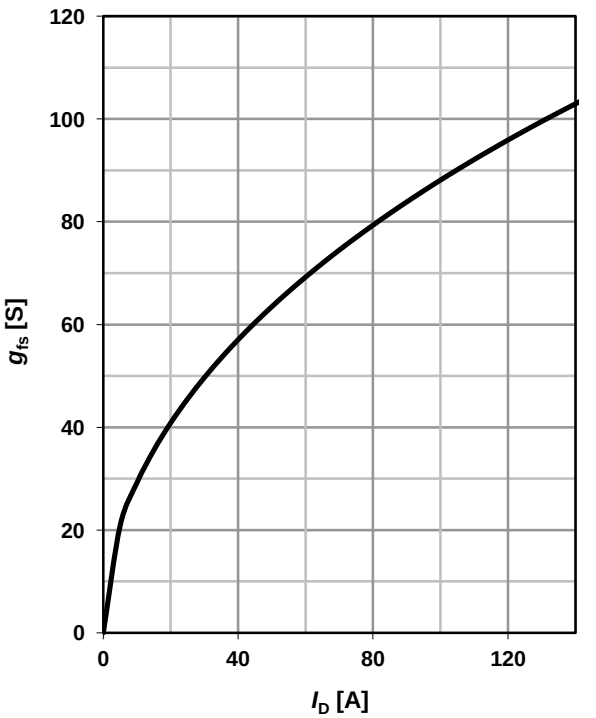
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



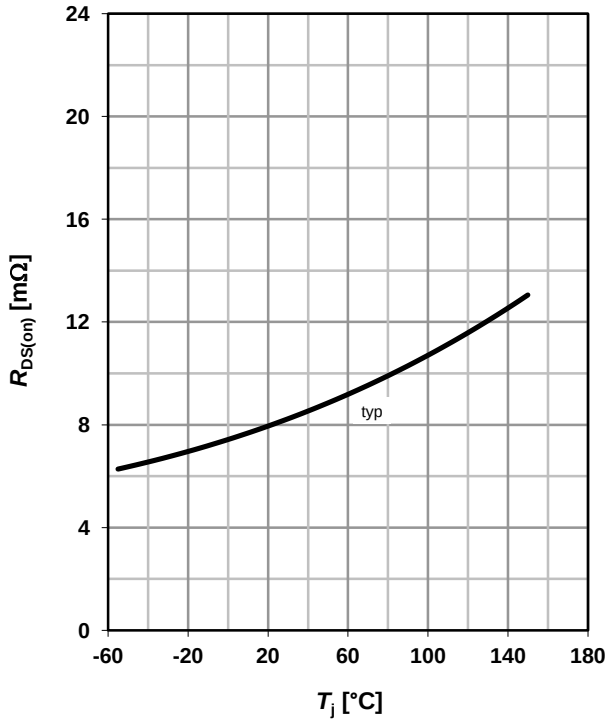
8 Typ. forward transconductance

$g_{fs}=f(I_D)$; $T_j=25$ °C



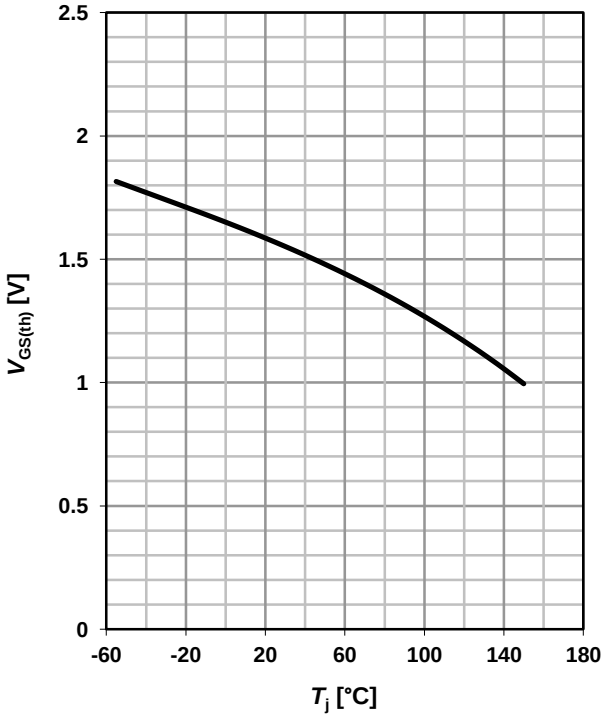
9 Drain-source on-state resistance

$R_{DS(on)}=f(T_j)$; $I_D=30$ A; $V_{GS}=10$ V



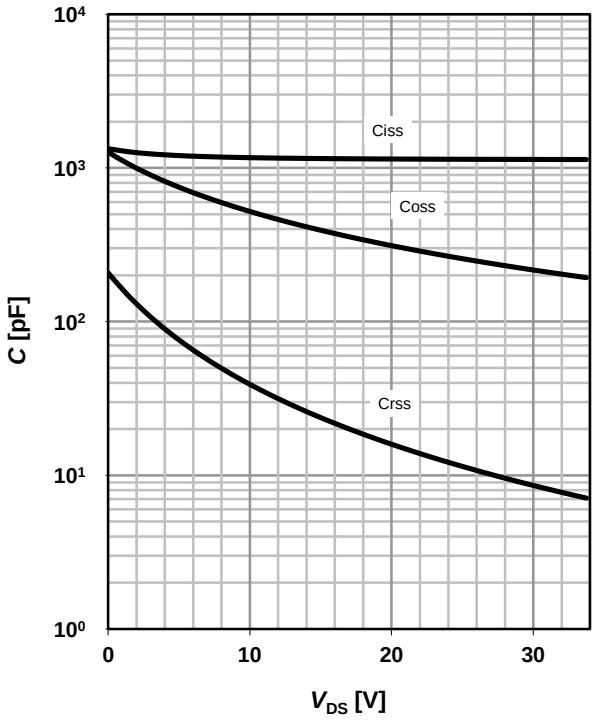
10 Typ. gate threshold voltage

$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; $I_D=250$ µA



11 Typ. capacitances

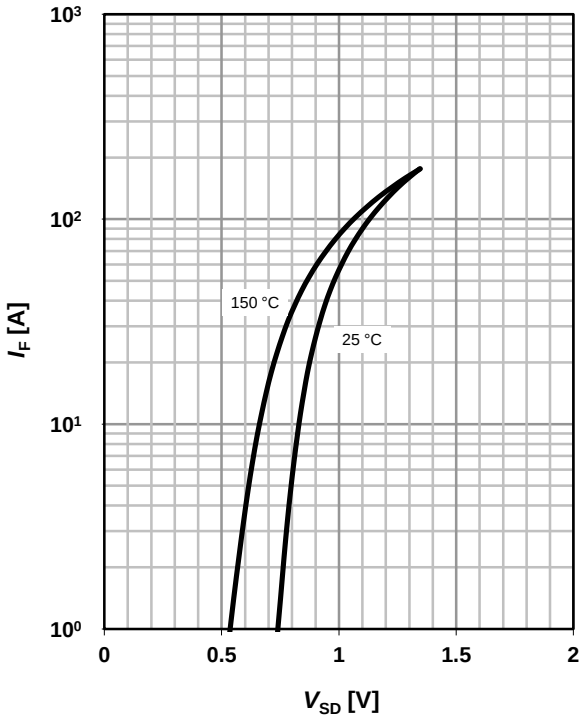
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

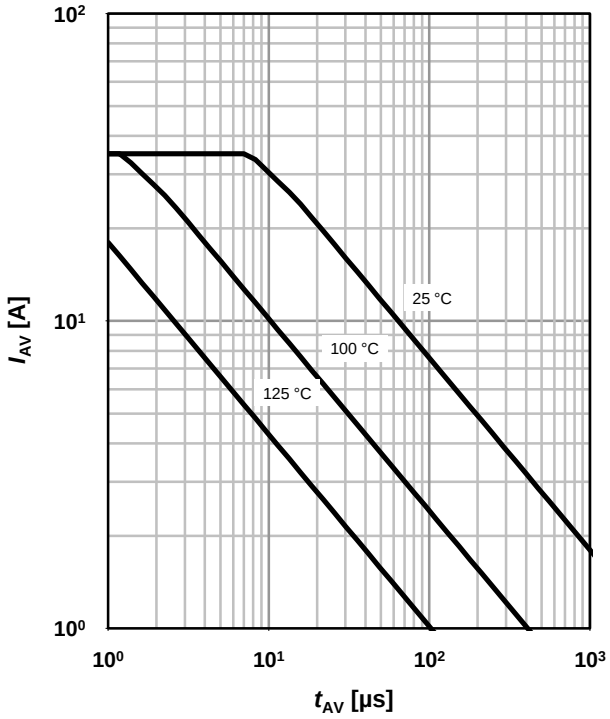
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

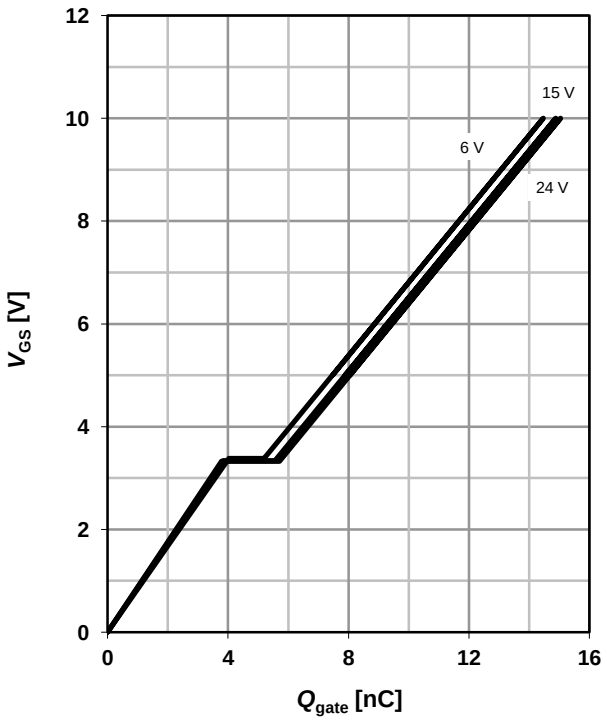
parameter: $T_{j(start)}$



14 Typ. gate charge

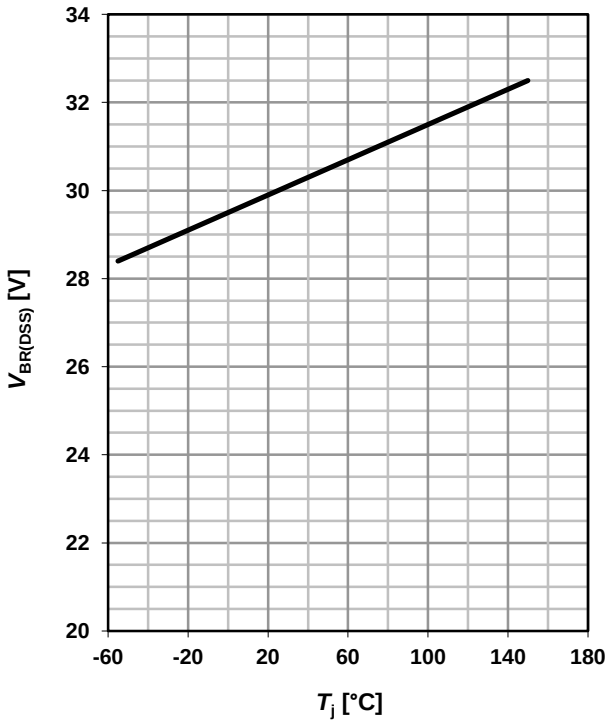
V_{GS}=f(Q_{gate}); I_D=30 A pulsed

parameter: V_{DD}

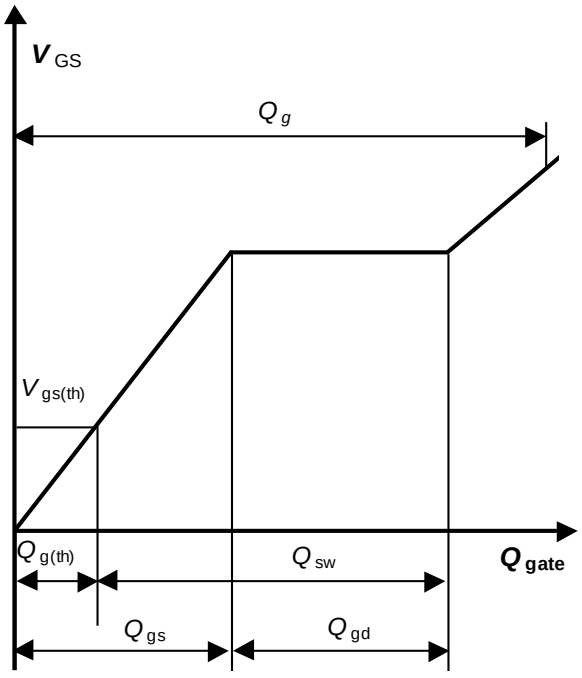


15 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=1 mA

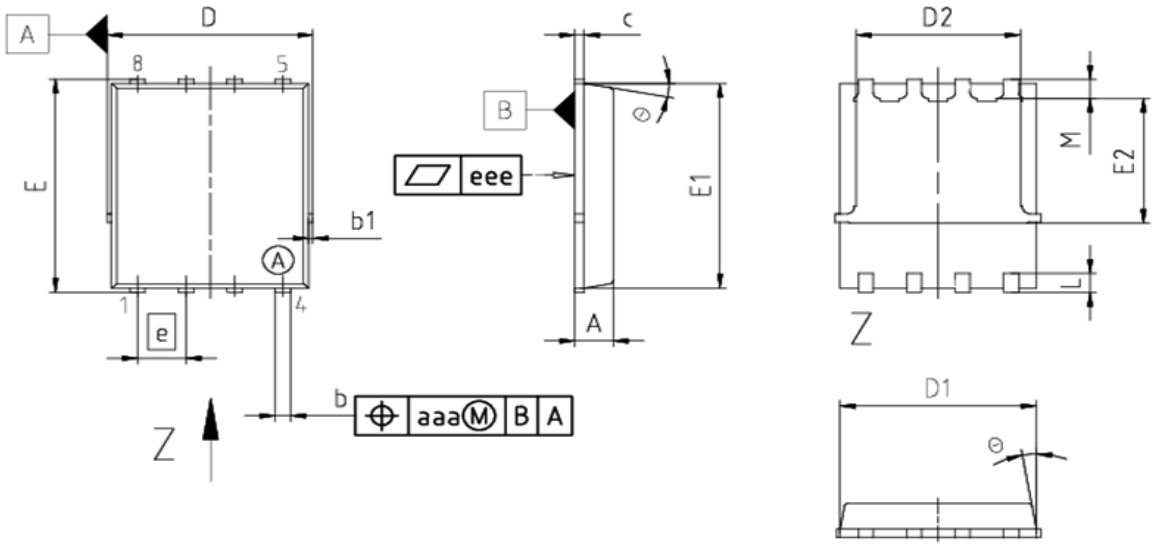


16 Gate charge waveforms



Package Outline **PG-TDSON-8**

PG-TDSON-8-5: Outline



DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
b	0.31	0.54
b1	0.02	0.22
c	0.15	0.35
D	5.15	5.49
D1	4.95	5.35
D2	3.70	4.40
E	5.95	6.35
E1	5.70	6.10
E2	3.40	3.80
e	1.27	
N	8	
L	0.45	0.71
M	0.45	0.75
Θ	8.5°	12°
aaa	0.25	
eee	0.08	

DOCUMENT NO.
Z8B00003332

SCALE
0 2 4mm

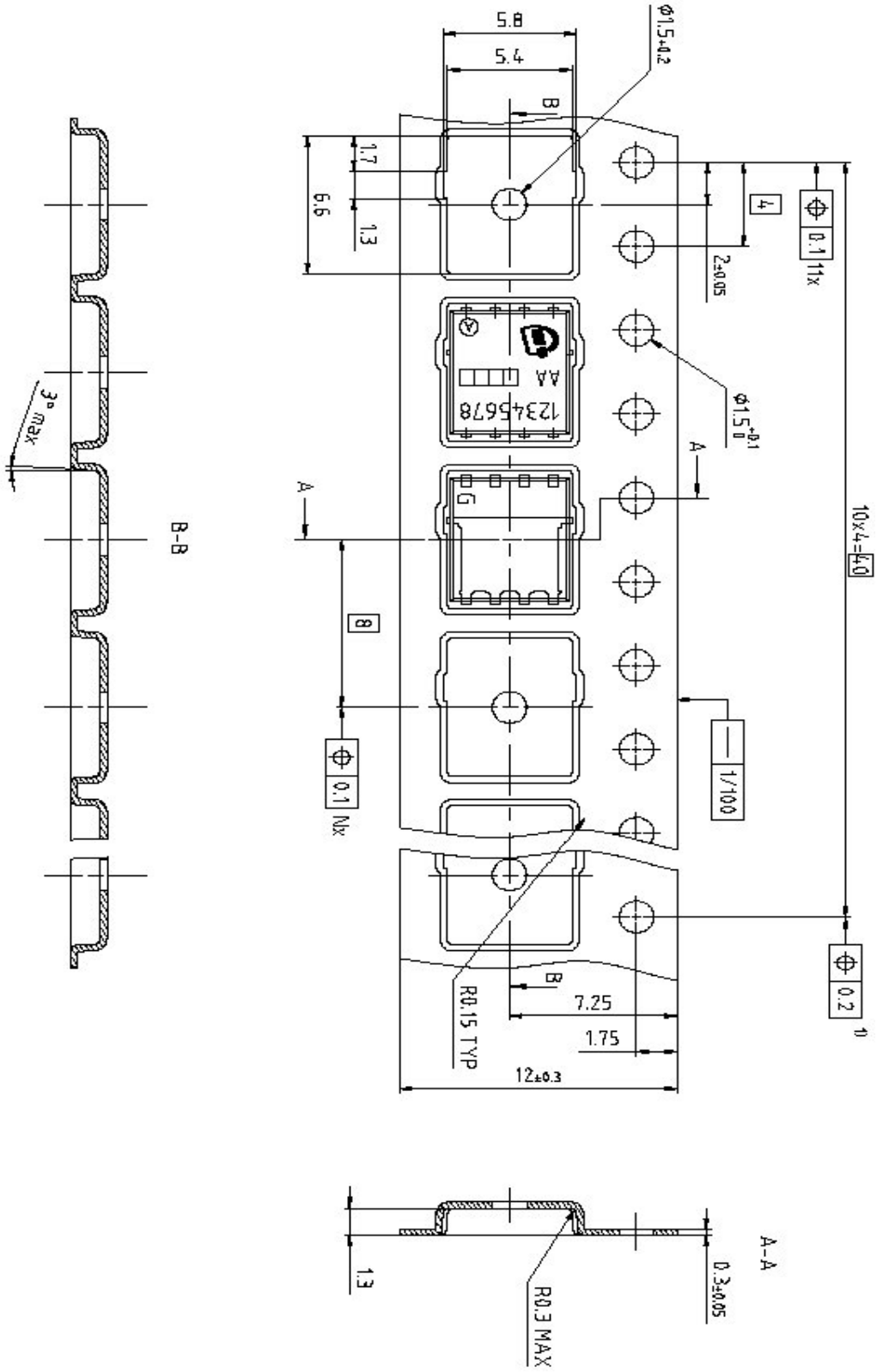
EUROPEAN PROJECTION

ISSUE DATE
10-04-2013

REVISION
04

Package Outline

PG-TDSON-8: Tape



Dimensions in mm

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