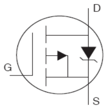
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-55	—	—	V	V_{GS} = 0V, I_D = -250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.05	—	V/°C	Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.02	Ω	V_{GS} = -10V, I_D = -38A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
gfs	Forward Trans conductance	21	—	—	S	V_{DS} = -25V, I_D = -38A
I_{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	V_{DS} = -55V, V_{GS} = 0V
		—	—	-250		V_{DS} = -44V,V_{GS} = 0V,T_J =150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V_{GS} = -20V
	Gate-to-Source Reverse Leakage	—	—	100		V_{GS} = 20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Q_g	Total Gate Charge	—	—	180	nC	I_D = -38A
Q_{gs}	Gate-to-Source Charge	—	—	32		V_{DS} = -44V
Q_{gd}	Gate-to-Drain Charge	—	—	86		V_{GS} = -10V,See Fig 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	V_{DD} = -28V
t_r	Rise Time	—	99	—		I_D = -38A
$t_{d(off)}$	Turn-Off Delay Time	—	61	—		R_G= 2.5Ω,
t_f	Fall Time	—	96	—		R_D= 0.72Ω, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	3400	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	1400	—		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	—	640	—		*ƒ* = 1.0MHz, See Fig. 5

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-74	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-260		
V_{SD}	Diode Forward Voltage	—	—	-1.6	V	T_J = 25°C,I_S = -38A,V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	89	130	ns	T_J = 25°C ,I_F = -38A
Q_{rr}	Reverse Recovery Charge	—	230	350	nC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig.11)

② Starting T_J = 25°C, L = 1.3mH, R_G = 25Ω, I_{AS} = -38A. (See Figure 12)

③ $I_{SD} \leq$ -38A, di/dt ≤ -270A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

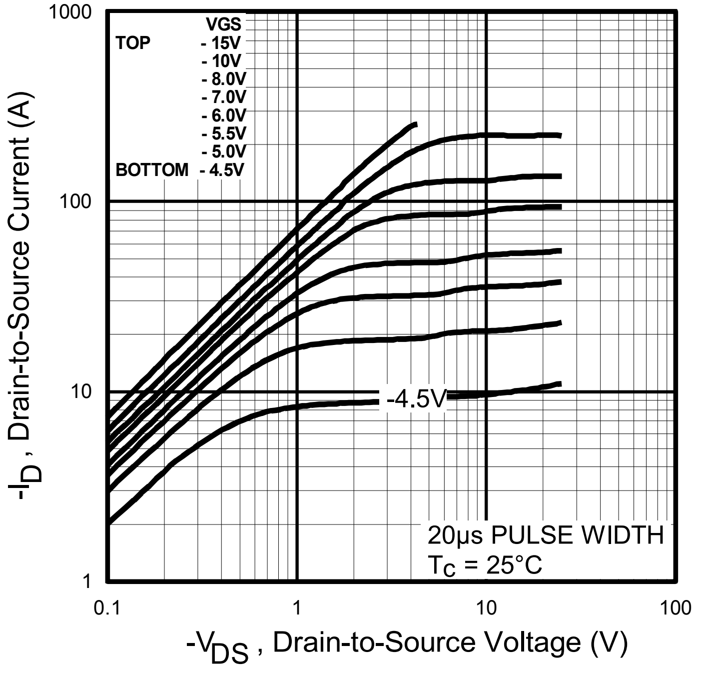


Fig. 1 Typical Output Characteristics

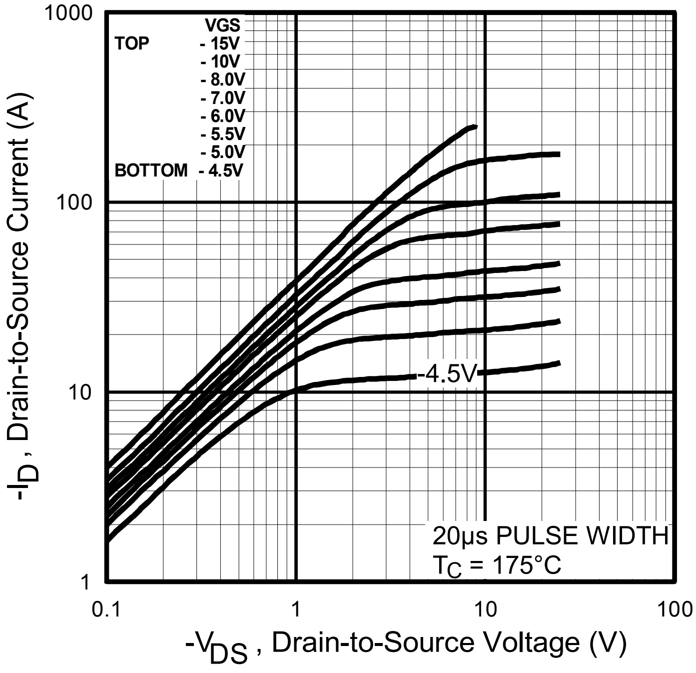


Fig. 2 Typical Output Characteristics

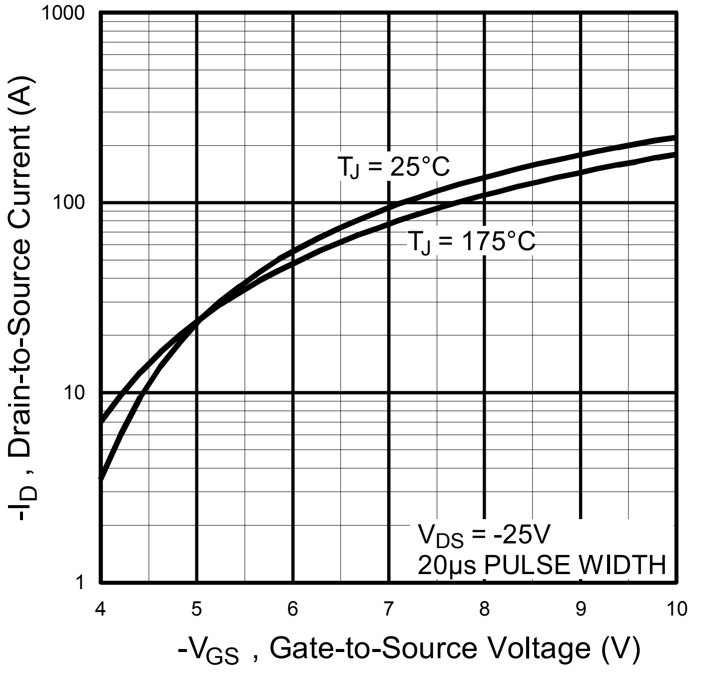


Fig. 3 Typical Transfer Characteristics

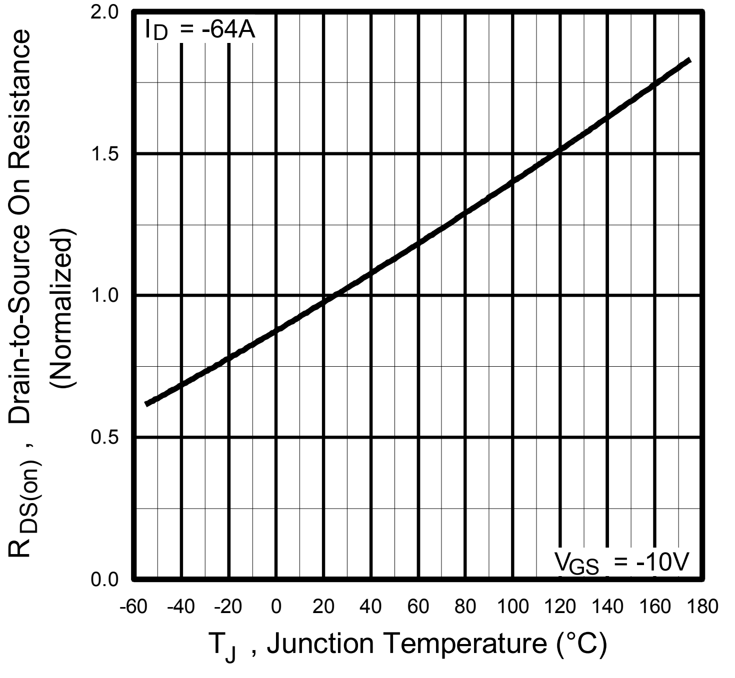


Fig. 4 Normalized On-Resistance
Vs. Temperature

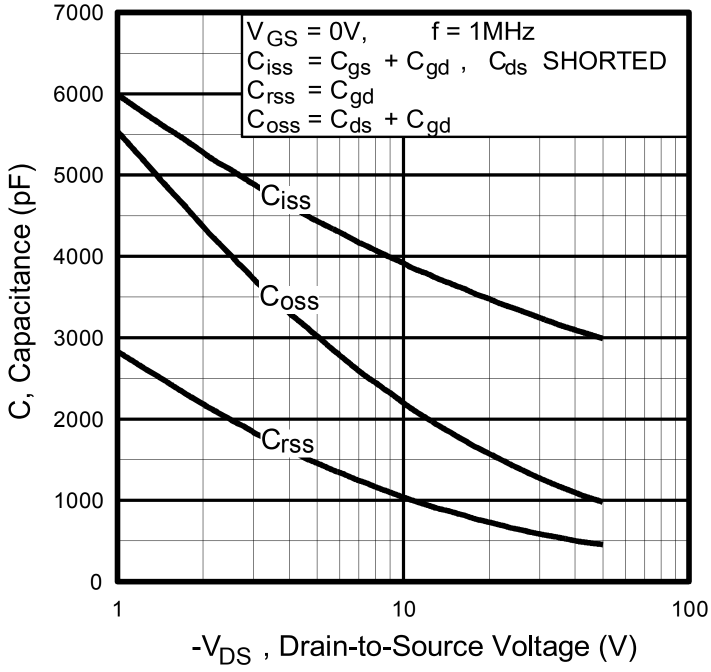


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

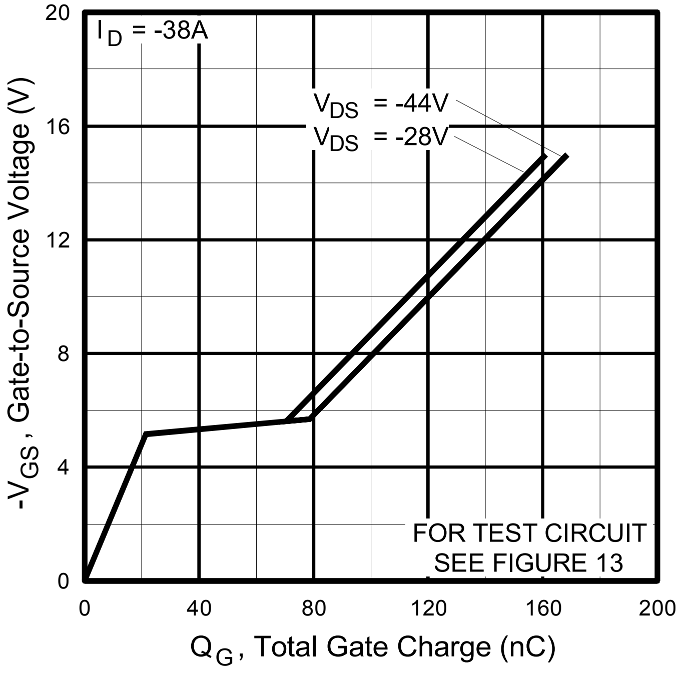


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

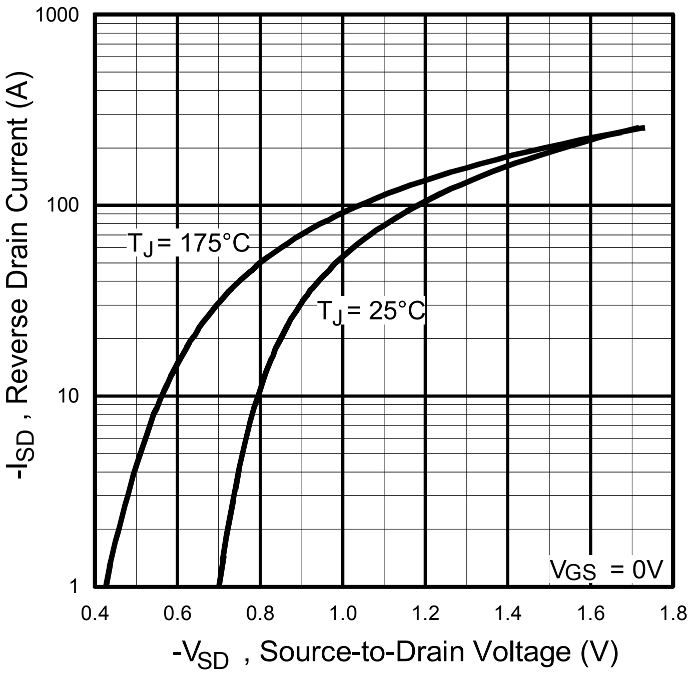


Fig. 7 Typical Source-to-Drain Diode
Forward Voltage

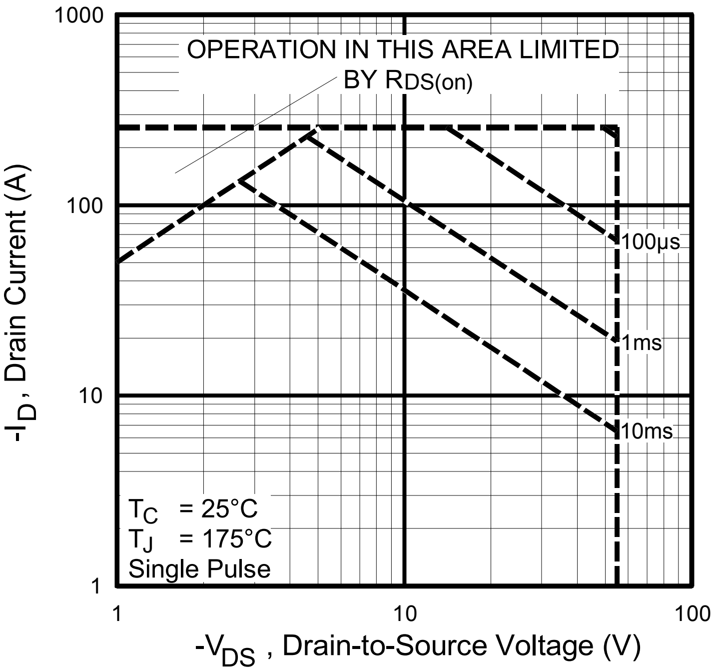


Fig 8. Maximum Safe Operating Area

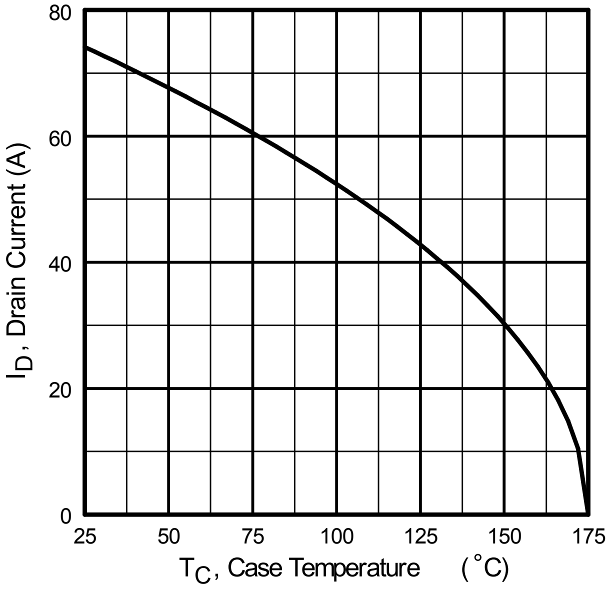


Fig 9. Maximum Drain Current vs.

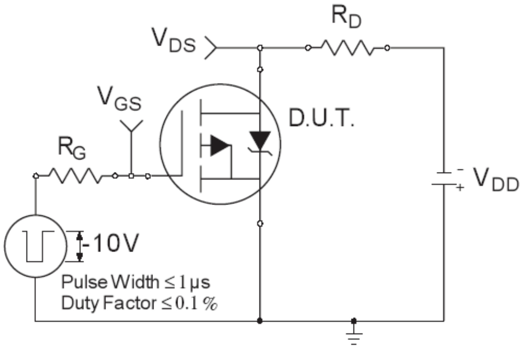


Fig 10a. Switching Time Test Circuit

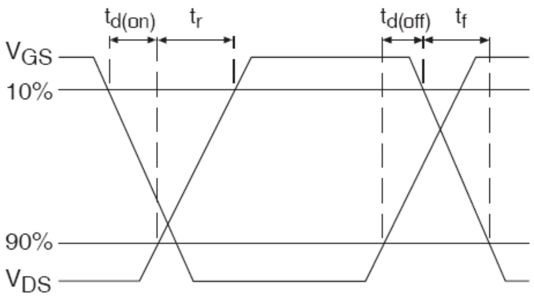


Fig 10b. Switching Time Waveforms

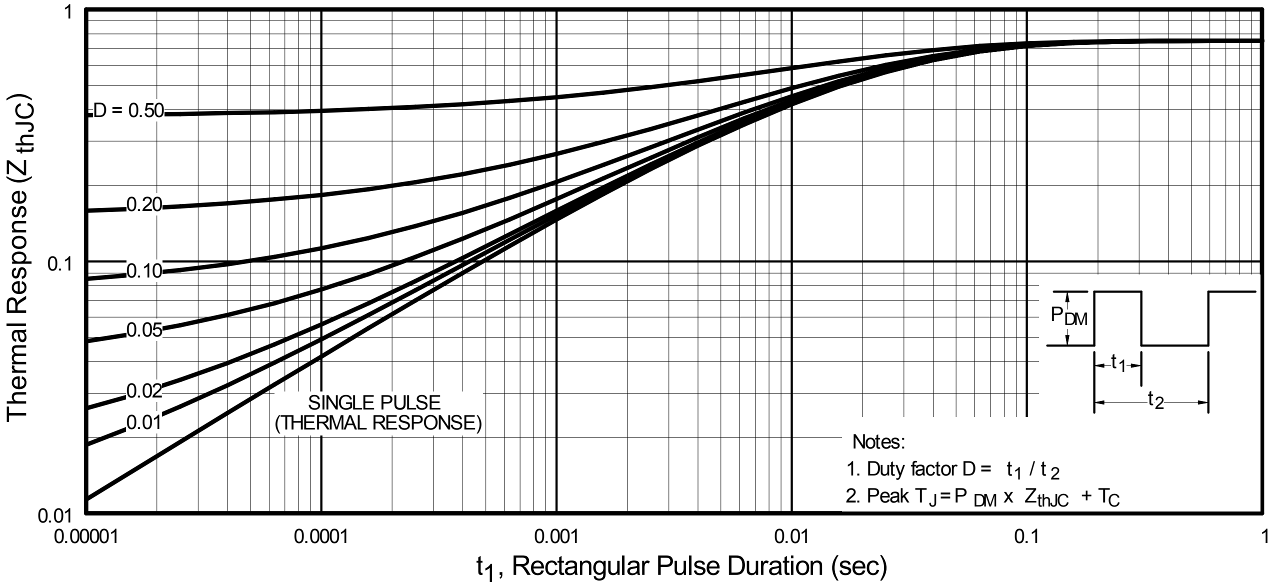


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

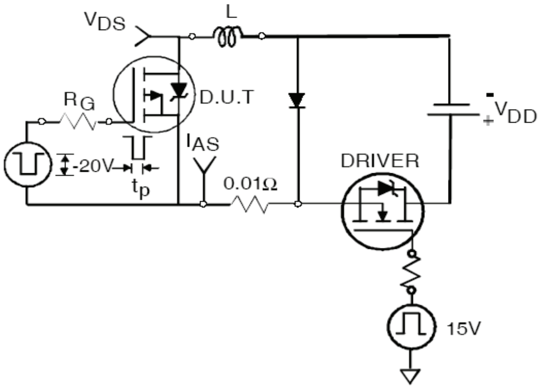


Fig 12a. Unclamped Inductive Test Circuit

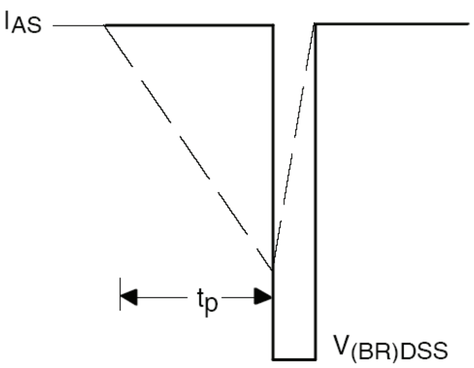


Fig 12b. Unclamped Inductive Waveforms

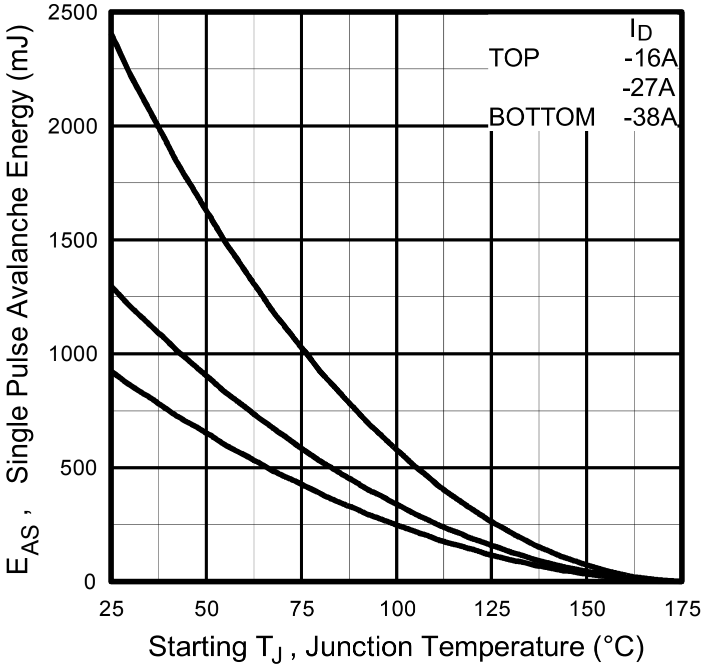


Fig 12c. Maximum Avalanche Energy vs. Drain Current

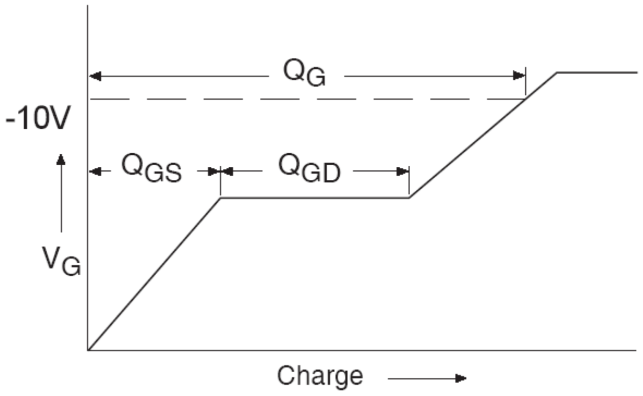


Fig 13a. Gate Charge Waveform

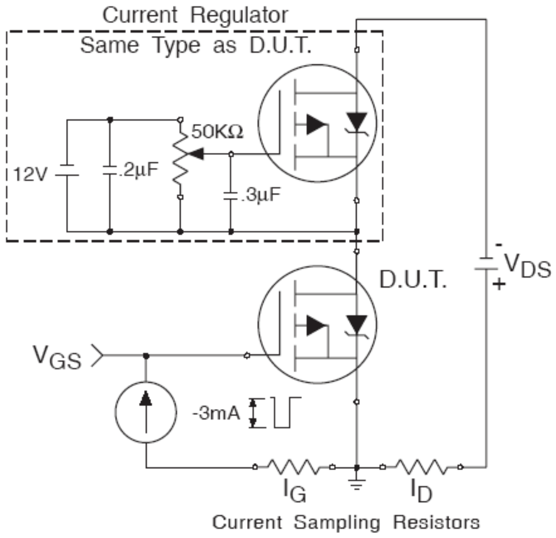
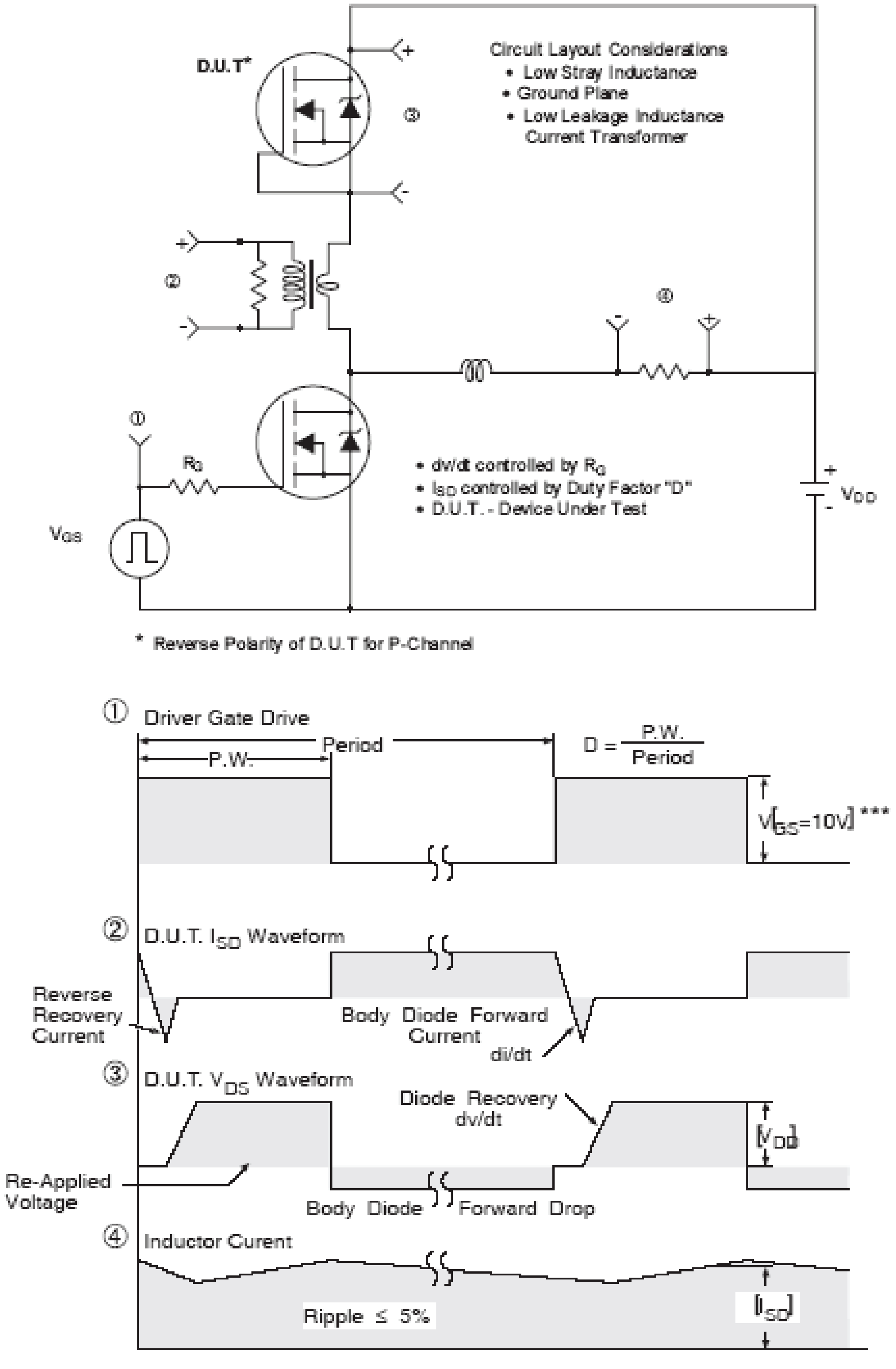


Fig 13b. Gate Charge Test Circuit

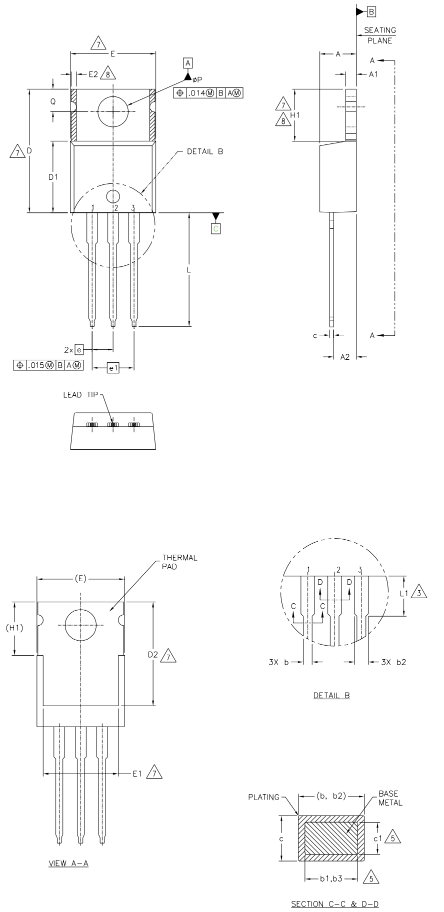


* Reverse Polarity of D.U.T for P-Channel

*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 14. Peak Diode Recovery dv/dt Test Circuit for P-Channel HEXFET® Power MOSFETs

TO-220AB Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1.– DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M– 1994.
2.– DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3.– LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4.– DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5.– DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
6.– CONTROLLING DIMENSION : INCHES.
7.– THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
8.– DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
9.– OUTLINE CONFORMS TO JEDEC TO–220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	1.14	1.40	.045	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	–	0.76	–	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE

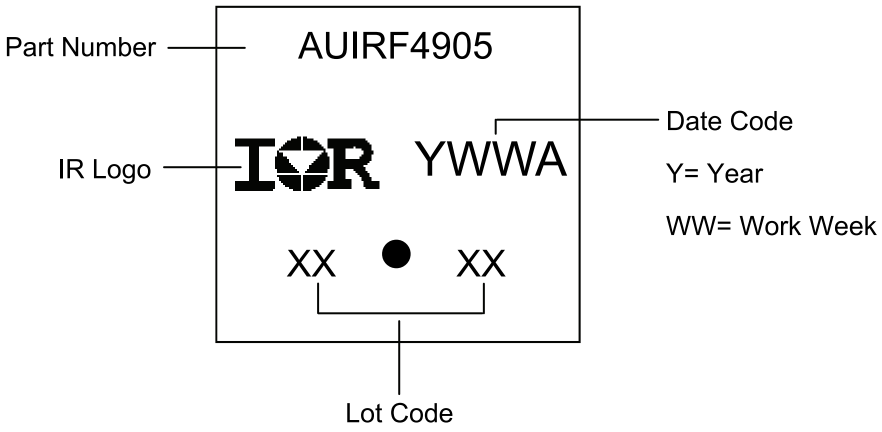
IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER

DIODES

1.– ANODE
2.– CATHODE
3.– ANODE

TO-220 Part Marking Information



Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information

Qualification Level		Automotive (per AEC-Q101) Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		3L-TO-220	N/A
ESD	Machine Model	Class M4 (+/- 425V)† AEC-Q101-002	
	Human Body Model	Class H2 (+/- 4000V)† AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 1125V)† AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
09/20/2017	• Updated datasheet with corporate template • Corrected typo error on package outline and part marking on page 8.

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