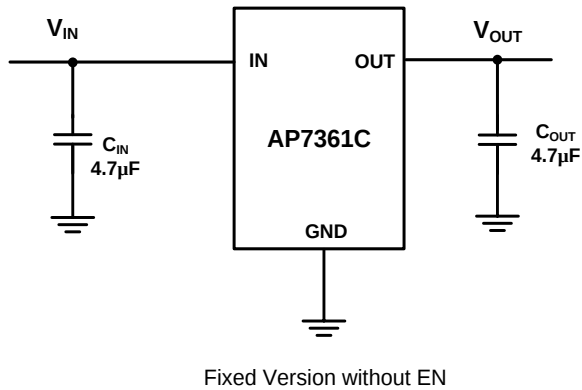
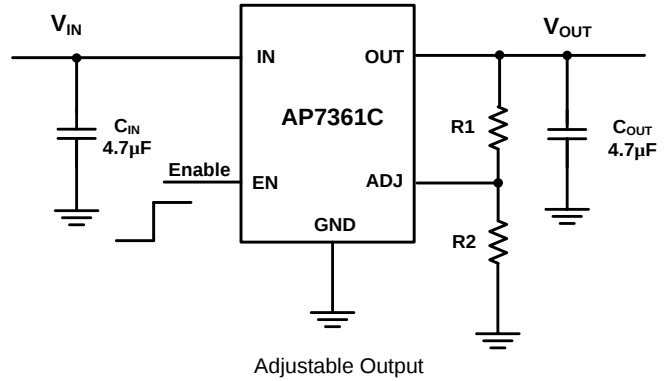
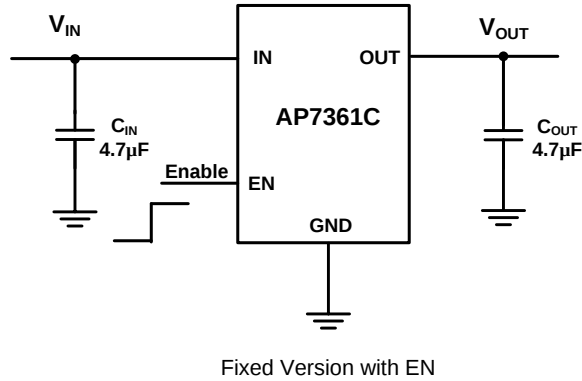


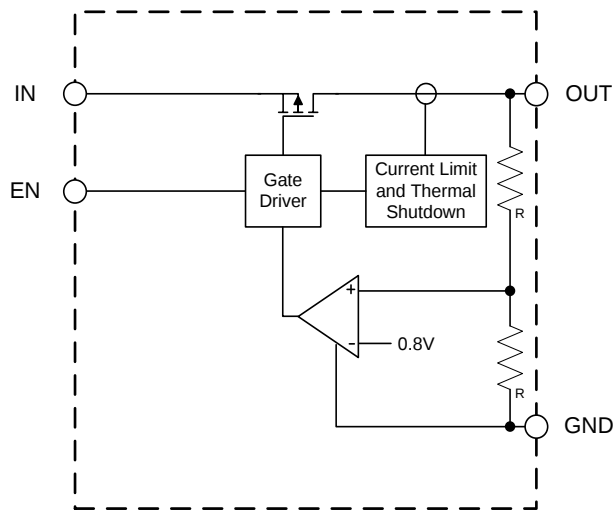
Typical Applications Circuit



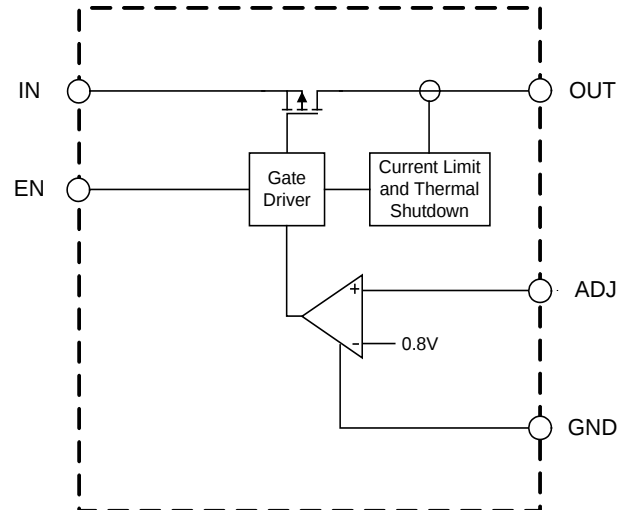
Pin Descriptions

Pin Number								Pin Name	Function
U-DFN3030-8 (Type E)	SOT89-5	TO252 (DPAK)	TO252 (DPAK)R	SOT223	SOT223R	SO-8EP	SO-8EPR		
8	4	1	3	1	3	8	8	IN	The input of the regulator. Bypass to ground through at least 1µF ceramic capacitor.
1	5	3	2	3	2	1	1	OUT	The output of the regulator. Bypass to ground through at least 2.2µF ceramic capacitor. For improved ac load response a larger capacitor is recommended.
4	2	2	1	2	1	4	3	GND	Ground
3	3	–	–	–	–	–	2	ADJ/NC	Adjustable voltage version only – a resistor divider from this pin to the OUT pin and ground sets the output voltage.
5	1	–	–	–	–	2	5	EN	Enable input, active high
2, 6, 7	–	–	–	–	–	3, 5, 6, 7	4, 6, 7	NC	No connection

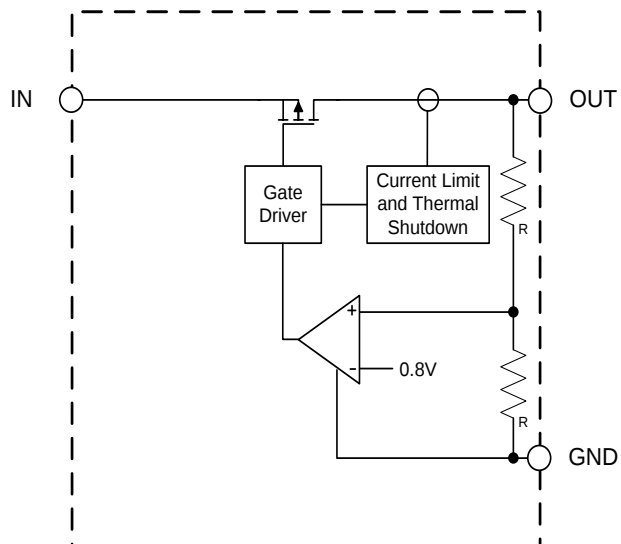
Functional Block Diagram



Fixed Version with EN



Adjustable Version



Fixed Version without EN

Absolute Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.) (Note 4)

Symbol	Parameter		Rating	Unit
V_{IN}	Input Voltage		6.5	V
—	OUT, ADJ, EN Voltage		$V_{IN} + 0.3$	V
T_J	Operating Junction Temperature Range		-40 to +150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		-65 to +150	$^\circ\text{C}$
P_D	Power Dissipation		Internally limited by maximum junction temperature of +150 $^\circ\text{C}$	
P_D	Power Dissipation	U-DFN3030-8 (Type E)	1700	mW
		TO252 (DPAK)	1250	
		SOT223	1100	
		SOT89-5	800	
		SO-8EP	1190	
ESD HBM	Human Body Model ESD Protection		> 2	KV
ESD MM	Machine Model ESD Protection (Note 5)		> 200	V

- Notes:
- Stresses greater than the 'Absolute Maximum Ratings' specified above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.
 - ESD MM rating at 150V for EN pin in SOT89-5 package.

Recommended Operating Conditions (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	2.2	6.0	V
V_{OUT}	Output Voltage	0.8	5.0	V
I_{OUT}	Output Current (Note 6)	0	1.0	A
T_A	Operating Ambient Temperature	-40	+85	$^\circ\text{C}$

- Notes:
- The device maintains a stable, regulated output voltage without a load current. When the output current is large, attention should be given to the limitation of the package power dissipation.

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, $V_{IN} = V_{OUT} + 1\text{V}$, $C_{IN} = 4.7\mu\text{F}$, $C_{OUT} = 4.7\mu\text{F}$, $V_{EN} = V_{IN}$, unless otherwise specified.)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V _{REF}	FB Reference Voltage, ADJ pin	I _{OUT} = 10mA, T _A = +25°C		0.792	0.8	0.808	V
I _{ADJ}	ADJ Pin Leakage Current	–		–	0.1	0.5	μA
I _Q	Input Quiescent Current	Enabled, I _{OUT} = 0A		–	60	80	μA
I _{SHDN}	Input Shutdown Current	V _{EN} = 0V, I _{OUT} = 0A		-1	0.05	1	μA
V _{OUT}	Output Voltage Accuracy	I _{OUT} = 100mA, T _A = +25°C	1.0V≤V _{OUT} <1.5V	V _{OUT} (s)- 0.015	V _{OUT} (s)	V _{OUT} (s)+ 0.015	V
			1.5 V≤V _{OUT} ≤3.3V	V _{OUT} (s)* 0.99	V _{OUT} (s)	V _{OUT} (s)* 1.01	
$\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$	Line Regulation	V _{IN} = V _{OUT} +1V to 5.5V, I _{OUT} = 100mA	T _A = +25°C	–	0.01	0.1	%V
			-40°C ≤T _A ≤ +85°C	–	–	0.2	
ΔV _{OUT} / V _{OUT}	Load Regulation	I _{OUT} from 1.0mA to 1A	1.2V<V _{OUT} ≤ 3.3V	-1.0	–	1.0	%
			1.0V□V _{OUT} ≤1.2V	-1.5	–	1.5	%
V _{DROPOUT}	Dropout Voltage (Note 7)	I _{OUT} = 300mA	1.0V≤V _{OUT} <1.1V	–	710	750	mV
			1.1V≤V _{OUT} <1.2V	–	600	640	
			1.2V≤V _{OUT} <1.3V	–	500	540	
			1.3V≤V _{OUT} <1.4V	–	400	440	
			1.4V≤V _{OUT} <1.5V	–	300	340	
			1.5V≤V _{OUT} <2.6V	–	200	250	
			2.6V≤V _{OUT} ≤3.3V	–	90	140	
		I _{OUT} = 1A	1.0V≤V _{OUT} <1.1V	–	840	–	
			1.1V≤V _{OUT} <1.2V	–	780	–	
			1.2V≤V _{OUT} <1.3V	–	710	–	
			1.3V≤V _{OUT} <1.4V	–	660	–	
			1.4V≤V _{OUT} <1.5V	–	610	–	
			1.5V≤V _{OUT} <2.0V	–	570	–	
			2.0V≤V _{OUT} <2.6V	–	440	–	
			2.6V≤V _{OUT} ≤3.3V	–	340	–	
V _{IL}	EN Input Logic Low Voltage	–	0	–	0.3	V	
V _{IH}	EN Input Logic High Voltage	–	1.0	–	V _{IN}	V	
R _{ENPD}	EN Pull-Down Resistor	–	–	3.0	–	MΩ	
I _{EN}	EN Input Leakage Current	V _{IN} = 5.5V, V _{EN} = 0V	-0.1	–	0.1	μA	
R _{PD}	Output Discharge Resistor	V _{OL} =1V	–	100	–	Ω	
I _{OUT}	Maximum Output Current	V _{IN} = V _{OUT} +1V	1.0	–	–	A	
I _{LIMIT}	Current Limit	V _{IN} = V _{OUT} +1V(V _{IN} MIN=2.2V)	1.1	1.5	–	A	
I _{SHORT}	Short-Circuit Current	V _{IN} = V _{OUT} +1V, Output Voltage < 15% V _{OUT}	–	400	–	mA	
PSRR	Power Supply Rejection Ratio (Note 8)	f = 1kHz, I _{OUT} = 100mA	–	75	–	dB	
		f = 10kHz, I _{OUT} = 100mA	–	55	–		
t _{ST}	Start-Up Time	V _{OUT} = 3V, C _{OUT} = 2.2μF, R _L = 30Ω	–	150	–	μs	
$\frac{\Delta V_{OUT}}{\Delta T_A \times V_{OUT}}$	Output Voltage Temperature Coefficient	I _{OUT} = 100mA, -40°C ≤ T _A ≤ +85°C	–	±100	–	ppm/°C	
T _{SHDN}	Thermal Shutdown Threshold	–	–	150	–	°C	
T _{HYS}	Thermal Shutdown Hysteresis	–	–	20	–	°C	

Notes: 7. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value. This parameter only applies to output voltages above 1.2V since minimum $V_{IN} = 2.2\text{V}$.

8. For $V_{IN} \geq 2.5\text{V}$ and $V_{IN} = V_{OUT} + 1\text{V}$. For $V_{IN} < 2.5\text{V}$, the PSRR performance may be reduced.

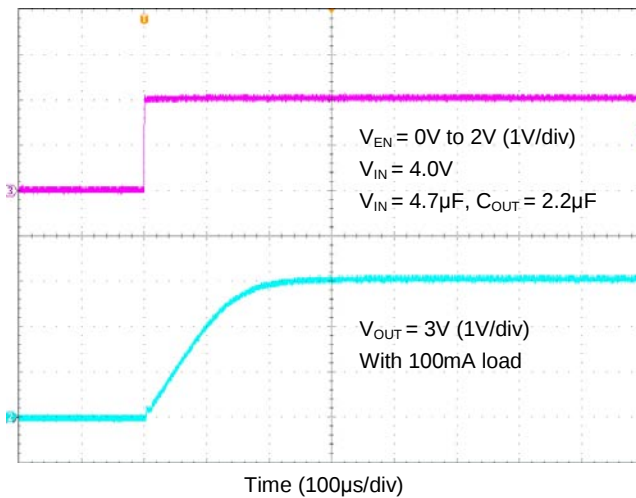
Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, $V_{IN} = V_{OUT} + 1\text{V}$, $C_{IN} = 4.7\mu\text{F}$, $C_{OUT} = 4.7\mu\text{F}$, $V_{EN} = V_{IN}$, unless otherwise specified.)
(Cont.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
θ_{JA}	Thermal Resistance Junction-to-Ambient	U-DFN3030-8 (Type E) (Note 9)	—	70	—	$^\circ\text{C/W}$
		TO252 (DPAK) (Note 9)	—	95	—	
		SOT223 (Note 9)	—	110	—	
		SOT89-5 (Note 9)	—	150	—	
		SO-8EP (Note 9)	—	100	—	

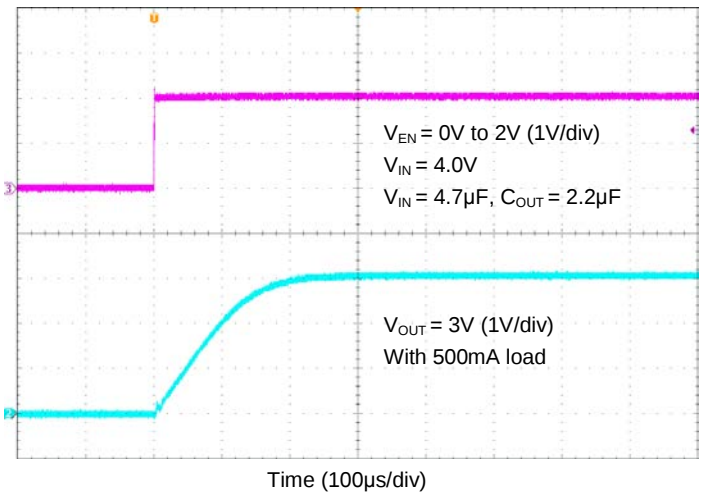
Notes: 9. Test condition: U-DFN3030-8 (Type E), SO-8EP devices are mounted on 2"x2", FR-4 substrate PCB, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane. TO252(DPAK) devices are mounted on 2"x2" FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout. For SOT223, the device is mounted on FR-4 substrate PC board, with minimum recommended pad layout. SOT89-5 devices are mounted on 1"x1" FR-4 substrate PC board, with minimum recommended pad layout.

Performance Characteristics

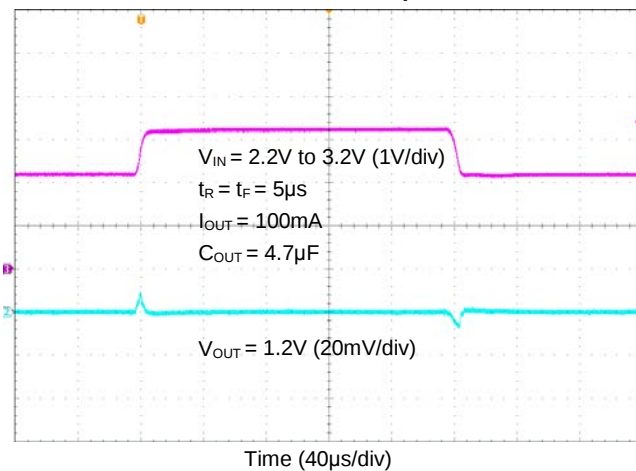
Start-up Time



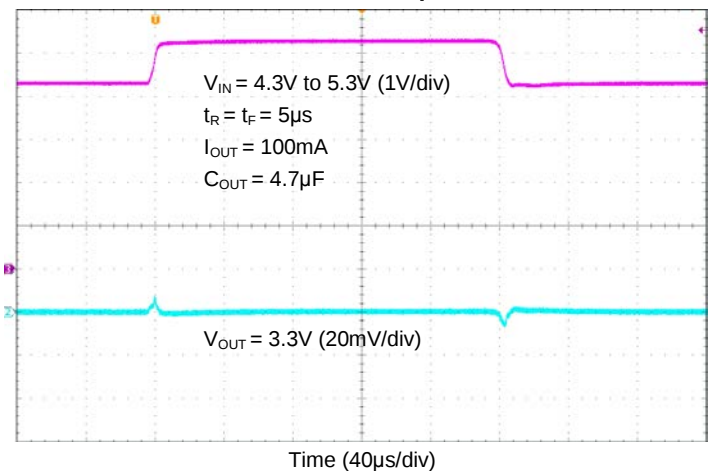
Start-up Time



Line Transient Response

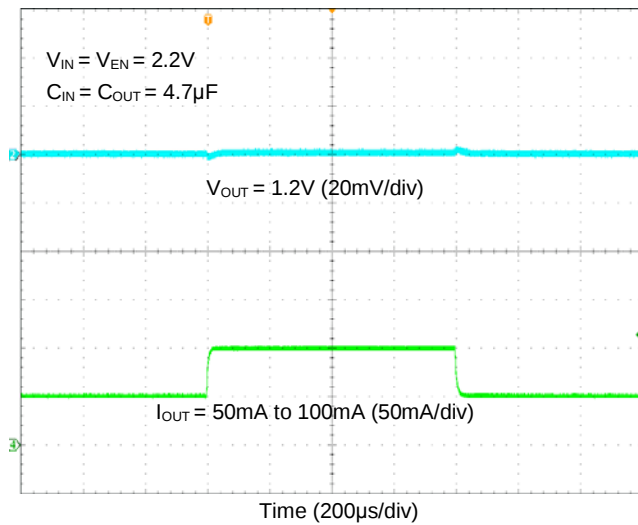


Line Transient Response

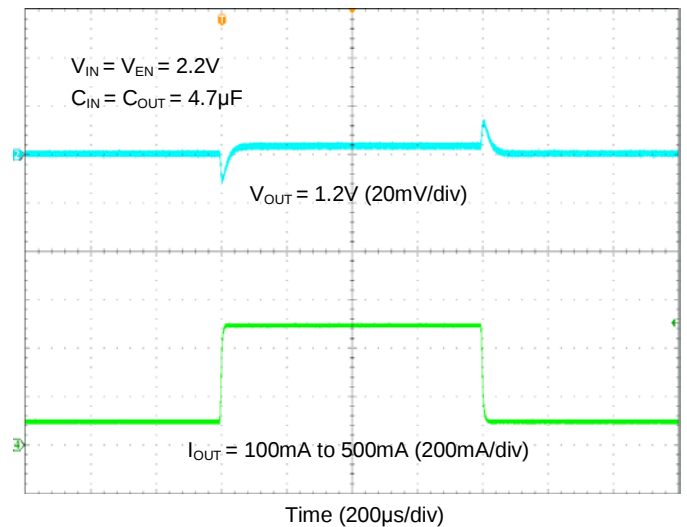


Performance Characteristics (Cont.)

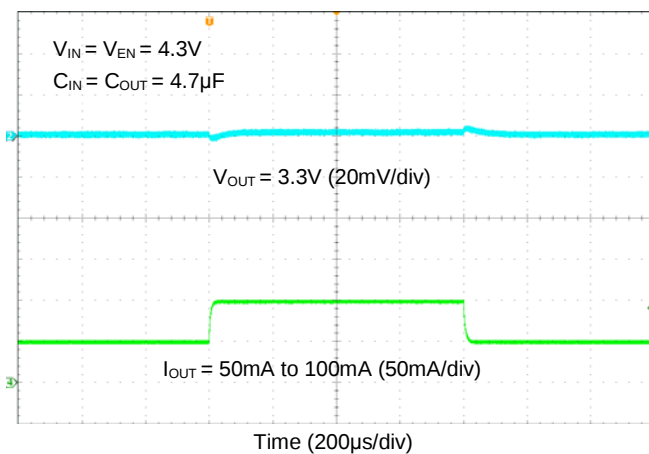
Load Transient Response



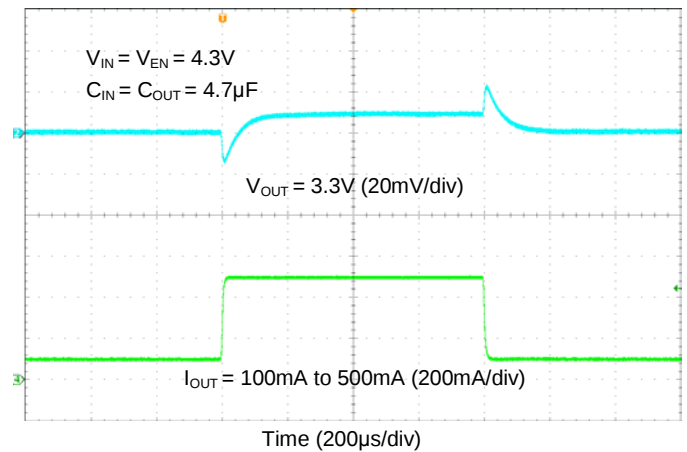
Load Transient Response



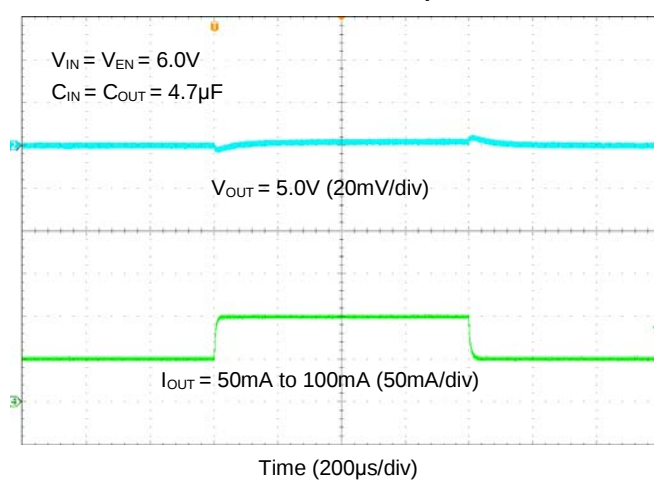
Load Transient Response



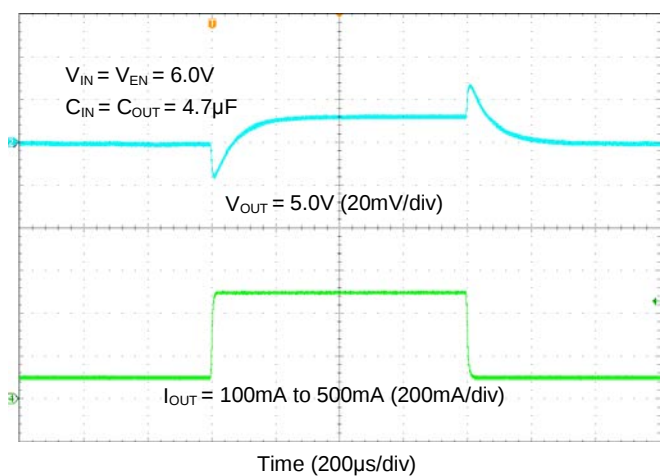
Load Transient Response



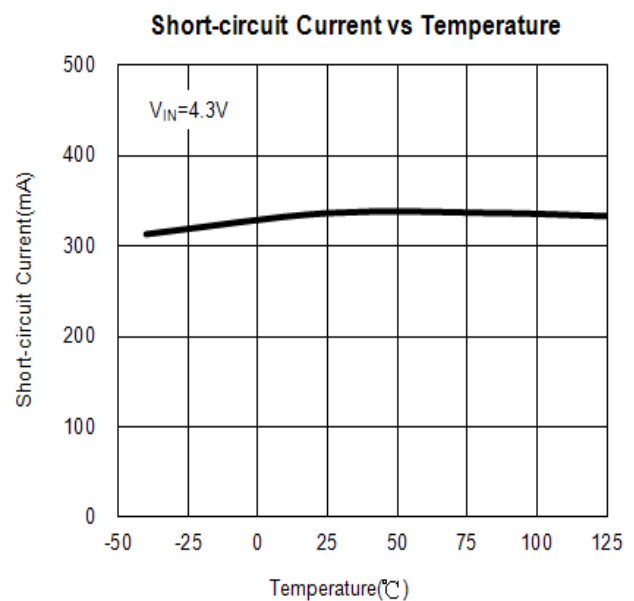
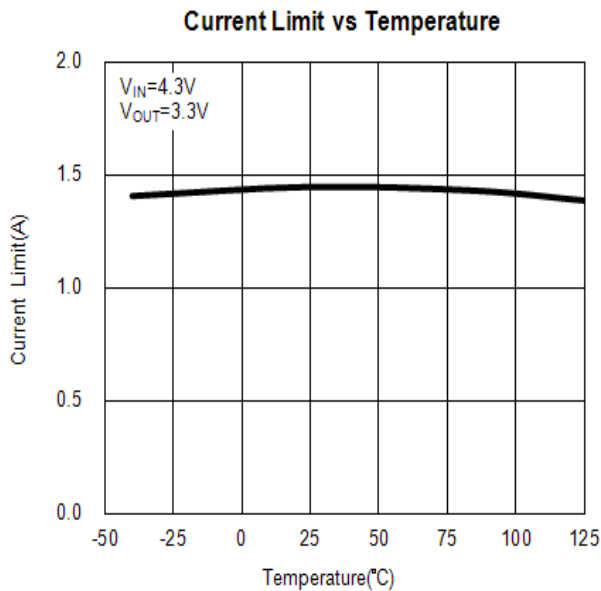
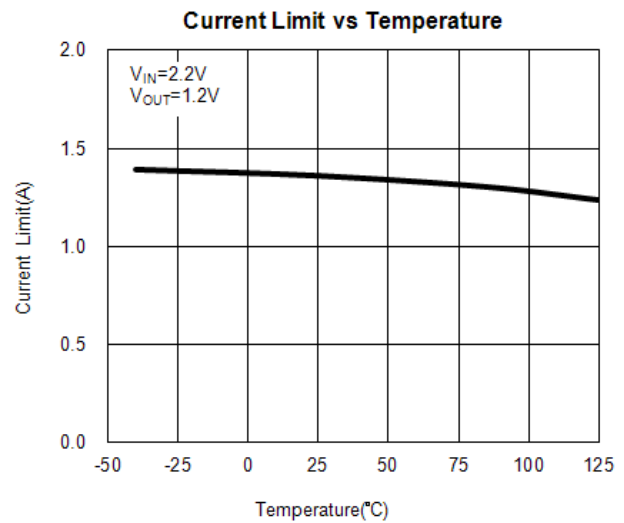
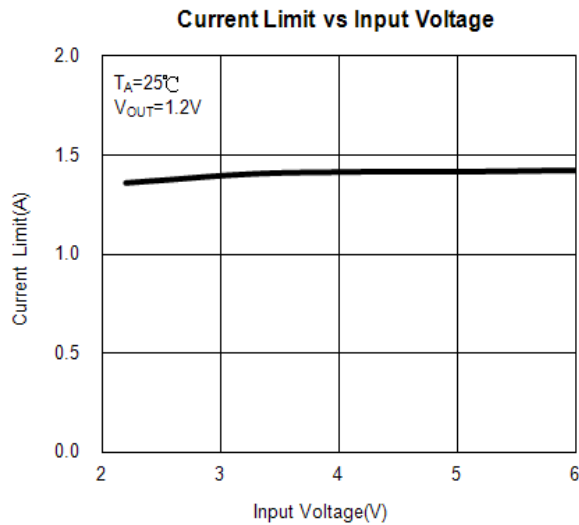
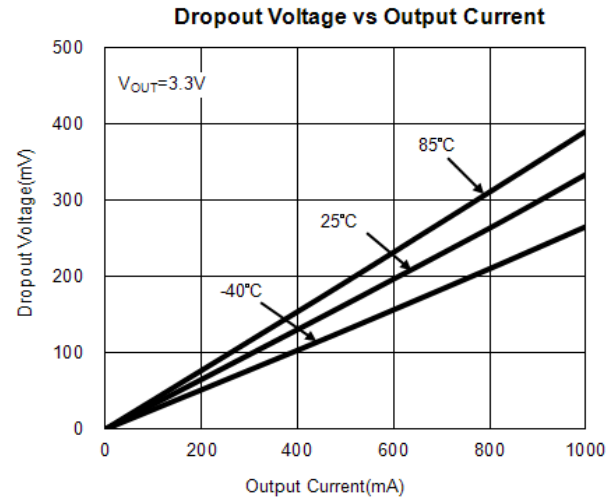
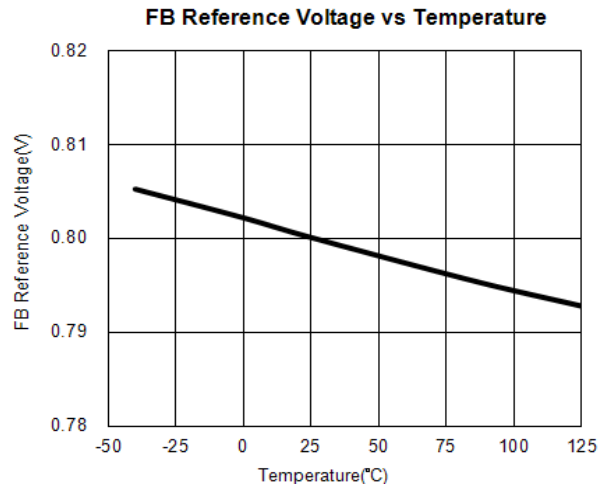
Load Transient Response



Load Transient Response

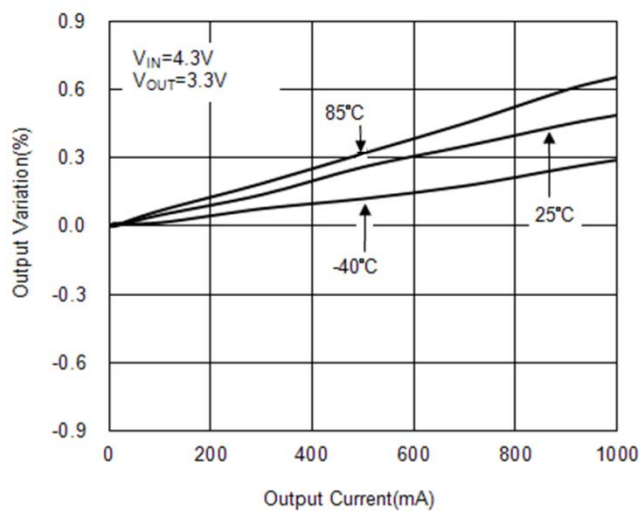


Performance Characteristics (Cont.)

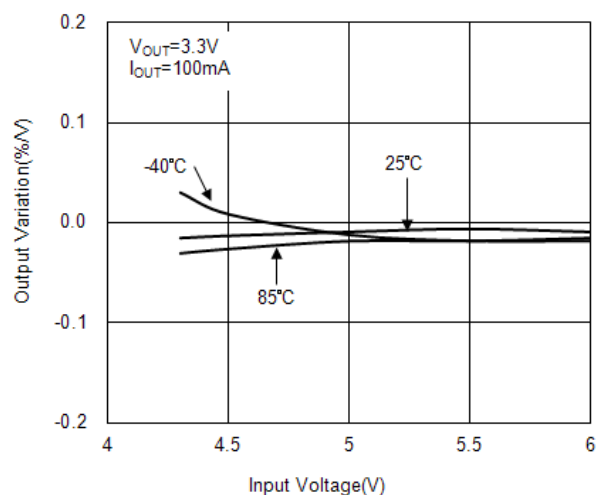


Performance Characteristics (Cont.)

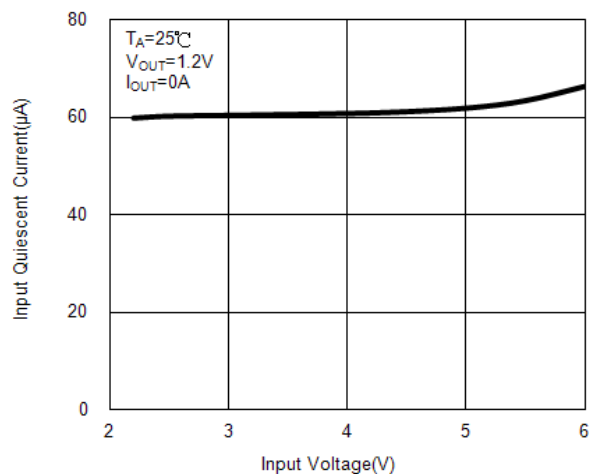
Load Regulation



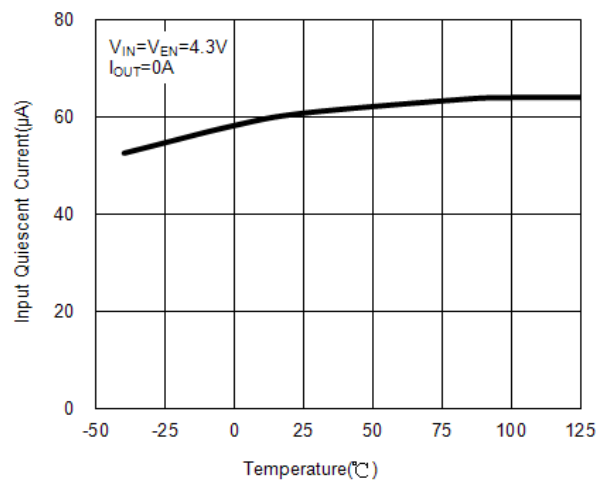
Line Regulation

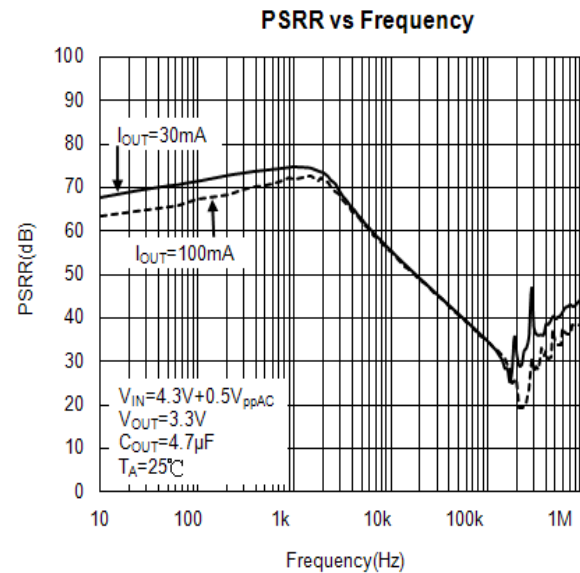
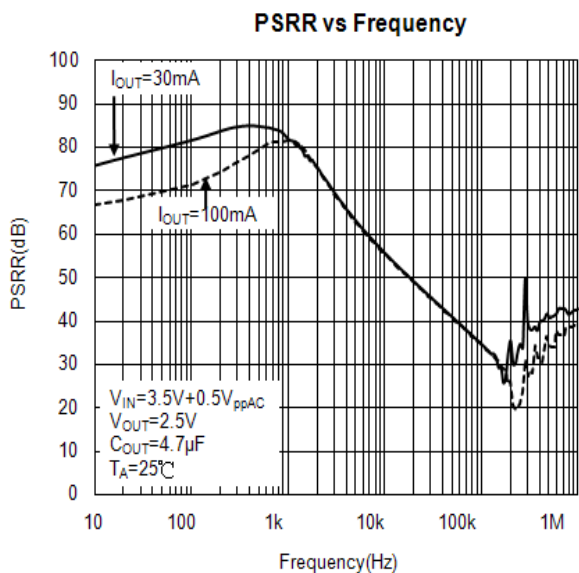
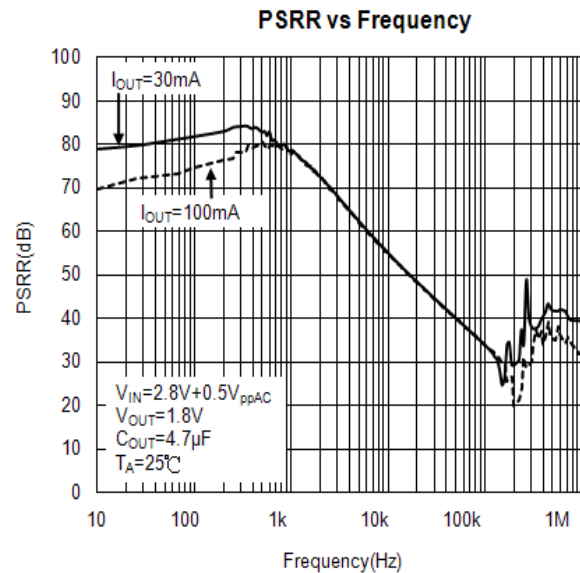
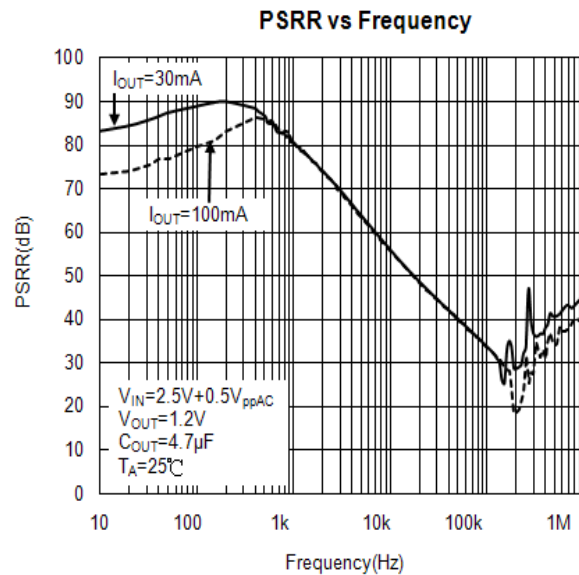


Input Quiescent Current vs Input Voltage



Input Quiescent Current vs Temperature



Performance Characteristics (Cont.)

Application Information
Input Capacitor

A 1 μF ceramic capacitor is recommended between the IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and reduce noise. For PCB layout, a wide copper trace is required for both IN and GND pins. A lower ESR capacitor type allows the use of less capacitance, while higher ESR type requires more capacitance.

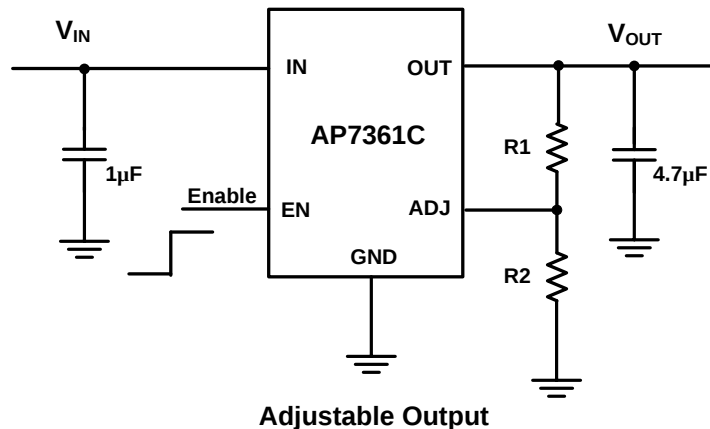
Output Capacitor

The output capacitor is required to stabilize and improve the transient response of the LDO. The AP7361C is stable with very small ceramic output capacitors. Using a ceramic capacitor value that is at least 2.2 μF on the output ensures stability. Higher capacitance values help to improve line and load transient response. The output capacitance may be increased to keep low undershoot and overshoot. Output capacitor must be placed as close as possible to OUT and GND pins.

Application Information (Cont.)

Adjustable Operation

The AP7361C provides output voltage from 0.8V to 5.0V through external resistor divider as shown below.



The output voltage is calculated by:

$$V_{OUT} = V_{REF} \left(1 + \frac{R_1}{R_2} \right)$$

Where $V_{REF} = 0.8V$ (the internal reference voltage)

Rearranging the equation will give the following that is used for adjusting the output to a particular voltage:

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

To maintain the stability of the internal reference voltage, R_2 needs to be kept smaller than $80k\Omega$.

No Load Stability

Other than external resistor divider, no minimum load is required to keep the device stable. The device will remain stable and regulated in no load condition.

ON/OFF Input Operation

The ON/OFF feature is not available in the SOT223 and TO252 (DPAK) packages.

The AP7361C is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH} .

Current Limit Protection

When output current at OUT pin is higher than current limit threshold, the current limit protection will be triggered and clamp the output current to prevent over-current and to protect the regulator from damage due to overheating.

Short Circuit Protection

When OUT pin is short-circuit to GND, short circuit protection will be triggered and clamp the output current to approximately 400mA. Full current is restored when the output voltage exceeds 15% of V_{OUT} . This feature protects the regulator from over-current and damage due to overheating.

Application Information (Cont.)

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +150°C, allowing the device to cool down. When the junction temperature reduces to approximately +130°C the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Ultra Fast Start-up

After enabled, the AP7361C is able to provide full power in as little as tens of microseconds, typically 200µs, without sacrificing low ground current. This feature will help load circuitry move in and out of standby mode in real time, eventually extend battery life for mobile phones and other portable devices.

Low Quiescent Current

The AP7361C, consuming only around 60µA for all input range, provides great power saving in portable and low power applications.

Power Dissipation

The device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoid thermal shutdown and ensure reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated by:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

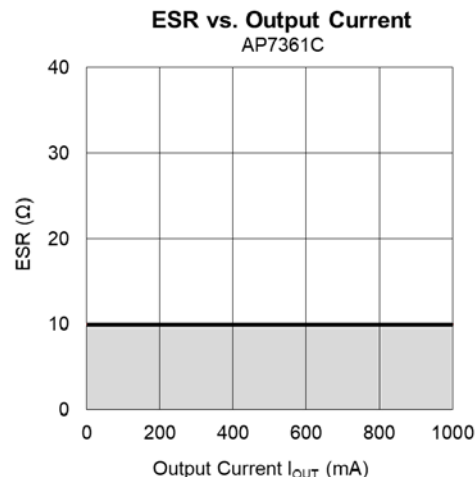
The maximum power dissipation, handled by the device, depends on the maximum junction to ambient thermal resistance, maximum ambient temperature, and maximum device junction temperature, which can be calculated by the equation in the following:

$$P_D(\text{max}@T_A) = \frac{(+150^\circ\text{C} - T_A)}{R_{\theta JA}}$$

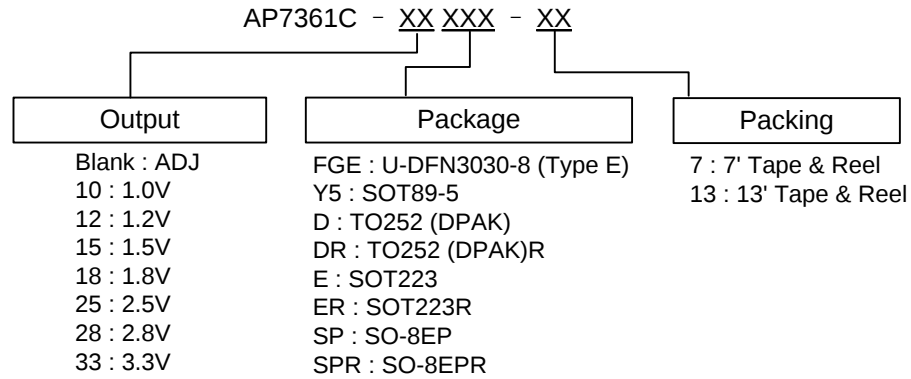
ESR vs. Output Current

Ceramic type output capacitor is recommended for this series; however, the other output capacitors with low ESR also can be used. The relations between I_{OUT} (Output Current) and ESR of an output capacitor are shown below. The stable region for the safety operating temperature (-40°C ~ +85°C) is marked as the gray area in the graph.

Measurement conditions: Frequency Band: 10Hz to 2MHz, Temperature: -40°C to +85°C.



Ordering Information

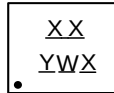


Part Number	Package Code	Packaging	7"/13" Tape and Reel	
			Quantity	Part Number Suffix
AP7361C-XXFGE-7	FGE	U-DFN3030-8 (Type E)	3000/Tape & Reel	-7
AP7361C-XXY5-13	Y5	SOT89-5	2500/Tape & Reel	-13
AP7361C-XXD-13	D	TO252 (DPAK)	2500/Tape & Reel	-13
AP7361C-XXDR-13	DR	TO252 (DPAK)R	2500/Tape & Reel	-13
AP7361C-XXE-13	E	SOT223	2500/Tape & Reel	-13
AP7361C-XXER-13	ER	SOT223R	2500/Tape & Reel	-13
AP7361C-XXSP-13	SP	SO-8EP	2500/Tape & Reel	-13
AP7361C-XXSPR-13	SPR	SO-8EPR	2500/Tape & Reel	-13

Marking Information

(1) U-DFN3030-8 (Type E)

(Top View)

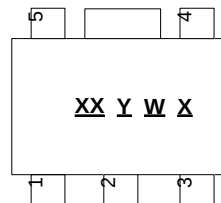


XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
 a~z : 27~52 week; z represents
 52 and 53 week
Z : Internal Code

Device	Package	Identification Code
AP7361C-ADJ	U-DFN3030-8 (Type E)	SH
AP7361C-10	U-DFN3030-8 (Type E)	SJ
AP7361C-12	U-DFN3030-8 (Type E)	SK
AP7361C-15	U-DFN3030-8 (Type E)	SV
AP7361C-18	U-DFN3030-8 (Type E)	SW
AP7361C-25	U-DFN3030-8 (Type E)	SX
AP7361C-28	U-DFN3030-8 (Type E)	SY
AP7361C-33	U-DFN3030-8 (Type E)	SZ

(2) SOT89-5

(Top View)



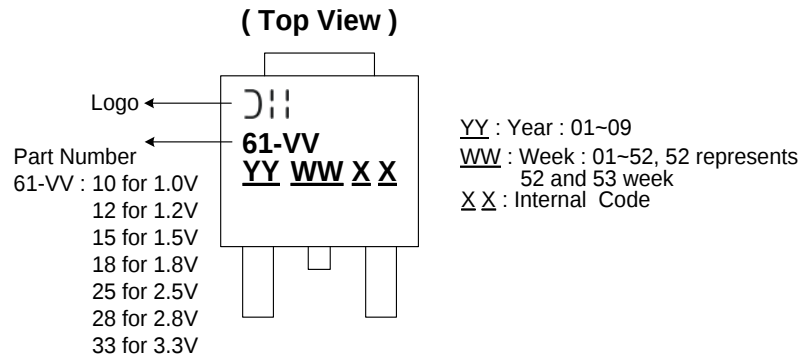
XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
 a~z : 27~52 week;
 z represents 52 and 53 week
Z : Internal Code

Device	Package	Identification Code
AP7361C-ADJ	SOT89-5	KR
AP7361C-10	SOT89-5	KS
AP7361C-12	SOT89-5	KT
AP7361C-15	SOT89-5	KU
AP7361C-18	SOT89-5	KV
AP7361C-25	SOT89-5	KW
AP7361C-28	SOT89-5	KX
AP7361C-33	SOT89-5	KZ

Marking Information (Cont.)

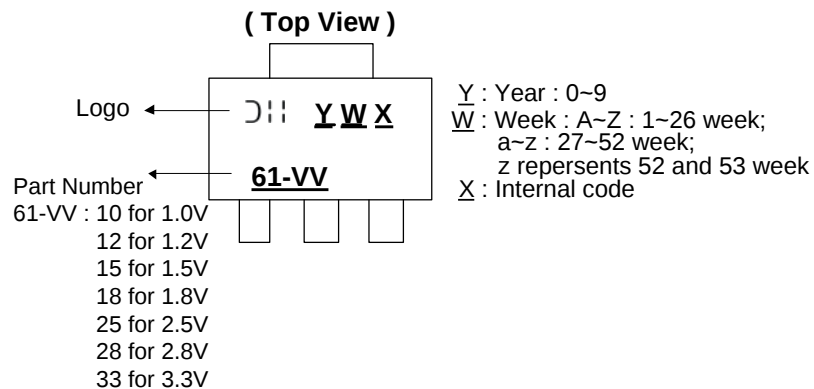
(3) TO252 (DPAK)

Pin 1: IN, Pin 2: GND, Pin 3: OUT



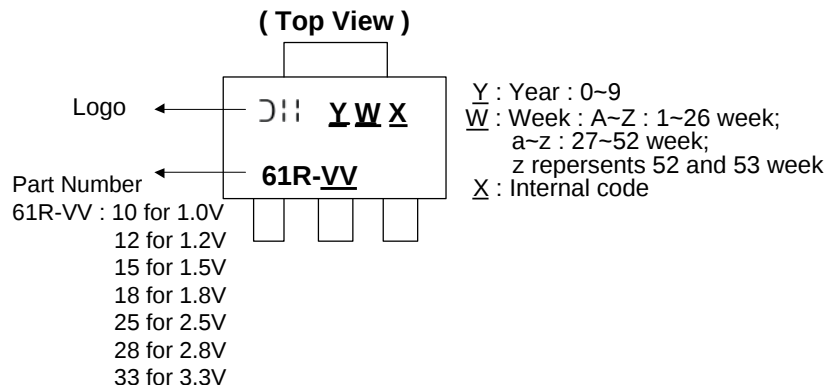
(4) SOT223

Pin 1: IN, Pin 2: GND, Pin 3: OUT



(5) SOT223R

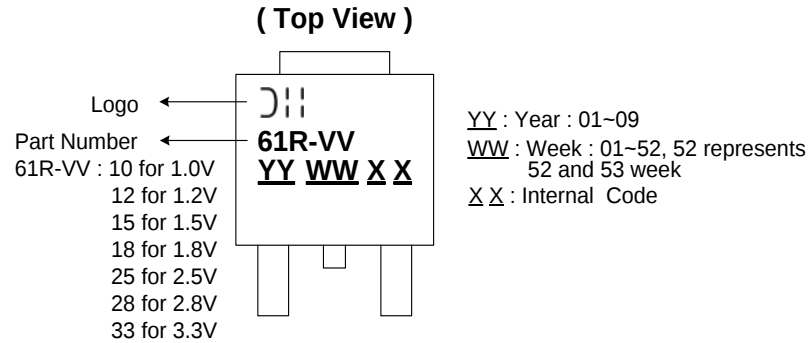
Pin 1: GND, Pin 2: OUT, Pin 3: IN



Marking Information (Cont.)

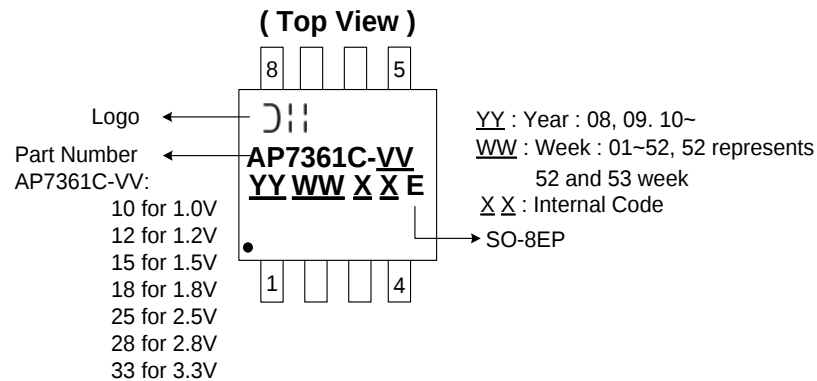
(6) TO252 (DPAK)R

Pin 1: GND, Pin 2: OUT, Pin 3: IN



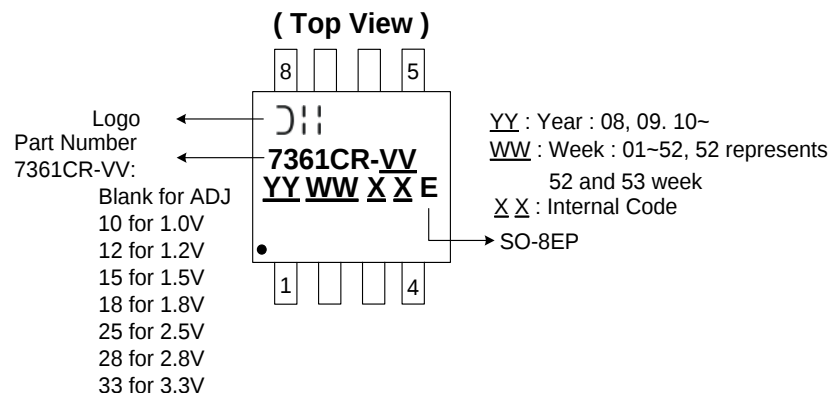
(7) SO-8EP

Pin 1: OUT, Pin 2: EN, Pins 3, 5, 6 and 7: NC, Pin 4: GND, Pin 8: IN



(8) SO-8EPR

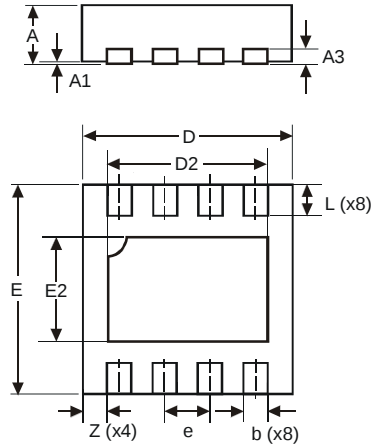
Pin 1: OUT, Pin 2: ADJ/NC, Pin 3: GND, Pins 4, 6 and 7: NC, Pin 5: EN, Pin 8: IN



Package Outline Dimensions (All dimensions in mm.)

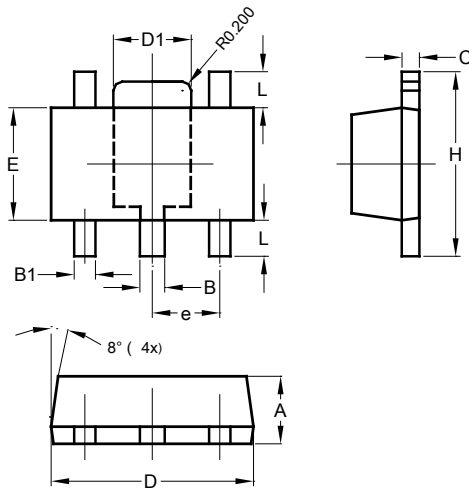
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(1) Package Type: U-DFN3030-8 (Type E)



U-DFN3030-8 Type E			
Dim	Min	Max	Typ
A	0.57	0.63	0.60
A1	0	0.05	0.02
A3	—	—	0.15
b	0.20	0.30	0.25
D	2.95	3.05	3.00
D2	2.15	2.35	2.25
E	2.95	3.05	3.00
e	—	—	0.65
E2	1.40	1.60	1.50
L	0.30	0.60	0.45
Z	—	—	0.40
All Dimensions in mm			

(2) Package Type: SOT89-5

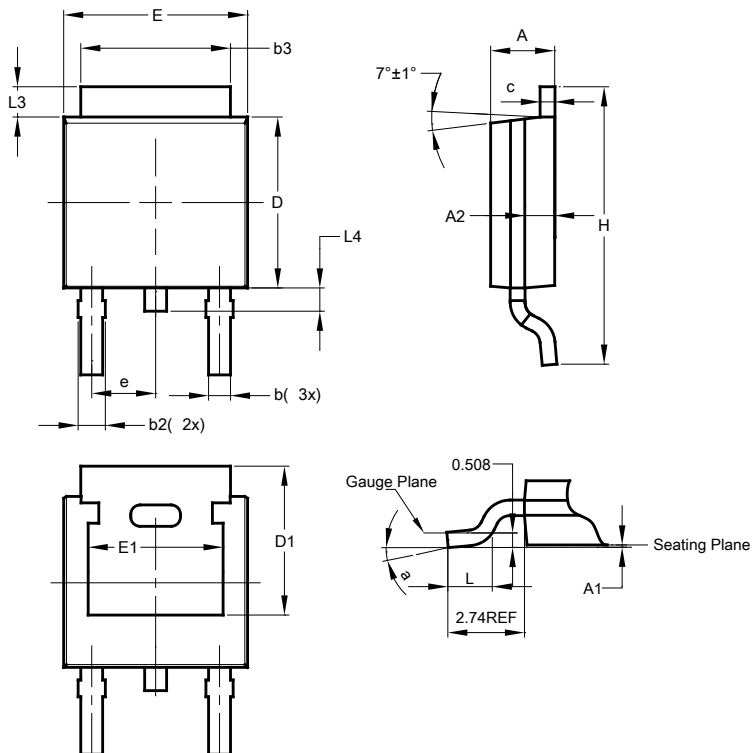


SOT89-5			
Dim	Min	Max	Typ
A	1.40	1.60	1.50
B	0.50	0.62	0.56
B1	0.44	0.54	0.48
C	0.35	0.43	0.38
D	4.40	4.60	4.50
D1	1.62	1.83	1.733
E	2.40	2.60	2.50
e	—	—	1.50
H	3.95	4.25	4.10
L	0.65	0.95	0.80
All Dimensions in mm			

Package Outline Dimensions (Cont.) (All dimensions in mm.)

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(3) Package Type: TO252 (DPAK)

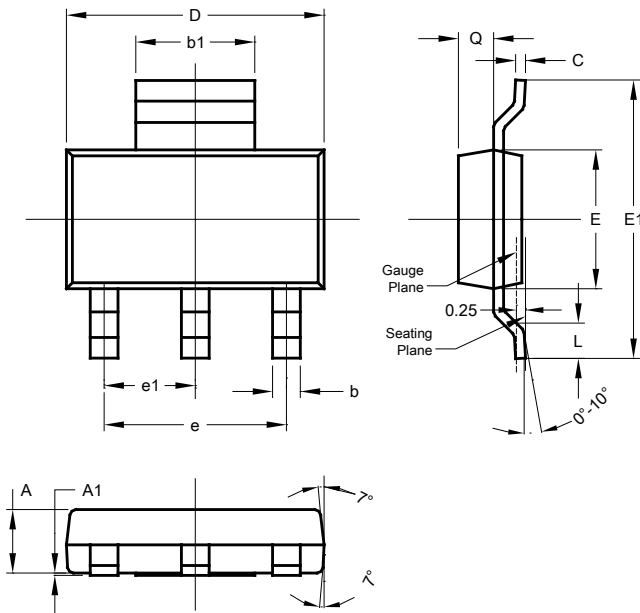


TO252 (DPAK)			
Dim	Min	Max	Typ
A	2.19	2.39	2.29
A1	0.00	0.13	0.08
A2	0.97	1.17	1.07
b	0.64	0.88	0.783
b2	0.76	1.14	0.95
b3	5.21	5.46	5.33
c	0.45	0.58	0.531
D	6.00	6.20	6.10
D1	5.21	-	-
e	-	-	2.286
E	6.45	6.70	6.58
E1	4.32	-	-
H	9.40	10.41	9.91
L	1.40	1.78	1.59
L3	0.88	1.27	1.08
L4	0.64	1.02	0.83
a	0°	10°	-
All Dimensions in mm			

Package Outline Dimensions (Cont.) (All dimensions in mm.)

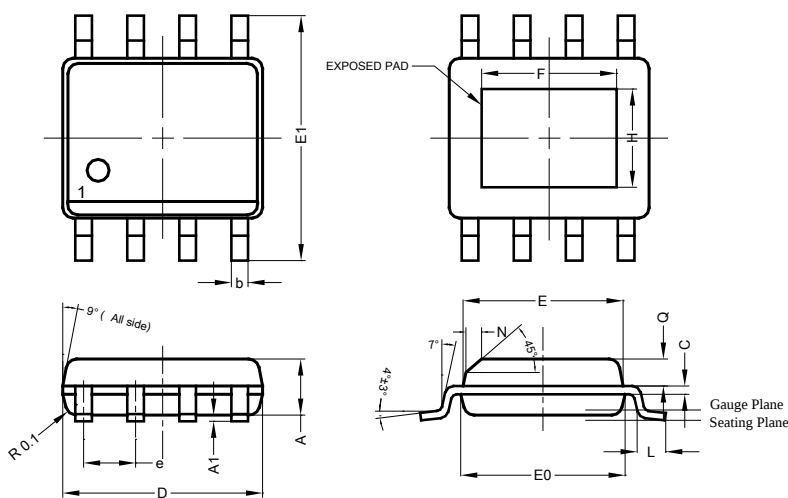
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(4) Package Type: SOT223



SOT223			
Dim	Min	Max	Typ
A	1.55	1.65	1.60
A1	0.010	0.15	0.05
b	0.60	0.80	0.70
b1	2.90	3.10	3.00
C	0.20	0.30	0.25
D	6.45	6.55	6.50
E	3.45	3.55	3.50
E1	6.90	7.10	7.00
e	-	-	4.60
e1	-	-	2.30
L	0.85	1.05	0.95
Q	0.84	0.94	0.89
All Dimensions in mm			

(5) Package Type: SO-8EP

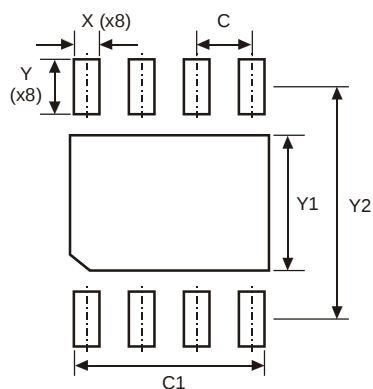


SO-8EP			
Dim	Min	Max	Typ
A	1.40	1.50	1.45
A1	0.00	0.13	-
b	0.30	0.50	0.40
C	0.15	0.25	0.20
D	4.85	4.95	4.90
E	3.80	3.90	3.85
E0	3.85	3.95	3.90
E1	5.90	6.10	6.00
e	-	-	1.27
F	2.75	3.35	3.05
H	2.11	2.71	2.41
L	0.62	0.82	0.72
N	-	-	0.35
Q	0.60	0.70	0.65
All Dimensions in mm			

Suggested Pad Layout

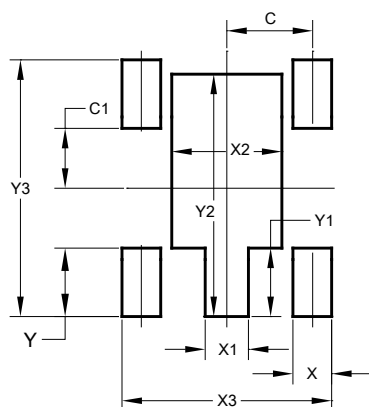
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(1) Package Type: U-DFN3030-8 (Type E)



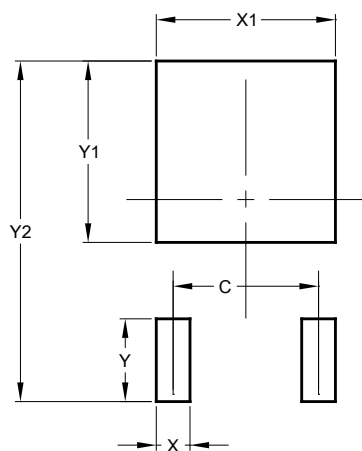
Dimensions	Value (in mm)
C	0.65
C1	2.35
X	0.30
Y	0.65
Y1	1.60
Y2	2.75

(2) Package Type: SOT89-5



Dimensions	Value (in mm)
C	1.500
C1	1.050
X	0.680
X1	0.760
X2	1.930
X3	3.680
Y	1.200
Y1	1.200
Y2	4.250
Y3	4.500

(3) Package Type: TO252 (DPAK)

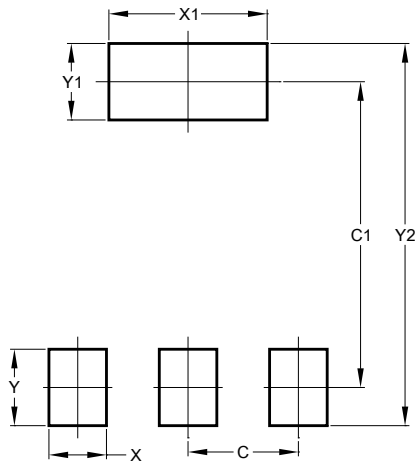


Dimensions	Value (in mm)
C	4.572
X	1.060
X1	5.632
Y	2.600
Y1	5.700
Y2	10.700

Suggested Pad Layout (Cont.)

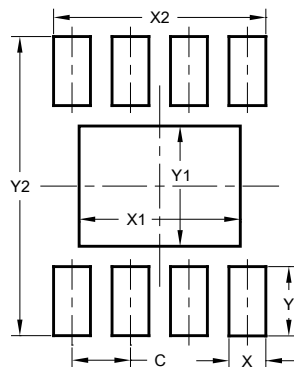
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(4) Package Type: SOT223



Dimensions	Value (in mm)
C	2.30
C1	6.40
X	1.20
X1	3.30
Y	1.60
Y1	1.60
Y2	8.00

(5) Package Type: SO-8EP



Dimensions	Value (in mm)
C	1.270
X	0.802
X1	3.502
X2	4.612
Y	1.505
Y1	2.613
Y2	6.500

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