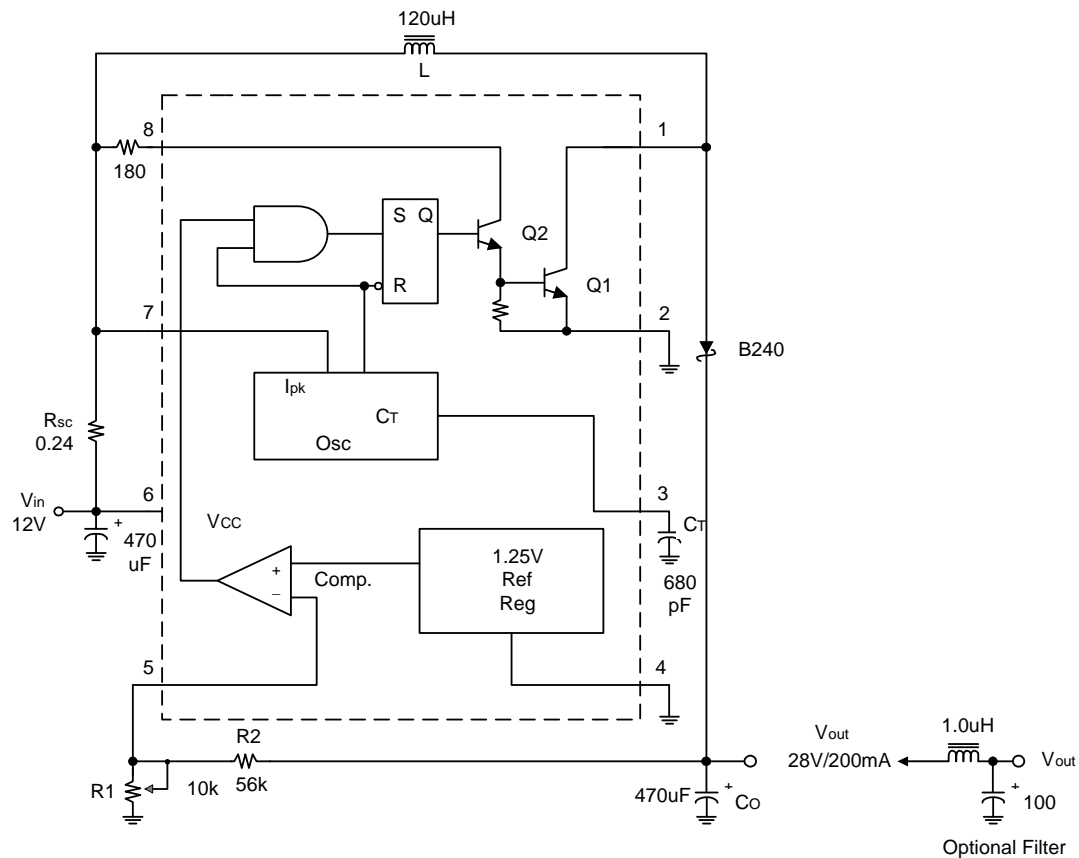


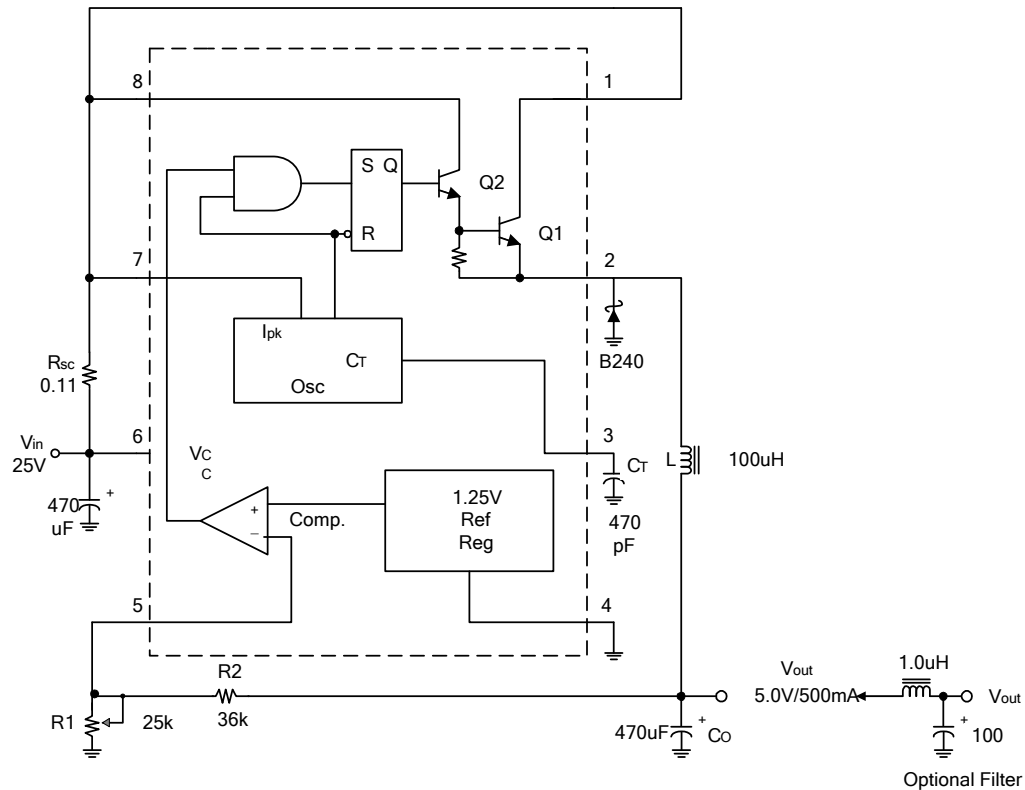
Typical Applications Circuit

(1) Step-Up Converter



Test	Conditions	Results
Line Regulation	$V_{IN} = 9V$ to $12V$, $I_O = 200mA$	$20mV = \pm 0.035\%$
Load Regulation	$V_{IN} = 12V$, $I_O = 50mA$ to $200mA$	$15mV = \pm 0.035\%$
Output Ripple	$V_{IN} = 12V$, $I_O = 200mA$	$500mV_{PP}$
Efficiency	$V_{IN} = 12V$, $I_O = 200mA$	80%

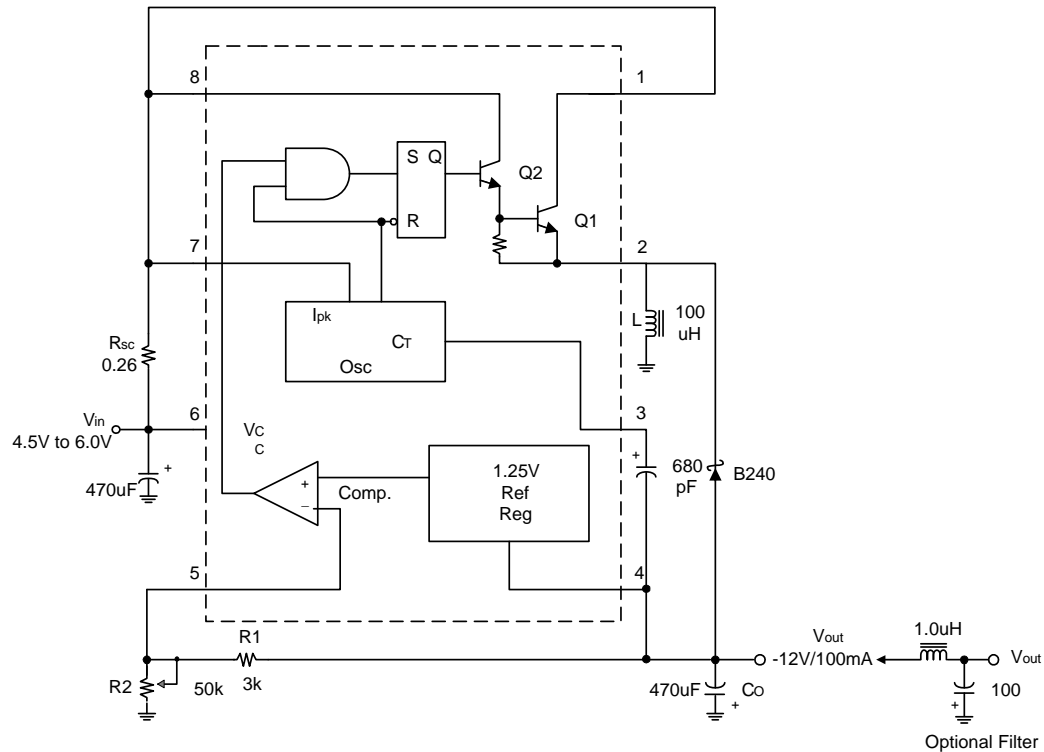
(2) Step-Down Converter



Test	Conditions	Results
Line Regulation	$V_{IN} = 12V$ to $24V$, $I_O = 500mA$	$20mV = \pm 0.2\%$
Load Regulation	$V_{IN} = 24V$, $I_O = 50mA$ to $500mA$	$5mV = \pm 0.05\%$
Output Ripple	$V_{IN} = 24V$, $I_O = 500mA$	$160mV_{PP}$
Efficiency	$V_{IN} = 24V$, $I_O = 500mA$	82%

Typical Applications Circuit (cont.)

(3) Voltage Inverting Converter



Test	Conditions	Results
Line Regulation	$V_{IN} = 4.5V \text{ to } 6.0V, I_O = 100mA$	$20mV = \pm 0.08\%$
Load Regulation	$V_{IN} = 5.0V, I_O = 20mA \text{ to } 100mA$	$30mV = \pm 0.12\%$
Output Ripple	$V_{IN} = 5.0V, I_O = 100mA$	$500mV_{PP}$
Efficiency	$V_{IN} = 5.0V, I_O = 100mA$	60%

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.

Symbol	Parameter		Value	Unit
V _{CC}	Power Supply Voltage		40	V
V _{IR}	Comparator Input Voltage Range		-0.3 to +40	V
V _{C(SWITCH)}	Switch Collector Voltage		40	V
V _{E(SWITCH)}	Switch Emitter Voltage (V _{PIN 1} = 40V)		40	V
V _{CE(SWITCH)}	Switch Collector to Emitter Voltage		40	V
V _{C(DRIVER)}	Driver Collector Voltage		40	V
I _{C(DRIVER)}	Driver Collector Current		100	mA
I _{SW}	Switch Current		1.6	A
P _D	Power Dissipation (Note 4)	SO-8: T _A = +25°C	600	mW
		PDIP-8: T _A = +25°C	1.25	W
θ _{JA}	Thermal Resistance	SO-8	117	°C/W
		PDIP-8	138	
θ _{JC}		SO-8	19	
		PDIP-8	25	
T _{MJ}	Maximum Junction Temperature (Note 5)		+150	°C
T _{OP}	Operating Junction Temperature Range		0 to +105	°C
T _{stg}	Storage Temperature Range		-65 to +150	°C

Notes: 4. Maximum package power dissipation limits must be observed.

5. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

Electrical Characteristics (V_{CC} = 5.0V, unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit
OSCILLATOR					
f _{OSC}	Frequency (V _{PIN 5} = 0V, C _T = 1.0nF, T _A = +25°C)	24	33	42	kHz
I _{CHG}	Charge Current (V _{CC} = 5.0V to 40V, T _A = +25°C)	24	30	42	μA
I _{DISCHG}	Discharge Current (V _{CC} = 5.0V to 40V, T _A = +25°C)	140	200	260	μA
I _{DISCHG} / I _{CHG}	Discharge to Charge Current Ratio (Pin 7 to V _{CC} , T _A = +25°C)	5.2	6.5	7.5	—
V _{ipk (SENSE)}	Current Limit Sense Voltage (I _{CHG} = I _{DISCHG} , T _A = +25°C)	300	400	450	mV
OUTPUT SWITCH (Note 3)					
V _{CE (sat)}	Saturation Voltage, Darlington Connection (I _{SW} = 1.0A, Pins 1, 8 connected)	—	1.0	1.3	V
V _{CE (sat)}	Saturation Voltage, Darlington Connection (I _{SW} = 1.0A, I _D = 50mA, Forced β ≈ 20)	—	0.45	0.7	V
h _{FE}	DC Current Gain (I _{SW} = 1.0A, V _{CE} = 5.0V, T _A = +25°C)	50	75	—	—
I _{C(off)}	Collector Off-State Current (V _{CE} = 40V)	—	0.01	100	μA
COMPARATOR					
V _{th}	Threshold Voltage	—	—	—	V
—	T _A = +25°C	1.225	1.25	1.275	—
—	T _A = 0°C to +70°C	1.21	—	1.29	—
Reg _{LINE}	Threshold Voltage Line Regulation (V _{CC} = 3.0V to 40V)	—	1.4	6.0	mV
TOTAL DEVICE					
I _{CC}	Supply Current (V _{CC} = 5.0V to 40V, C _T = 1.0nF, Pin 7 = V _{CC} , V _{PIN 5} > V _{TH} Pin 2 = Gnd, remaining pins open)	—	—	3.5	mA

The schematic diagram illustrates the internal components of the Ipk Sense Amplifier, enclosed in a dashed box. The circuit includes an Ipk Oscillator (CT) block, a Comparator, a 1.25V Reference Regulator, an S-Q flip-flop, and a driver stage with transistors Q1 and Q2. The input pins are labeled: Drive Collector (8), Ipk Sense (7), Vcc (6), and Comparator Inverting Input (5). The output pins are labeled: Switch Collector (1), Switch Emitter (2), Timing Capacitor (3), and Gnd (4). The Ipk Sense input (7) is connected to the Ipk Oscillator and the Comparator. The Drive Collector input (8) is connected to the driver stage. The Comparator's non-inverting input (+) is connected to the 1.25V Reference Regulator. The S-Q flip-flop's S input is connected to the Ipk Oscillator, and its Q output is connected to the driver stage. The driver stage consists of a 100Ω resistor in series with transistor Q2, which is connected to the Switch Collector output (1). Transistor Q1 is connected to the Switch Emitter output (2). The Timing Capacitor (3) is connected to the CT block. The 1.25V Reference Regulator is connected to the Comparator's non-inverting input (+) and the Gnd pin (4).

(Bottom View)

Typical Performance Characteristics

Figure 1. $V_{ce(sat)}$ versus I_e

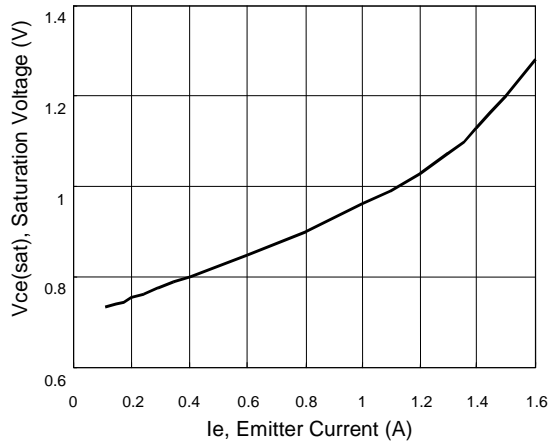


Figure 2. Reference Voltage versus Temp.

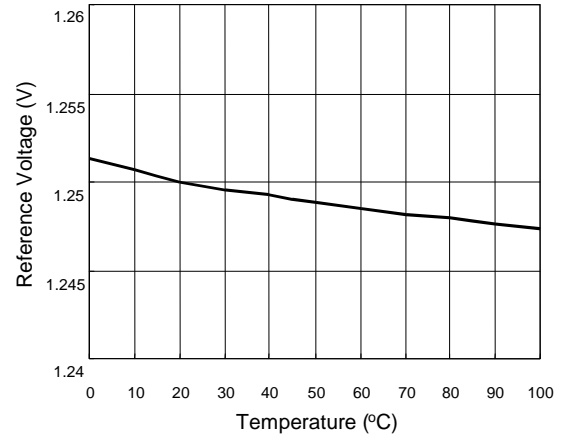


Figure 3. Current Limit Sense Voltage versus Temperature

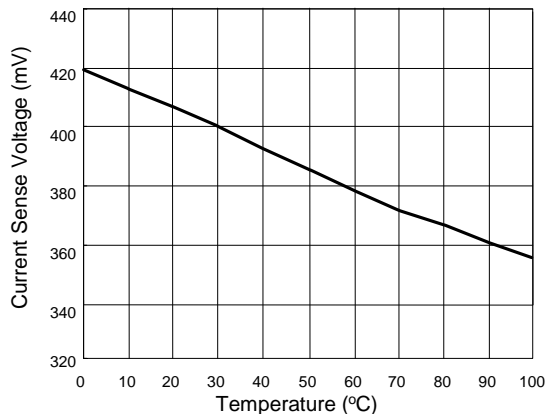


Figure 4. Standby Supply Current versus Supply Voltage

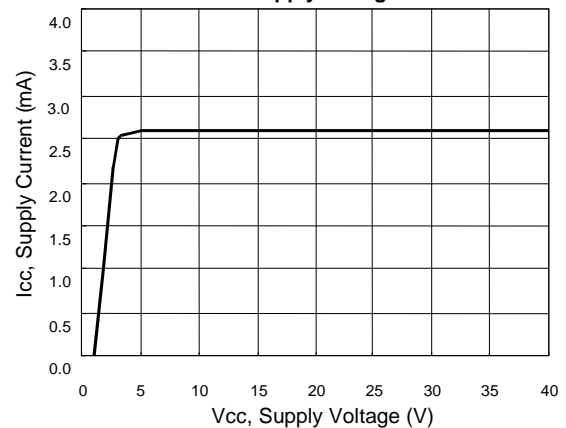


Figure 5. Emitter Follower Configuration Output Saturation Voltage vs. Emitter Current

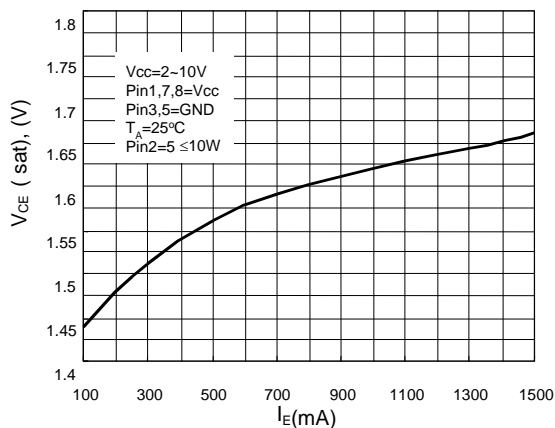
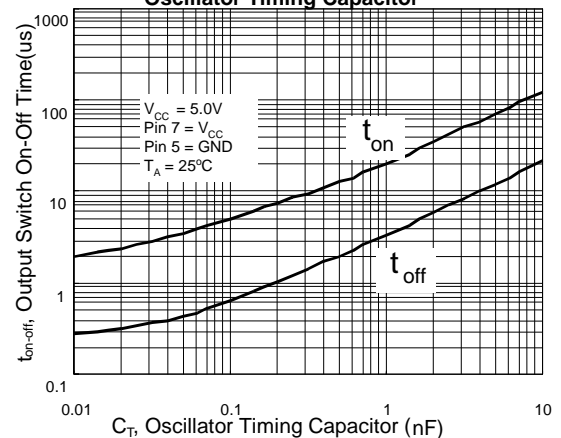


Figure 6. Output Switch On-Off Time versus Oscillator Timing Capacitor



Design Formula Table

Calculation	Step-Up				Step-Down				Voltage-Inverting			
t_{ON} / t_{OFF}	$V_{OUT} + V_F - V_{IN(MIN)}$				$V_{OUT} + V_F$				$ V_{OUT} + V_F$			
		$V_{IN(MIN)} - V_{SAT}$				$V_{IN(MIN)} - V_{SAT} - V_{OUT}$				$V_{IN(MIN)} - V_{SAT}$		
$(t_{ON} + t_{OFF})$	$1/f$				$1/f$				$1/f$			
t_{OFF}	$t_{ON} + t_{OFF}$				$t_{ON} + t_{OFF}$				$t_{ON} + t_{OFF}$			
		t_{ON}	+1			t_{ON}	+1			t_{ON}	+1	
		t_{OFF}				t_{OFF}				t_{OFF}		
t_{ON}	$(t_{ON} + t_{OFF}) - t_{OFF}$				$(t_{ON} + t_{OFF}) - t_{OFF}$				$(t_{ON} + t_{OFF}) - t_{OFF}$			
C_T	$4.0 \times 10^{-5} t_{ON}$				$4.0 \times 10^{-5} t_{ON}$				$4.0 \times 10^{-5} t_{ON}$			
$I_{PK} \text{ (switch)}$	$2I_{OUT(MAX)} (t_{ON} / t_{OFF} + 1)$				$2I_{OUT(MAX)}$				$2I_{OUT(MAX)} (t_{ON} / t_{OFF} + 1)$			
R_{SC}	$0.3 / I_{PK} \text{ (SWITCH)}$				$0.3 / I_{PK} \text{ (SWITCH)}$				$0.3 / I_{PK} \text{ (SWITCH)}$			
$L \text{ (MIN)}$		$(V_{IN(MIN)} - V_{SAT})$		$t_{ON(MAX)}$		$(V_{IN(MIN)} - V_{SAT} - V_{OUT})$		$t_{ON(MAX)}$		$(V_{IN(MIN)} - V_{SAT})$		$t_{ON(MAX)}$
		$I_{PK} \text{ (SWITCH)}$				$I_{PK} \text{ (SWITCH)}$				$I_{PK} \text{ (SWITCH)}$		
C_O	9	$I_{OUT} t_{ON}$				$I_{PK} \text{ (SWITCH)} (t_{ON} + t_{OFF})$			9	$I_{OUT} t_{ON}$		
		$V_{RIPPLE} \text{ (pp)}$				$8V_{RIPPLE} \text{ (pp)}$				$V_{RIPPLE} \text{ (pp)}$		

V_{SAT} = Saturation voltage of the output switch.

V_F = Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{IN} - Nominal input voltage.

V_{OUT} - Desired output voltage, $|V_{OUT}| = 1.25 (1 + R_2/R_1)$

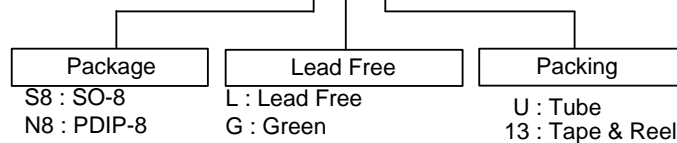
I_{OUT} - Desired output current.

F_{MIN} - Minimum desired output switching frequency at the selected values of V_{IN} and I_O .

$V_{RIPPLE(pp)}$ - Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

Ordering Information

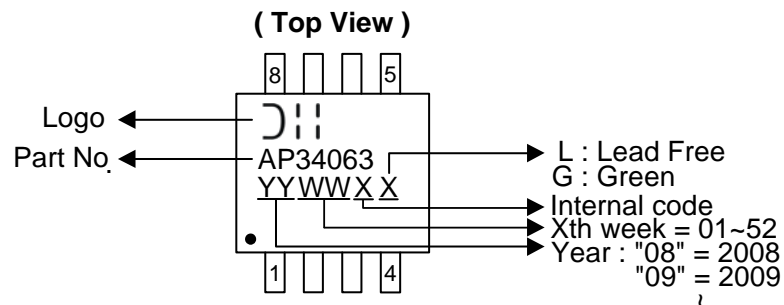
AP 34063 XX X - X



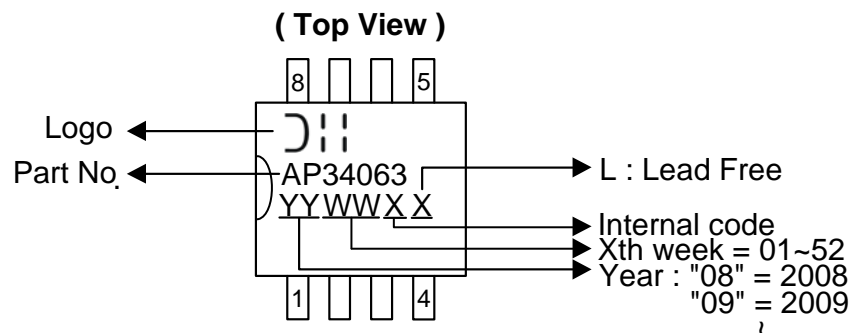
Part Number	Package Code	Packaging	Tube		13" Tape and Reel	
			Quantity	Part Number Suffix	Quantity	Part Number Suffix
AP34063S8L-13	S8	SO-8	NA	NA	2500/Tape & Reel	-13
AP34063S8G-13	S8	SO-8	NA	NA	2500/Tape & Reel	-13
AP34063N8L-U	N8	PDIP-8	60	- U	NA	NA

Marking Information

(1) SO-8



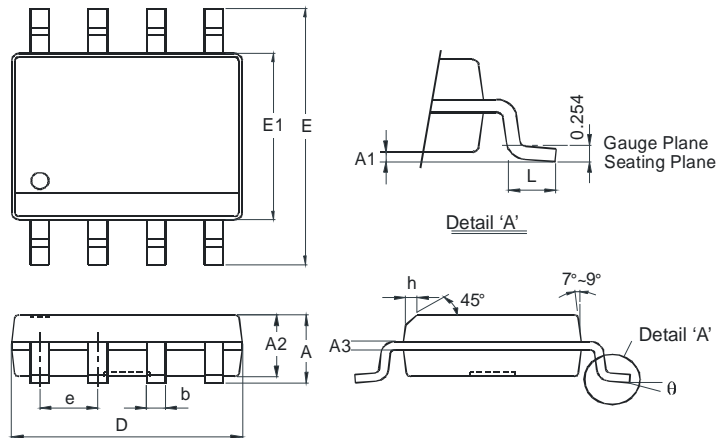
(2) PDIP-8



Package Outline Dimensions (All dimensions in mm.)

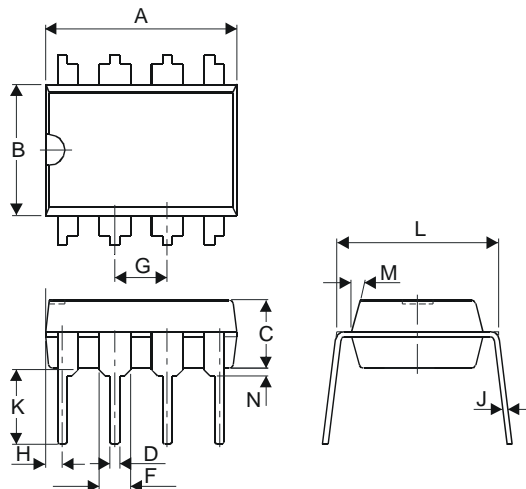
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.

(1) SO-8



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

(2) PDIP-8

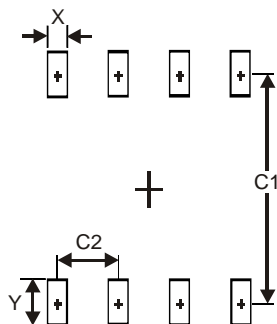


PDIP-8		
Dim	Min	Max
A	9.02	9.53
B	6.15	6.35
C	3.10	3.50
D	0.36	0.56
F	1.40	1.65
G	2.54 typ.	
H	0.71	0.97
J	0.20	0.36
K	2.92	3.81
L	7.62	8.26
M	—	15°
N	0.38 (min)	
All Dimensions in mm		

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.

(1) SO-8



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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