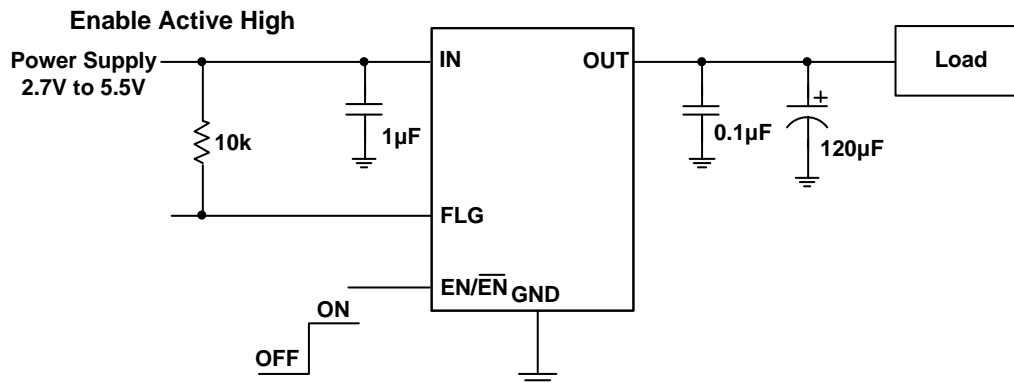


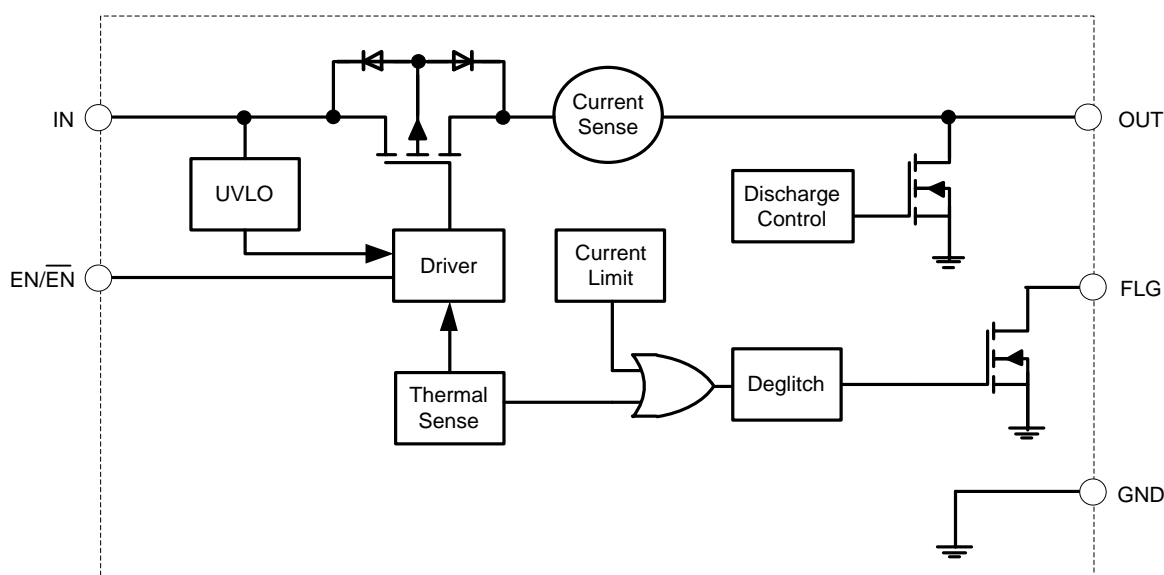
## Typical Applications Circuit



## Pin Descriptions

Pin Number		Pin Name	Function
SOT25	MSOP-8		
1	6, 7, 8	OUT	Voltage Output Pin, connect a 0.1µF bypass capacitor and a high-value capacitor to GND, close to IC. (At least 10µF in USB application.)
2	1	GND	Ground Pin of the Circuitry
3	5	FLG	Over Current and Over temperature fault report; Open-Drain flag is active low when triggered.
4	4	EN/ $\overline{\text{EN}}$	Enable Input
			AP22811A: Active High
			AP22811B: Active Low
5	2, 3	IN	Voltage Input Pin, connect a 1µF low ESR capacitor to GND, close to IC.

## Functional Block Diagram



# Absolute Maximum Ratings (@ $T_A = +25^{\circ}\text{C}$ , unless otherwise specified.) (Note 4)

Symbol	Parameter	Ratings	Unit
ESD HBM	Human Body ESD Protection	2000	V
ESD MM	Machine Model ESD Protection	200	V
$V_{IN}$	Input Voltage	-0.3 to 6.0	V
$V_{OUT}$	Output Voltage	-0.3 to ( $V_{IN} + 0.3$ )	V
$V_{EN/\overline{EN}}$	Enable Voltage	-0.3 to ( $V_{IN} + 0.3$ )	V
$I_L$	Load Current	Internal Limited	A
$T_{J(max)}$	Maximum Junction Temperature	+150	$^{\circ}\text{C}$
$T_{ST}$	Storage Temperature	-65 to +150	$^{\circ}\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	SOT25 (Note 6)	123
		MSOP-8 (Note 5)	165
$R_{\theta JC}$	Thermal Resistance, Junction to Case	SOT25 (Note 6)	33
		MSOP-8 (Note 5)	33

- Notes:
- Stresses greater than the 'Absolute Maximum Ratings' specified above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.
  - Test condition for MSOP-8: Device mounted on 1"x1"/2"x2" FR-4 substrate PC board, 2oz copper with minimum recommended pad layout.
  - $R_{\theta JA}$  and  $R_{\theta JC}$  are measured at  $T_A = +25^{\circ}\text{C}$  on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

# Recommended Operating Conditions (Note 7)

Symbol	Parameter	Min	Max	Unit
$V_{IN}$	Input Voltage	2.7	5.5	V
$I_{OUT}$	Output Current	0	2	A
$V_{IL}$	$\overline{EN}/\overline{EN}$ Input Logic Low Voltage	0	0.5	V
$V_{IH}$	$\overline{EN}/\overline{EN}$ Input Logic High Voltage	1.5	$V_{IN}$	V
$T_A$	Operating Ambient Temperature	-40	+85	$^{\circ}\text{C}$

- Note:
- Refer to the typical application circuit.

**Electrical Characteristics** ( $V_{IN} = 5V$  @  $T_A = +25^\circ C$ ,  $C_{IN} = 1\mu F$ ,  $C_L = 100nF$ , unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{UVLO}$	Input UVLO	$V_{IN}$ Rising	1.6	2.0	2.4	V
$\Delta V_{UVLO}$	Input UVLO Hysteresis	$V_{IN}$ Decreasing	—	180	—	mV
$I_{SHDN}$	Input Shutdown Current	Disabled, $O_{UT} = \text{Open}$	—	0.1	1	$\mu A$
$I_Q$	Input Quiescent Current	Enabled, $O_{UT} = \text{Open}$	—	80	—	$\mu A$
$I_{LEAK}$	Input Leakage Current	Disabled, $O_{UT}$ Grounded	—	0.1	1	$\mu A$
$I_{REV}$	Reverse Leakage Current	Disabled, $V_{IN} = 0V$ , $V_{OUT} = 5V$ , $I_{REV}$ at $V_{IN}$	—	0.01	1	$\mu A$
$R_{DS(ON)}$	Switch On-Resistance	$V_{IN} = 5V$ , $I_{OUT} = 1A$ $T_A = +25^\circ C$	—	50	65	m $\Omega$
		$V_{IN} = 3.3V$ , $I_{OUT} = 1A$ $T_A = +25^\circ C$	—	60	90	
$I_{LIMIT}$	Over Load Current Limit	$V_{IN} = 5V$ , $V_{OUT} = 4.5V$	2.2	2.7	3.2	A
$I_{SHORT}$	Short-Circuit Current Limit	Enabled, Output short to ground	—	0.3	—	A
$V_{IL}$	EN/ $\overline{EN}$ Input Logic Low Voltage	$V_{IN} = 2.7V$ to $5.5V$	—	—	0.5	V
$V_{IH}$	EN/ $\overline{EN}$ Input Logic High Voltage	$V_{IN} = 2.7V$ to $5.5V$	1.5	—	—	V
$I_{LEAK-EN/\overline{EN}}$	EN/ $\overline{EN}$ Input Leakage	$V_{IN} = 5V$ , $V_{EN/\overline{EN}} = 0V$ and $5.5V$	—	0.01	1	$\mu A$
$I_{LEAK-O}$	Output Leakage Current	Disabled, $V_{OUT} = 0V$	—	0.5	1	$\mu A$
$t_{D(ON)}$	Output Turn-On Delay Time	$C_L = 4.7\mu F$ , $R_{LOAD} = 10\Omega$ @ $V_{IN} = 3.3V$ Figure 1	—	1.7	—	ms
$t_R$	Output Turn-On Rise Time	$C_L = 4.7\mu F$ , $R_{LOAD} = 10\Omega$ @ $V_{IN} = 3.3V$ Figure 1	1.0	2.1	3.5	ms
$t_{D(OFF)}$	Output Turn-Off Delay Time	$C_L = 4.7\mu F$ , $R_{LOAD} = 10\Omega$ @ $V_{IN} = 3.3V$ Figure 1	—	20	—	$\mu s$
$t_F$	Output Turn-Off Fall Time	$C_L = 4.7\mu F$ , $R_{LOAD} = 100\Omega$ @ $V_{IN} = 3.3V$ Figure 1	—	0.65	—	ms
$R_{FLG}$	FLG Output FET On-Resistance	$I_{FLG} = 10mA$	—	40	60	$\Omega$
$I_{FOH}$	FLG Off Current	$V_{FLG} = 5V$	—	0.01	1	$\mu A$
$t_{BLANK}$	FLG Blanking Time	Assertion or deassertion due to overcurrent and over-temperature condition	2	6	13	ms
$t_{DIS}$	Discharge Time	$C_L = 1\mu F$ , $V_{IN} = 5V$ , disabled to $V_{OUT} < 0.5V$	—	0.4	—	ms
$R_{DIS}$	Discharge Resistance	$V_{IN} = 5V$ , Disabled, $I_{OUT} = 1mA$	—	90	130	$\Omega$
$T_{SHDN}$	Thermal Shutdown Threshold	Enabled	—	+140	—	$^\circ C$
$T_{HYS}$	Thermal Shutdown Hysteresis	—	—	+35	—	$^\circ C$
$V_{RVP}$	Reverse-Voltage Comparator Trip Point	$V_{OUT} - V_{IN}$	25	50	75	mV
$I_{ROCP}$	Reverse Current Limit	$V_{OUT} - V_{IN} = 100mV$	—	400	—	mA
$t_{TRIG}$	Time from Reverse-Voltage Condition to MOSFET Turn off	$V_{IN}$	2	6	13	ms

## Performance Characteristics

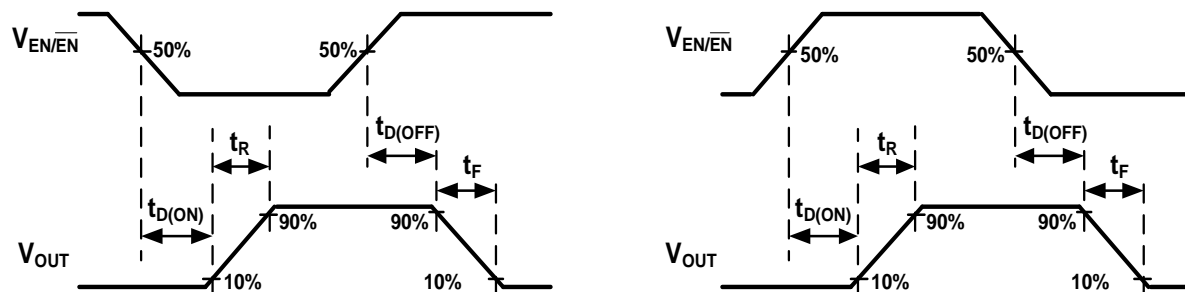
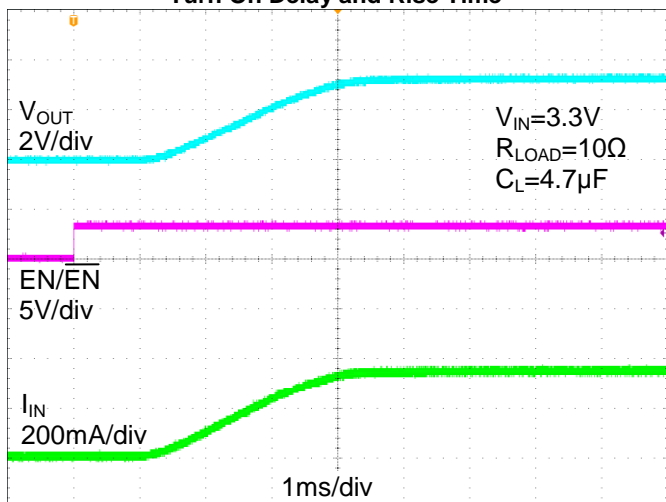


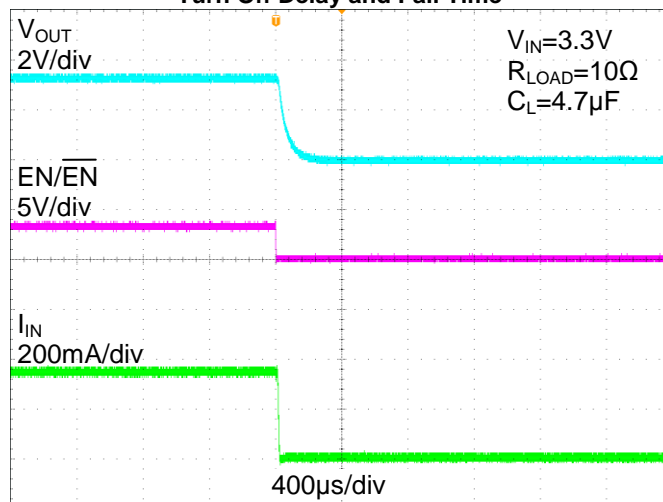
Figure 1. Voltage Waveforms: AP22811B (Active Low, Left), AP22811A (Active High, Right)

**Performance Characteristics** (Cont.) ( $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $C_{IN} = 1\mu\text{F}$ ,  $C_L = 0.1\mu\text{F}$ , unless otherwise specified.)

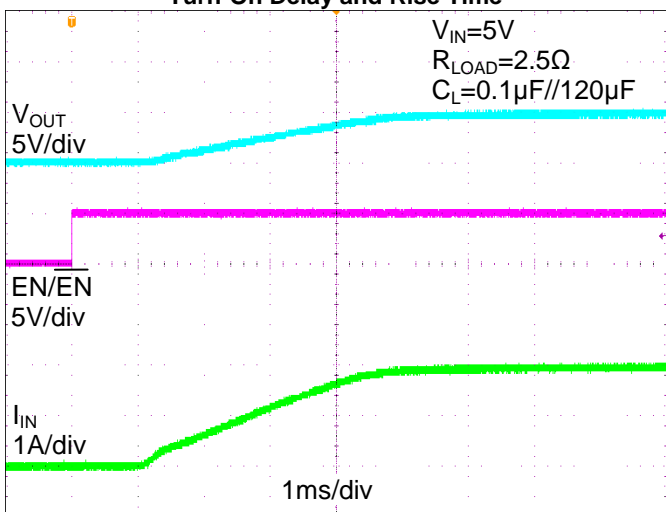
**Turn On Delay and Rise Time**



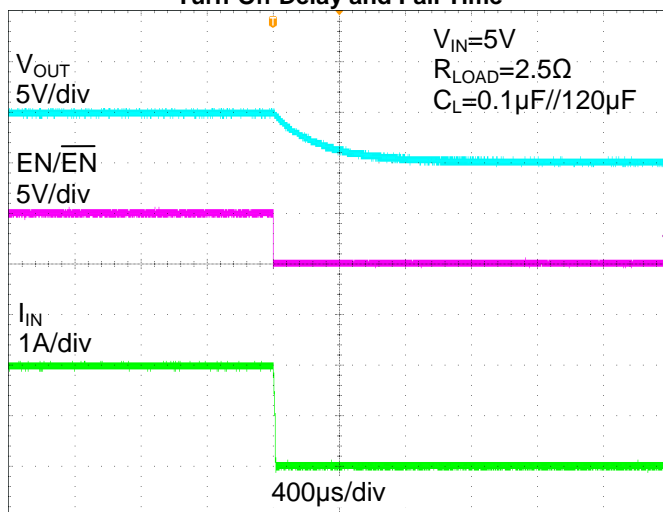
**Turn Off Delay and Fall Time**



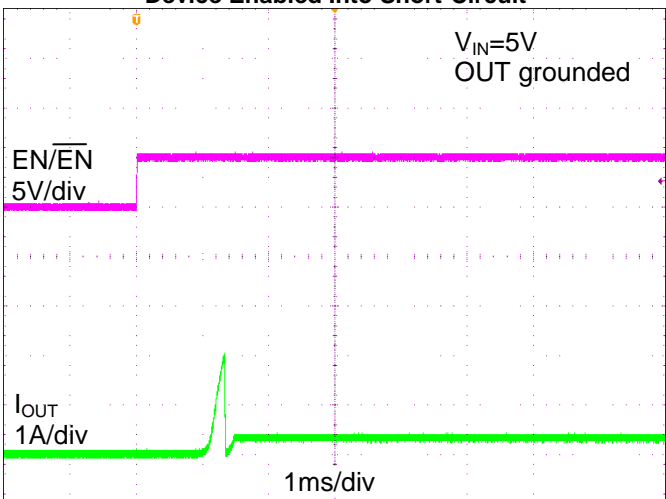
**Turn-On Delay and Rise Time**



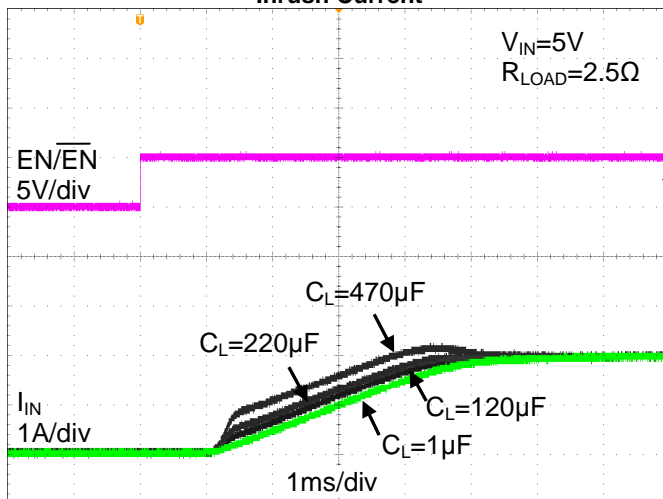
**Turn-Off Delay and Fall Time**



**Device Enabled Into Short-Circuit**

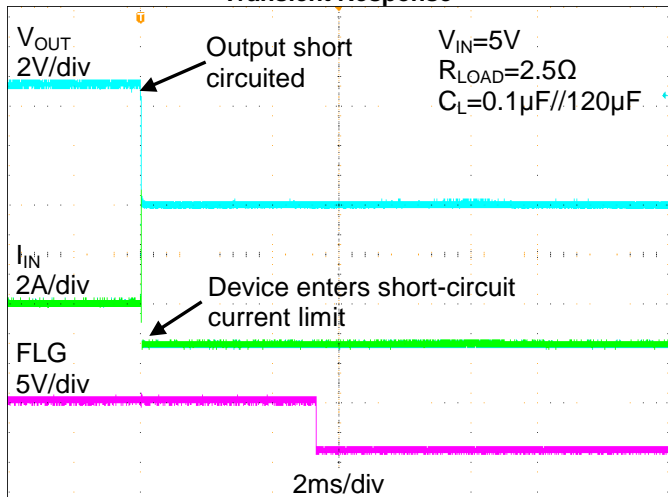


**Inrush Current**

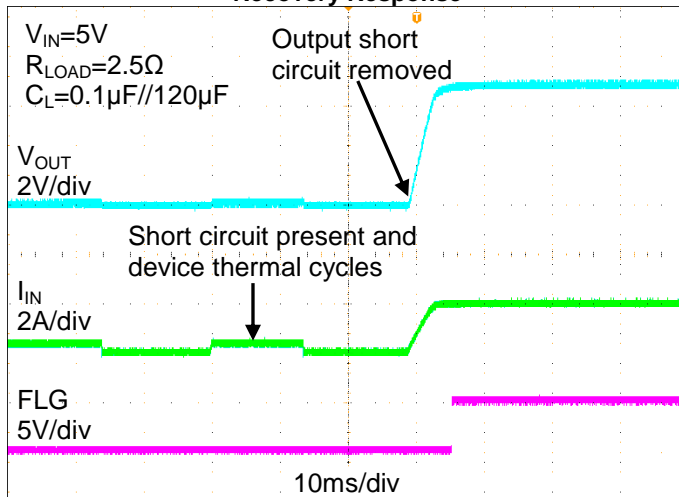


**Performance Characteristics** (Cont.) ( $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $C_{IN} = 1\mu\text{F}$ ,  $C_L = 0.1\mu\text{F}$ , unless otherwise specified.)

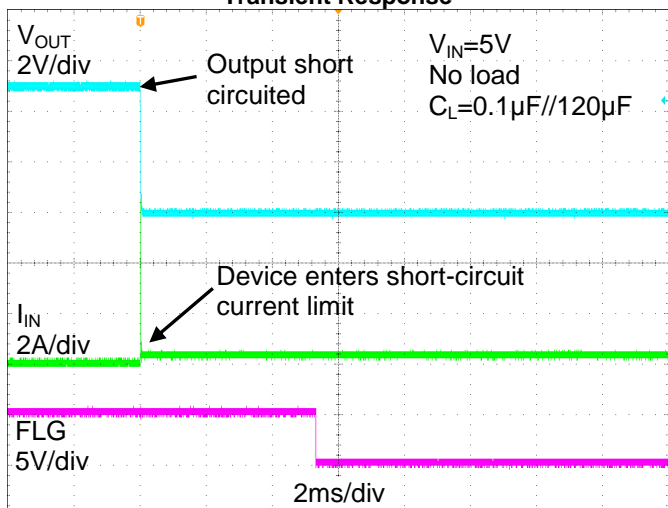
**Full-Load to Short-Circuit  
Transient Response**



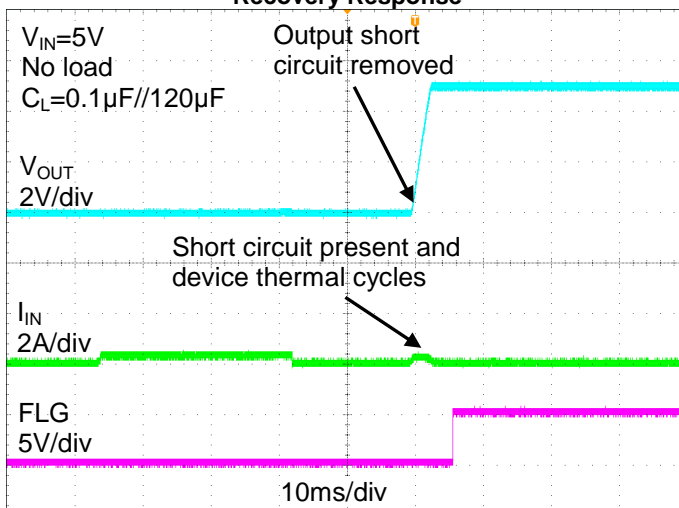
**Short-Circuit to Full-Load  
Recovery Response**



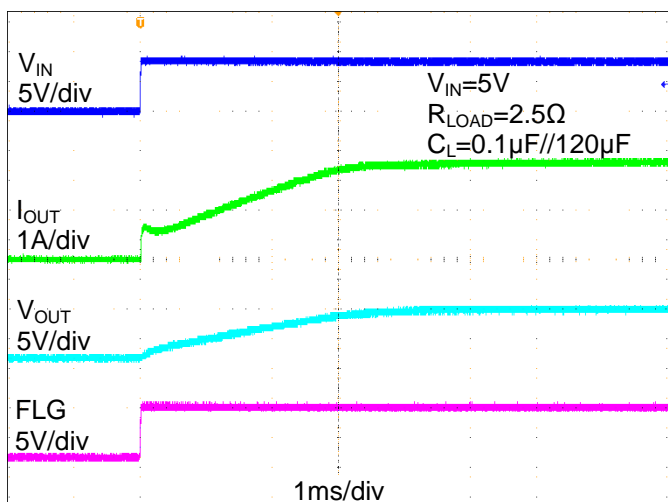
**No-Load to Short-Circuit  
Transient Response**



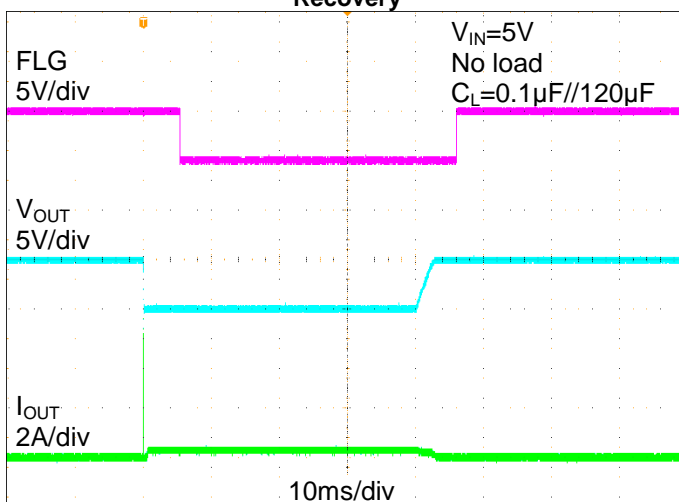
**Short-Circuit to No-Load  
Recovery Response**



**Power ON**

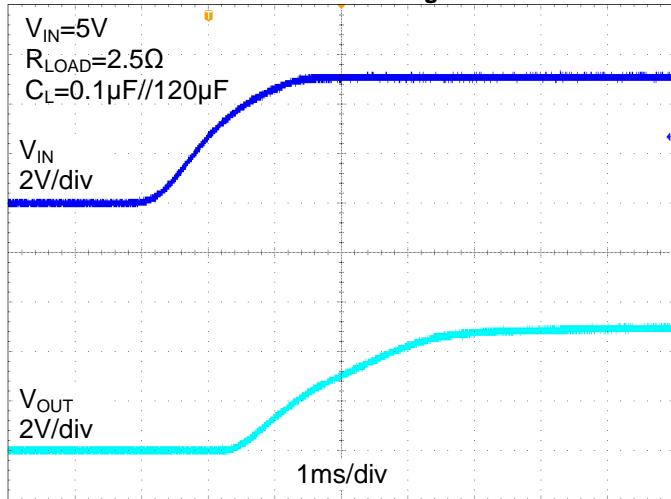


**Short-Circuit with Blanking Time and  
Recovery**

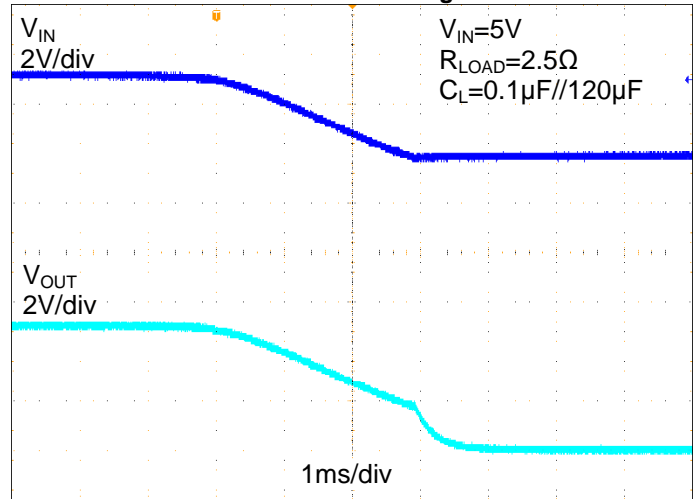


**Performance Characteristics** (Cont.) ( $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $C_{IN} = 1\mu\text{F}$ ,  $C_L = 0.1\mu\text{F}$ , unless otherwise specified.)

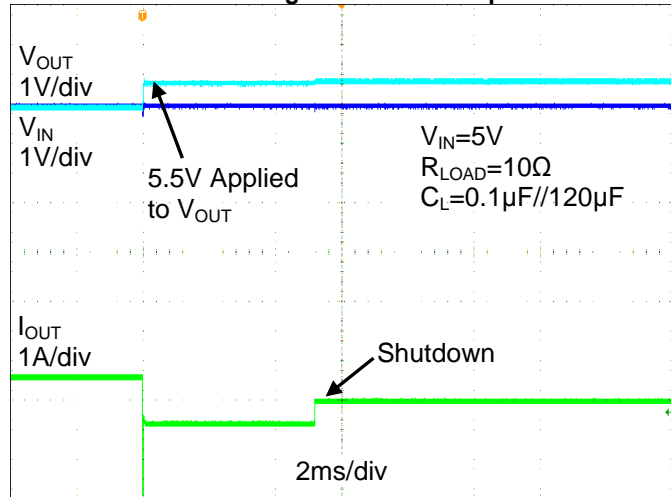
**UVLO Increasing**



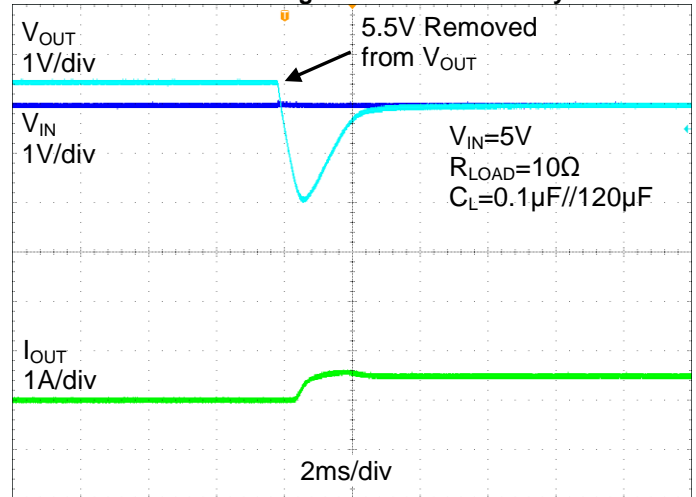
**UVLO Decreasing**



**Reverse-Voltage Protection Response**

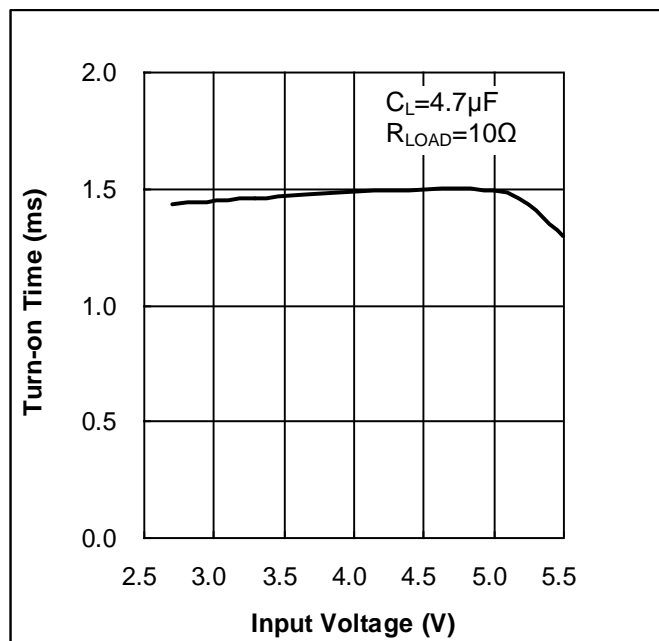


**Reverse-Voltage Protection Recovery**

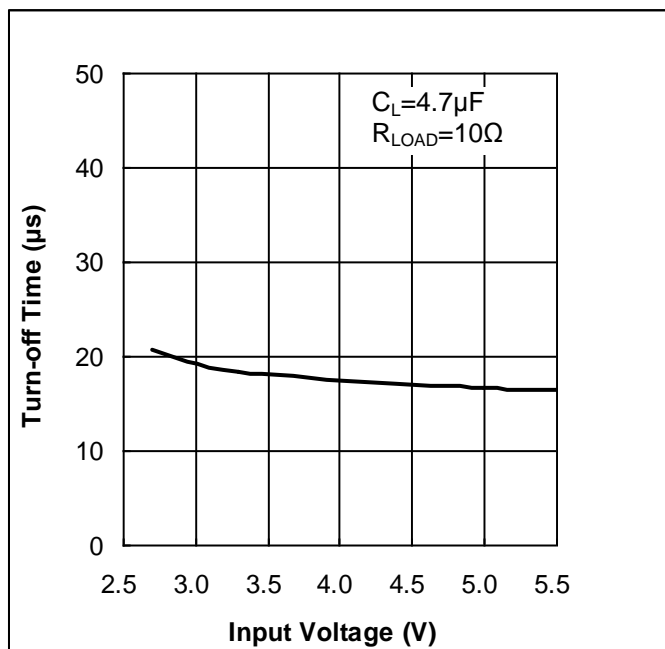


**Performance Characteristics** (Cont.) ( $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $C_{IN} = 1\mu\text{F}$ ,  $C_L = 0.1\mu\text{F}$ , unless otherwise specified.)

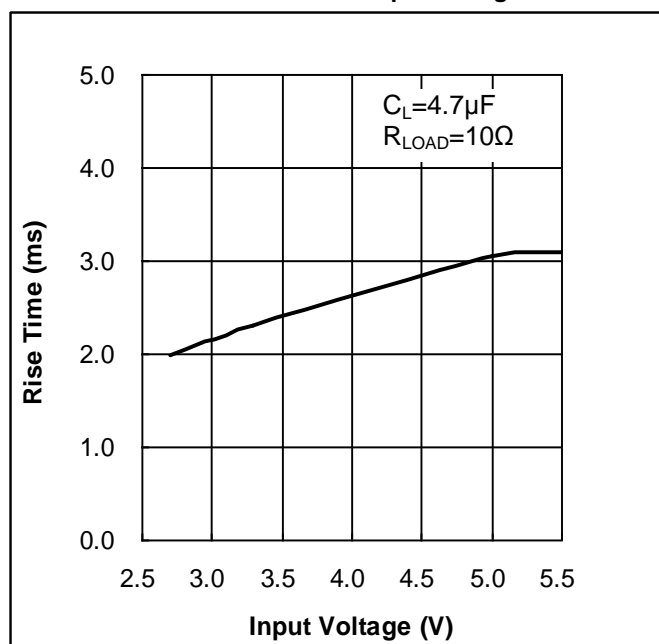
**Turn-on Time vs. Input Voltage**



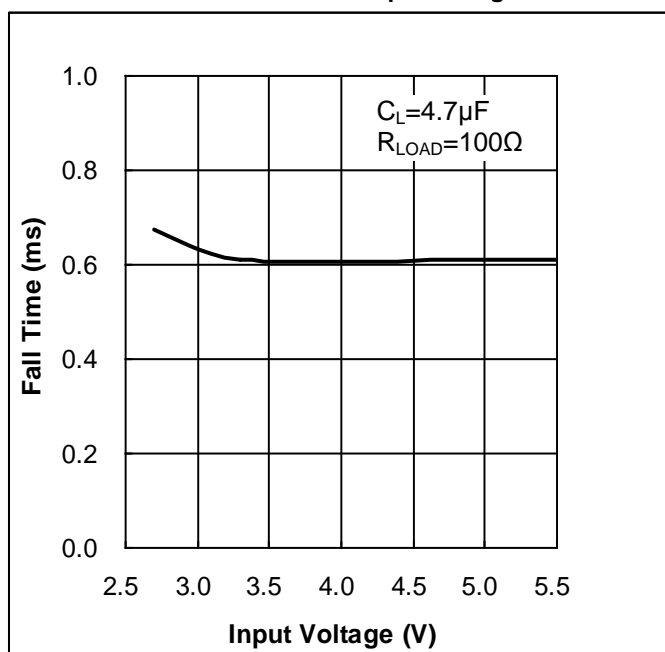
**Turn-off Time vs. Input Voltage**



**Rise Time vs. Input Voltage**



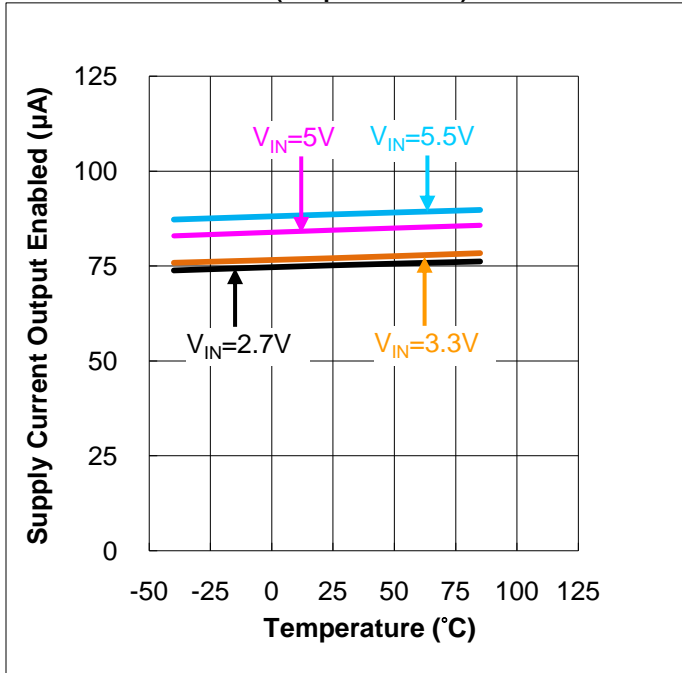
**Fall Time vs. Input Voltage**



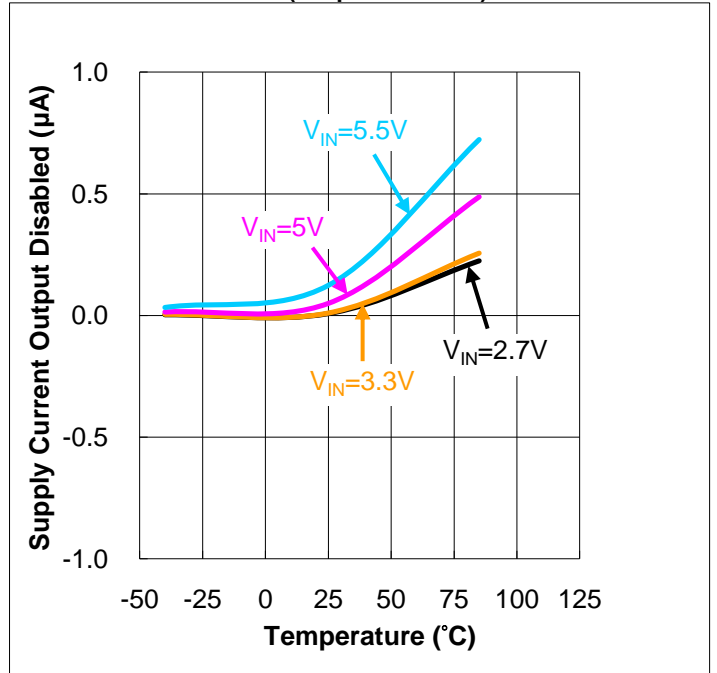


**Performance Characteristics** (Cont.) ( $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $C_{IN} = 1\mu\text{F}$ ,  $C_L = 0.1\mu\text{F}$ , unless otherwise specified.)

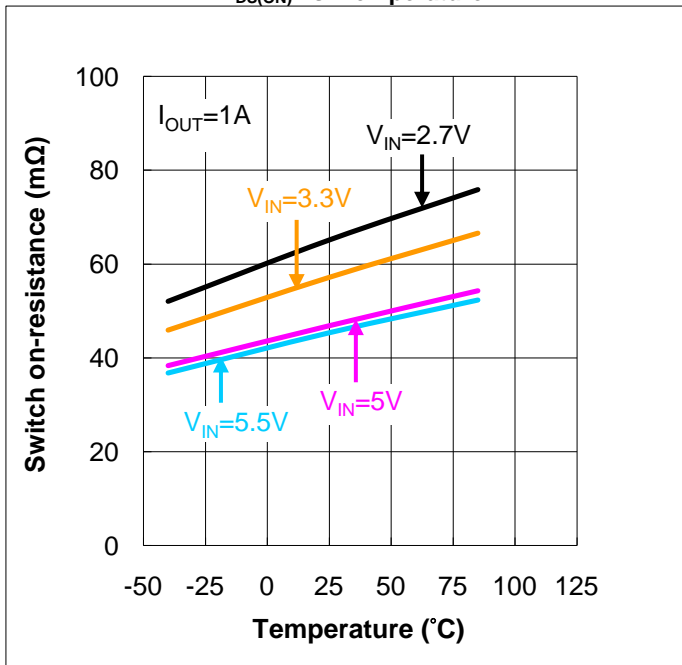
**Supply Current vs. Temperature  
(Output Enabled)**



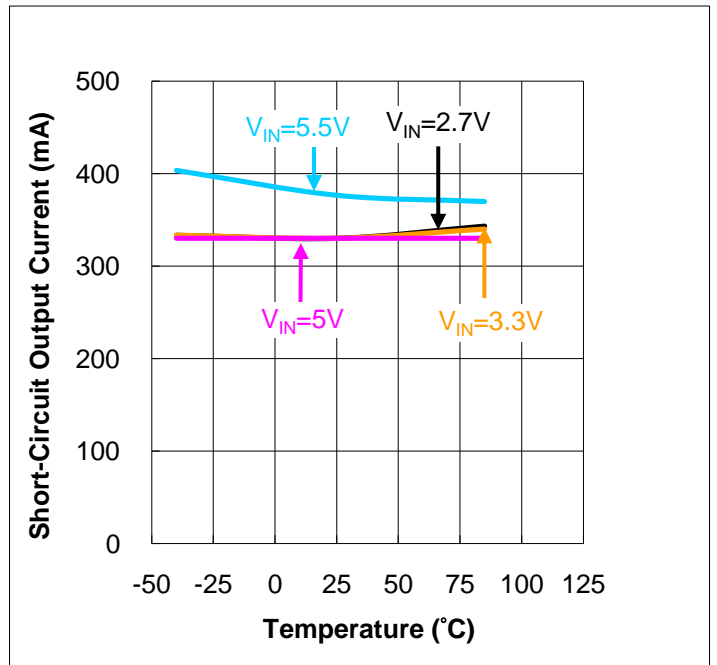
**Supply Current vs. Temperature  
(Output Disabled)**



**$R_{DS(ON)}$  vs. Temperature**

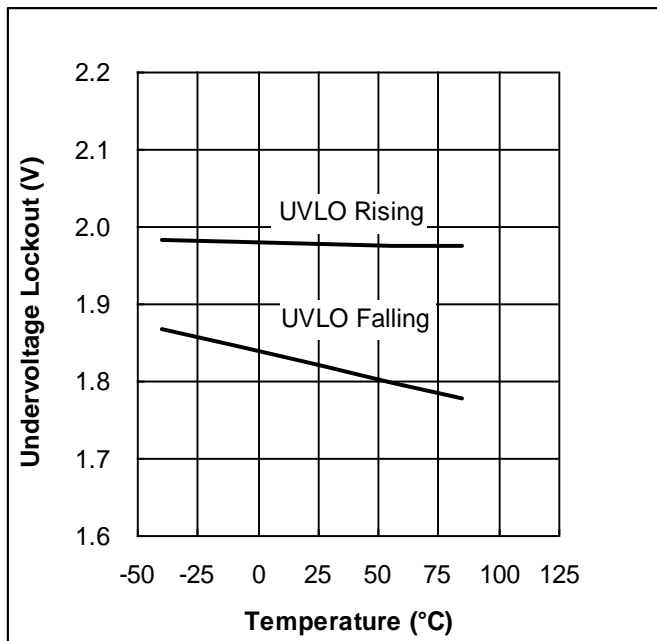


**Short-Circuit Output Current vs. Temperature**

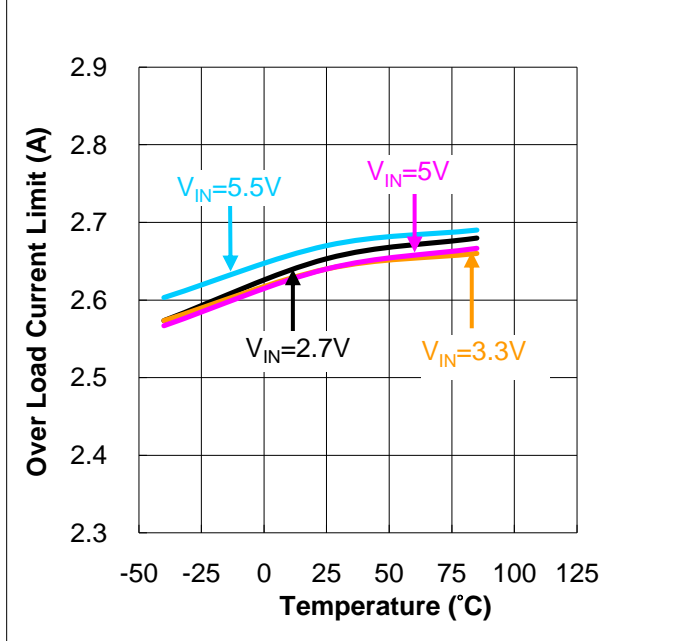


**Performance Characteristics** (Cont.) ( $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $C_{IN} = 1\mu\text{F}$ ,  $C_L = 0.1\mu\text{F}$ , unless otherwise specified.)

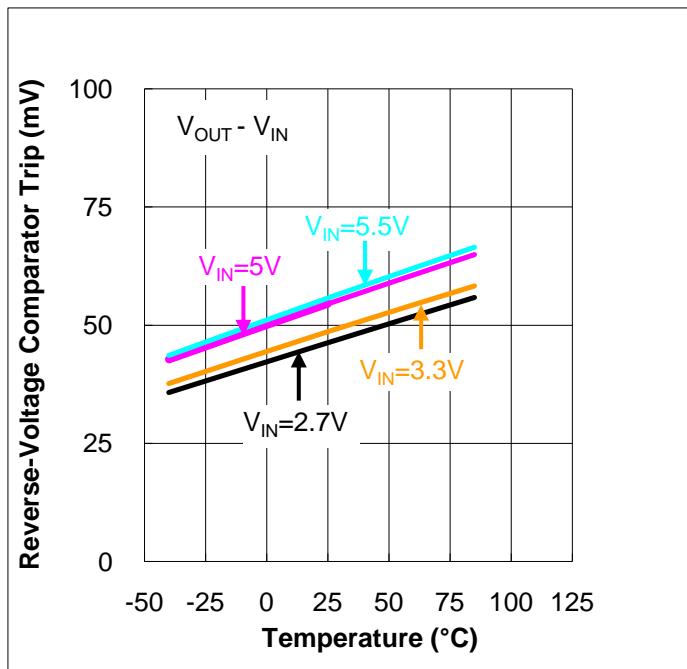
**Under Voltage Lockout vs. Temperature**



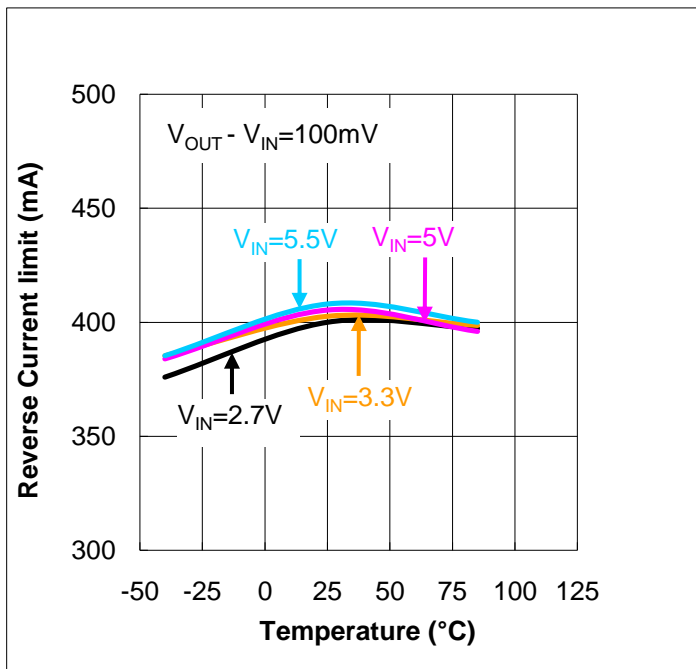
**Over Load Current Limit vs. Temperature**



**Reverse-Voltage Comparator Trip vs. Temperature**



**Reverse Current Limit vs. Temperature**



## Application Information

### Input and Output Capacitors

It is needed to place a 1 $\mu$ F X7R or X5R ceramic bypass capacitor between IN and GND, close to the device. Placing a high-value capacitor (10 $\mu$ F or 47 $\mu$ F) close to input pin is also recommended when the output transient load is heavy. This precaution reduces power-supply transients that may cause ringing on the input.

Connect a minimum 100 $\mu$ F low ESR electrolytic or tantalum capacitor (or 10 $\mu$ F MLCC) between OUT and GND is also needed for hot-plug applications. It's a must to bypass the output with a 0.1 $\mu$ F ceramic capacitor which improves the immunity of the device to short-circuit transients. The Bulky 100 $\mu$ F or larger capacitors help to reduce output droop voltage when a device is plugged in. When abnormal short-circuit condition happens, these capacitors can also reduce output negative voltage due to parasitic inductive effect and avoid device damage.

Please note without the bypass capacitors, an output short may cause ringing on the input; if the voltage is over the maximum voltage rating, it will destroy the internal control circuitry even the duration is short.

### FLG Response

When an over-current or over-temperature shutdown condition is encountered, the FLG open-drain output goes active low after a nominal 6ms deglitch timeout. The FLG output remains low until both over-current and over-temperature conditions are removed. Connecting a heavy capacitive load to the output of the device can cause a momentary over-current condition, which does not trigger the FLG due to the 6ms deglitch timeout. The AP22811 is designed to eliminate false over-current reporting without the need of external components to remove unwanted pulses.

However, It is to be noted that, when the FLG pin is not supplied via the same  $V_{IN}$  voltage source of the AP22811 but other external power source, it is strongly required that the AP22811 must be sure to reach a stable operating voltage condition before the other power source applied to FLG pin.

### Over-Current and Short Circuit Protection

An internal sensing FET is employed to check for over-current conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault stays long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted to GND before the device is enabled or before  $V_{IN}$  has been applied. The AP22811 senses the short circuit and immediately clamps output current to a certain safe level.

In the second condition, an output short or an overload occurs while the device is enabled. At the instance the overload occurs, higher current may flow for a very short period of time before the current limit function can react. After the current limit function has tripped, the device switches into current limiting mode and the current is clamped at  $I_{LIMIT}$ , or  $I_{SHORT}$ .

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold ( $I_{TRIG}$ ) is reached or until the thermal limit of the device is exceeded. The AP22811 is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its current limiting mode and is set at  $I_{LIMIT}$ .

### Thermal Protection

Thermal protection prevents the IC from damage when heavy-overload or short-circuit faults are present for extended periods of time. The AP22811 implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. Once the die temperature rises to approximately +140°C due to excessive power dissipation in an over-current or short-circuit condition the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit allowing the device to cool down approximately +35°C before the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The FLG open-drain output is asserted when an over-temperature shutdown or over-current occurs with 6ms deglitch.

### ON/OFF Input Operator

The EN/ $\overline{EN}$  input allows the output current to be switched on and off using a GPIO compatible input. The high signal (switch on) should be at least 1.5V, and the low signal (switch off) no higher than 0.65V. This pin should NOT be left floating. It is advisable to hold the EN/ $\overline{EN}$  signal low when applying or removing power.

## Application Information (Cont.)

### Under-voltage Lockout (UVLO)

Under-voltage lockout function (UVLO) keeps the internal power switch from being turned on until the power supply has reached at least 2V, even if the switch is enabled. Whenever the input voltage falls below approximately 2V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed.

### Discharge Function

The discharge function of the device is active when enable is disabled or de-asserted. The discharge function with the N-MOS power switch implementation is activated and offers a resistive discharge path for the external storage capacitor. This is designed for discharging any residue of the output voltage when either no external output resistance or load resistance is present at the output.

### Output Reverse-Voltage/ Current Protection

The output reverse-voltage protection turns off the MOSFET switch whenever the output voltage is higher than the input voltage by 50mV for 6ms and the MOSFET switch will turn on when output reverse-voltage/current conditions is removed.

### Power Dissipation and Junction Temperature

The low on-resistance of the internal MOSFET allows the small surface-mount packages to pass large current. Using the maximum operating ambient temperature ( $T_A$ ) and  $R_{DS(ON)}$ , the power dissipation can be calculated by:

$$P_D = R_{DS(ON)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

$T_A$  = Ambient temperature °C

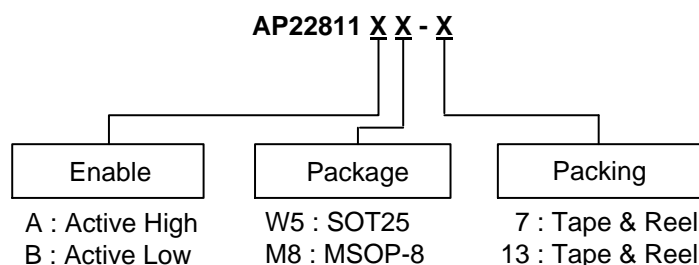
$R_{\theta JA}$  = Thermal resistance

$P_D$  = Total power dissipation

### Board Layout Instruction

Placing input and output capacitors, 1μF and 0.1μF+100μF respectively, close and next to the device pins must be implemented to minimize the effects of parasitic inductance. For best performance, all trace lengths should be kept as short as possible. The input and output PCB traces should be as wide as possible. Use a ground plane to enhance the power dissipation capability of the device.

## Ordering Information

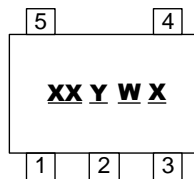


Part Number	Package Code	Packaging	7" and 13" Tape and Reel	
			Quantity	Part Number Suffix
AP22811AW5-7	W5	SOT25	3000/Tape & Reel	-7
AP22811BW5-7	W5	SOT25	3000/Tape & Reel	-7
AP22811AM8-13	M8	MSOP-8	2500/Tape & Reel	-13
AP22811BM8-13	M8	MSOP-8	2500/ Tape & Reel	-13

## Marking Information

### (1) SOT25

( Top View )

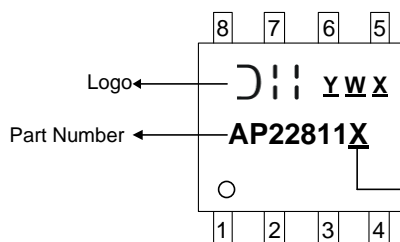


XX : Identification code  
 Y : Year 0~9  
 W : Week : A~Z : 1~26 week;  
 a~z : 27~52 week; z represents  
 52 and 53 week  
 X : Internal Code

Part Number	Package Type	Identification Code
AP22811AW5-7	SOT25	5Y
AP22811BW5-7	SOT25	5Z

### (2) MSOP-8

( Top view )

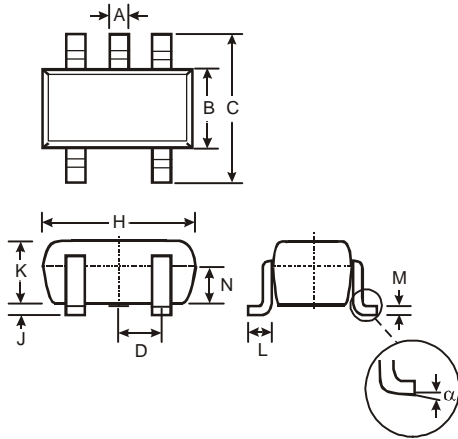


Y : Year : 0~9  
 W : Week : A~Z : 1~26 week;  
 a~z : 27~52 week; z represents  
 52 and 53 week  
 X : Internal Code  
 A : Active High  
 B : Active Low

## Package Outline Dimensions

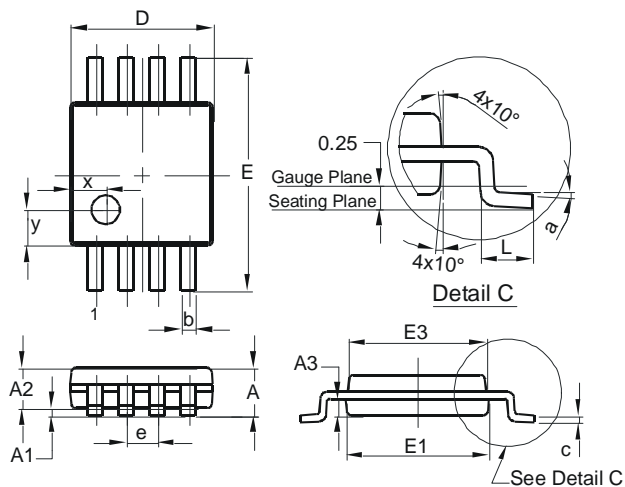
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

### (1) SOT25



SOT25			
Dim	Min	Max	Typ
A	0.35	0.50	0.38
B	1.50	1.70	1.60
C	2.70	3.00	2.80
D	—	—	0.95
H	2.90	3.10	3.00
J	0.013	0.10	0.05
K	1.00	1.30	1.10
L	0.35	0.55	0.40
M	0.10	0.20	0.15
N	0.70	0.80	0.75
α	0°	8°	—
All Dimensions in mm			

### (2) MSOP-8

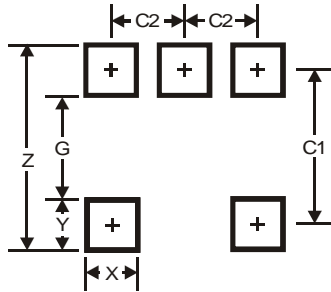


MSOP-8			
Dim	Min	Max	Typ
A	-	1.10	-
A1	0.05	0.15	0.10
A2	0.75	0.95	0.86
A3	0.29	0.49	0.39
b	0.22	0.38	0.30
c	0.08	0.23	0.15
D	2.90	3.10	3.00
E	4.70	5.10	4.90
E1	2.90	3.10	3.00
E3	2.85	3.05	2.95
e	-	-	0.65
L	0.40	0.80	0.60
a	0°	8°	4°
x	-	-	0.750
y	-	-	0.750
All Dimensions in mm			

## Suggested Pad Layout

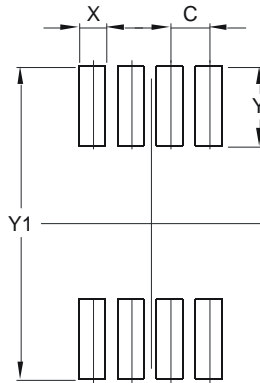
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

### (1) SOT25



Dimensions	Value (in mm)
Z	3.20
G	1.60
X	0.55
Y	0.80
C1	2.40
C2	0.95

### (2) MSOP-8



Dimensions	Value (in mm)
C	0.650
X	0.450
Y	1.350
Y1	5.300

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