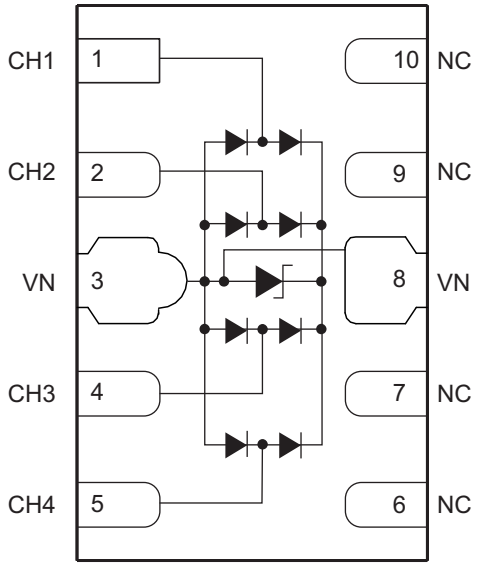
Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ8829DI-05	-40 °C to +85 °C	2.5 mm x 1.0 mm x 0.55 mm DFN-10	Green Product

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



DFN-10
(Top View)

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Storage Temperature (T_S)	-65 °C to +150 °C
ESD Rating per IEC61000-4-2, contact[1][3]	±30 kV
ESD Rating per IEC61000-4-2, air[1][3]	±30 kV
ESD Rating per Human Body Model[2][3]	±30 kV

Notes:

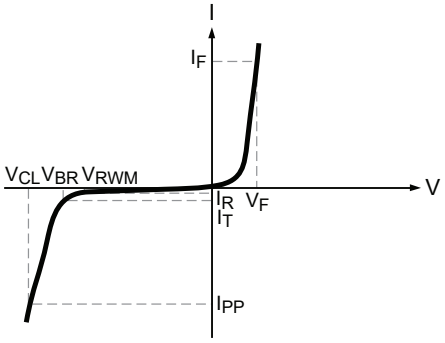
1. IEC 61000-4-2 discharge with $C_{Discharge}$ = 150pF, $R_{Discharge}$ = 330 Ω.
2. Human Body Discharge per MIL-STD-883, Method 3015 $C_{Discharge}$ = 100 pF, $R_{Discharge}$ = 1.5 kΩ.

Maximum Operating Ratings

Parameter	Rating
Junction Temperature (T_J)	-40 °C to +125 °C

Electrical Characteristics

T_A = 25°C unless otherwise specified.

Symbol	Parameter	Diagram
I_{PP}	Maximum Reverse Peak Pulse Current	
V_{CL}	Clamping Voltage @ I_{PP} 100ns Transmission Line Pulse (TLP)	
V_{RWM}	Working Peak Reverse Voltage	
I_R	Maximum Reverse Leakage Current	
V_{BR}	Breakdown Voltage	
I_T	Test Current	
V_F	Forward Voltage @ I_F	
C_J	Max. Capacitance @ V_R = 0 and f = 1 MHz	

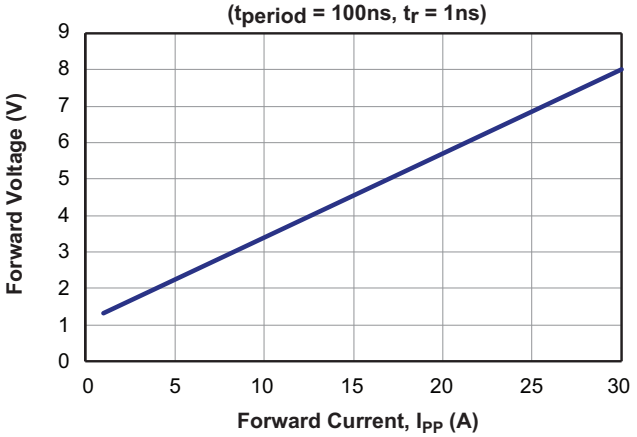
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{RWM}	Reverse Working Voltage	I/O pin to ground			5	V
V_{BR}	Reverse Breakdown Voltage	I_T = 100 µA, I/O pin-to-ground	6			V
I_R	Reverse Leakage Current	Max. VRWM, I/O pin-to-ground			0.1	µA
V_{CL}	Clamping Voltage[3] (100 ns Transmission Line Pulse, I/O Pin-to-Ground)	I_{TLP} = 2 A I_{TLP} = -2 A			3 -2.5	V V
		I_{TLP} = 12 A I_{TLP} = -12 A			6.5 -4.0	V V
	Clamping Voltage[3] (IEC61000-4-5, 8/20 µs, I/O Pin-to-Ground)	I_{PP} = 6 A I_{PP} = -8 A			7.5 -8.5	V V
R_{DNY}	Dynamic Resistance[3]	I_{TLP} = 1 A to 16 A I_{TLP} = -1 A to -16 A		0.35 0.15		Ω Ω
C_J	Junction Capacitance	$V_{PIN\ 3,8}$ = 0 V, $V_{I/O}$ = 0 V, f = 1 MHz, I/O pin-to-ground		0.6		pF
		$V_{PIN\ 3,8}$ = 0 V, $V_{I/O}$ = 0 V, f = 1 MHz, I/O pin-to-I/O pin		0.25		pF

Notes:

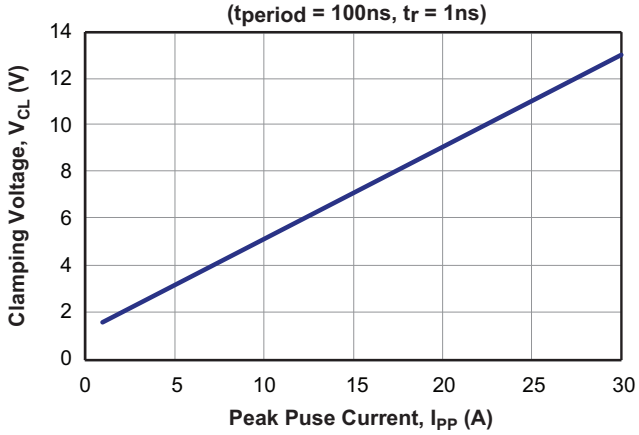
3. These specifications are guaranteed by design and characterization.

Typical Performance Characteristics

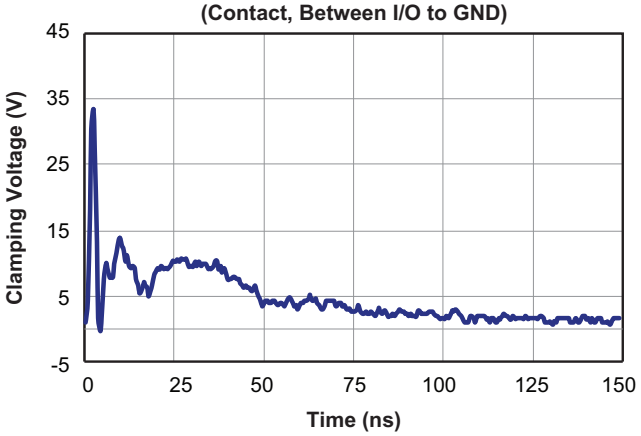
Forward Voltage vs. Forward Peak Pulse Current
(t_{period} = 100ns, t_r = 1ns)



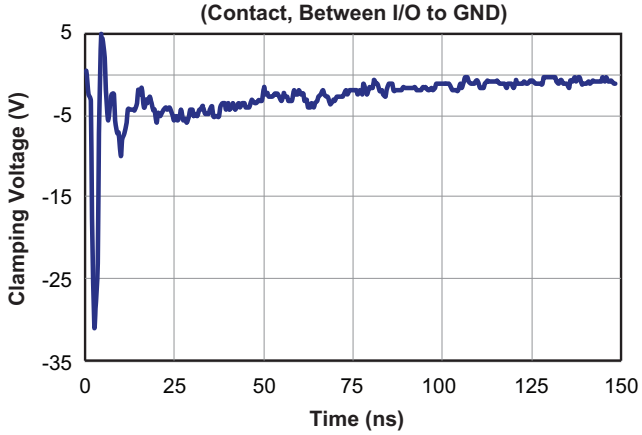
Clamping Voltage vs. Peak Pulse Current
(t_{period} = 100ns, t_r = 1ns)



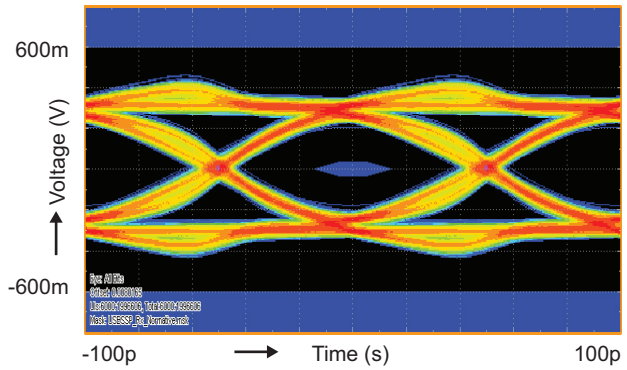
+8kV ESD Clamping Per IEC 61000-4-2
(Contact, Between I/O to GND)



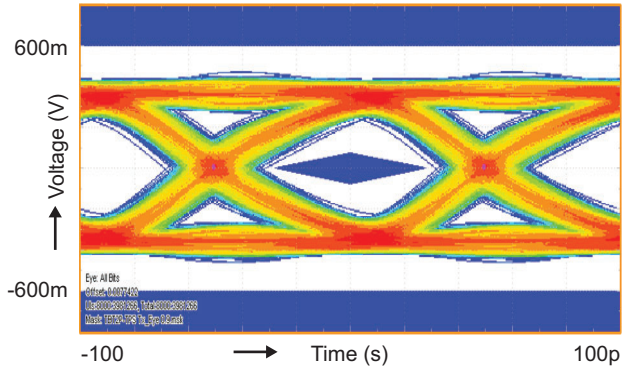
-8kV ESD Clamping Per IEC 61000-4-2
(Contact, Between I/O to GND)



USB 3.1 Eye Diagram with AOZ8829 (10Gbps)



Thunderbolt 2.0 Eye Diagram with AOZ8829 (10Gbps)



High Speed PCB Layout Guidelines

Printed circuit board layout is the key to achieving the highest level of surge immunity on power and data lines. The location of the protection devices on the PCB is the simplest and most important design rule to follow. The AOZ8829DI-05 devices should be located as close as possible to the noise source. The AOZ8829DI-05 device should be placed on all data and power lines that enter or exit the PCB at the I/O connector. In most systems, surge pulses occur on data and power lines that enter the PCB through the I/O connector. Placing the AOZ8829DI-05 devices as close as possible to the noise source ensures that a surge voltage will be clamped before the pulse can be coupled into adjacent PCB traces. In addition, the PCB should use the shortest possible traces. A short trace length equates to low impedance, which ensures that the surge energy will be dissipated by the AOZ8829DI-05 device. Long signal traces will act as antennas to receive energy from fields that are produced by the ESD pulse. By keeping line lengths as short as possible, the efficiency of the line to act as an antenna for ESD related fields is reduced. Minimize interconnecting line lengths by placing devices with the most interconnect as close together as possible. The protection circuits should shunt the surge voltage to either the reference or chassis ground. Shunting the surge voltage directly to the IC's signal ground can cause ground bounce. The clamping performance of TVS diodes on a single ground PCB can be improved by minimizing the impedance with relatively short and wide ground traces. The PCB layout and IC package parasitic inductances can cause significant overshoot to the TVS's clamping voltage. The inductance of the PCB can be reduced by using short trace lengths and multiple layers with separate ground and power planes. One effective method to minimize loop problems is to incorporate a ground plane in the PCB design.

The AOZ8829DI-05 ultra-low capacitance TVS is designed to protect four high speed data transmission lines from transient over-voltages by clamping them to a fixed reference. The low inductance and construction minimizes voltage overshoot during high current surges. When the voltage on the protected line exceeds the reference voltage the internal steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. The AOZ8829DI-05 is designed for ease of PCB layout by allowing the traces to run underneath the device. The pin out of the AOZ8829DI-05 is designed to simply drop onto the IO lines of a High Definition Multimedia Interface (HDMI 1.4/2.0) or USB 3.1 design without having to divert the signal lines that may add more parasitic inductance. Pins 1, 2, 4 and 5 are connected to the internal TVS devices and pins 6, 7, 9 and 10 are no connects. The no connects was done so the package can be securely soldered onto the PCB surface.

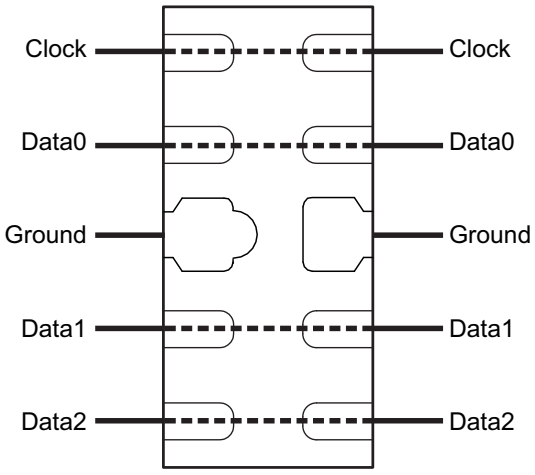


Figure 3. Flow Through Layout for HDMI 1.4/2.0

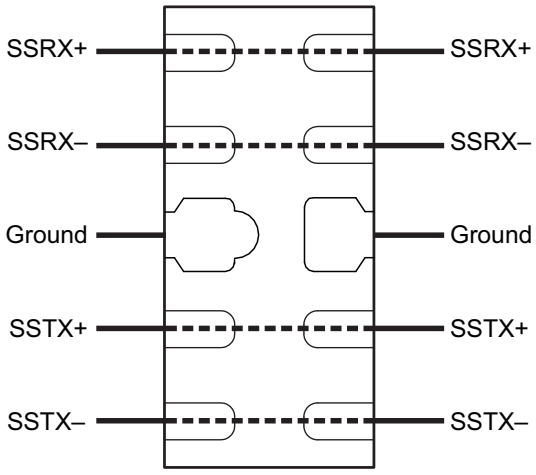


Figure 4. Flow Through Layout for USB 3.1

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.