TABLE OF CONTENTS

REVISION HISTORY

4/07—Rev. B to Rev. C

Updated Format ..... Universal
Changes to Figure 1, Figure 2 1
Deleted Pin Function Descriptions Section and Pin Configurations Section 2
Changes to Figure 20 and Figure 21 9
Updated Outline Dimensions 10

10/04—Rev. A to Rev. B

Changes to Pin Configurations ..... Universal
Changes to Ordering Guide 2
Changes to Outline Dimensions 7

6/03—Rev. 0 to Rev. A

Added SC70 package ..... Universal
Changes to Features 1
Changes to General Description 1
Changes to Specifications 2
Changes to Ordering Guide 2
Changes to TPCs 4, 6, and 7 3
Updated SOT-23 Outline Dimensions 7

11/02—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{IN} = 2.55 V to 5.5 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
Output Voltage	V_{OUT}	2.4 V < V_{IN} < 5.5 V, 0 µA < I_{OUT} < 10 µA, –40°C < T_A < +85°C	1.195	1.200	1.205	V
Temperature Coefficient	TCV_O	0°C < T_A < 50°C		5	20	ppm/°C
		–40°C < T_A < +85°C		10	40	ppm/°C
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	2.55 V < V_{IN} < 5.5 V, no load		2	12	ppm/V
Supply Current	I_{IN}	2.4 V < V_{IN} < 5.5 V, no load		10	16	µA
Ground Current	I_{GND}	V– grounded, I_{LOAD} = 10 µA		12	20	µA
Input Voltage Range	V_{IN}		2.4		5.5	V
Operating Temperature Range	T_A		–40		+85	°C
Nominal Load Capacitance	C_{OUT}		1			µF
Output Noise Voltage	V_N rms	f = 10 Hz to 10 kHz		12.5		µV rms
Voltage Noise Density	e_N	f = 400 kHz		12.5		nV/√Hz
Power Supply Ripple Rejection[2]	PSRR	I_{LOAD} = 10 µA		–80		dB
Start-Up Time	t_{ON}			2		ms

[1] Typical values represent average readings taken at room temperature.
[2] Power supply ripple rejection measurement applies to a changing input voltage (V_{IN}) waveform with a nominal 3.6 V baseline that drops to a 3 V value for 380 µs at a 4.6 ms repetition rate.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
Supply Voltage	6 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 60 Sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for a device soldered in circuit board for surface-mount packages.

Table 3.

Package Type	θ_{JA}	θ_{JC}	Unit
SOT-23	230	146	°C/W
SC70	376	102	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

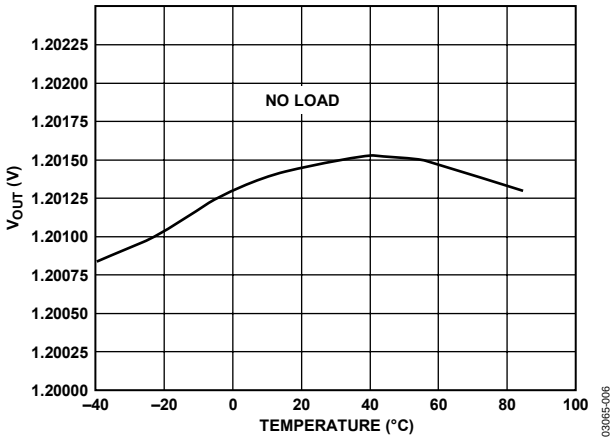

Figure 4. V_{OUT} vs. Temperature

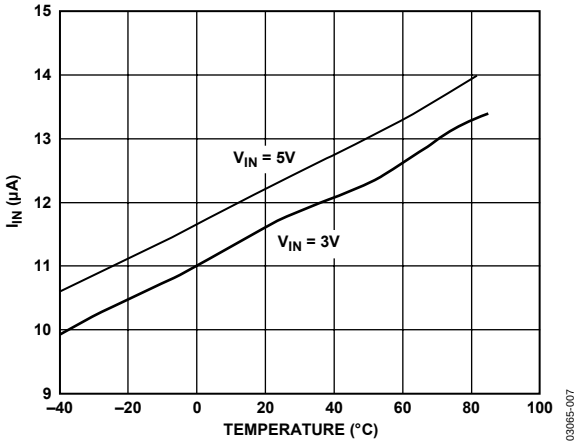

Figure 5. Supply Current vs. Temperature

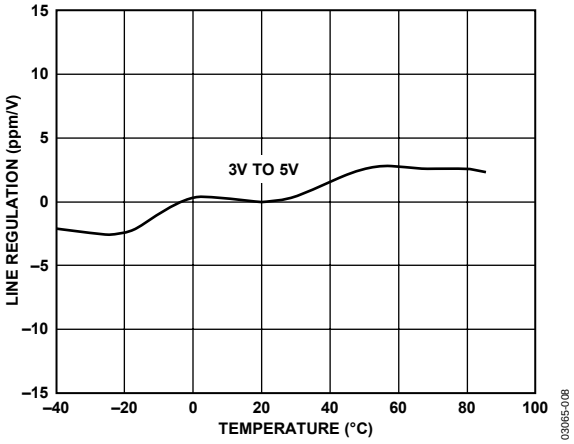

Figure 6. Line Regulation vs. Temperature

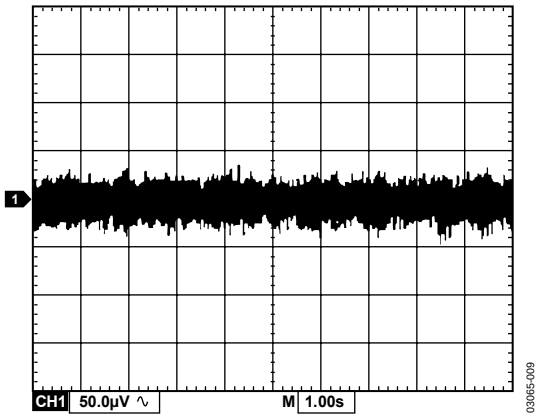

Figure 7. Noise Voltage Peak-to-Peak, 10 Hz to 10 kHz

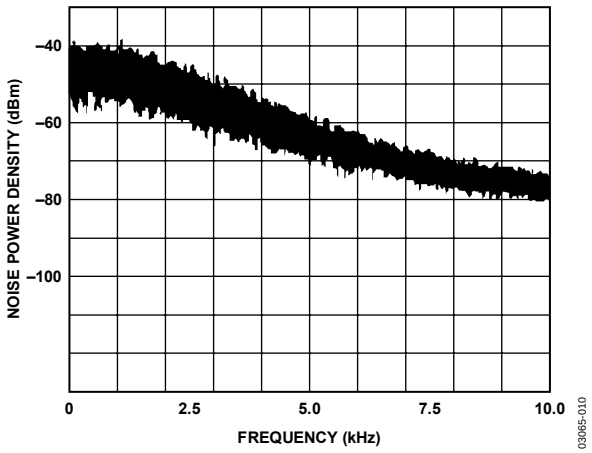

Figure 8. Output Noise Density Plot (V_+ = 3.6 V, C_{OUT} = 1 µF, C_{IN} = 1 µF)

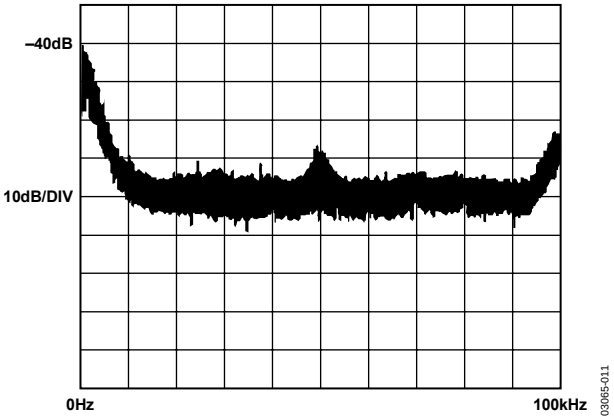

Figure 9. Voltage Noise Density, 0 Hz to 100 kHz

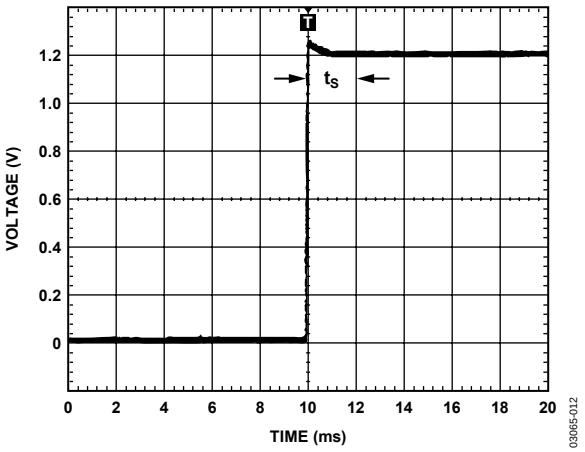

Figure 10. Settling Time

THEORY OF OPERATION

The ADR280 provides the basic core 1.2 V band gap reference. It contains two NPN transistors, Q9 and Q17, with their emitter areas scaled in a fixed ratio. The difference in the V_{BE} produces a proportional to absolute temperature (PTAT) voltage that cancels the complementary to absolute temperature (CTAT) Q9 V_{BE} voltage. As a result, a core band gap voltage that is almost a constant 1.2 V over temperature is generated (see Figure 11). Precision laser trimming of the internal resistors and other proprietary circuit techniques are used to enhance the initial accuracy, temperature curvature, and temperature drift performance.

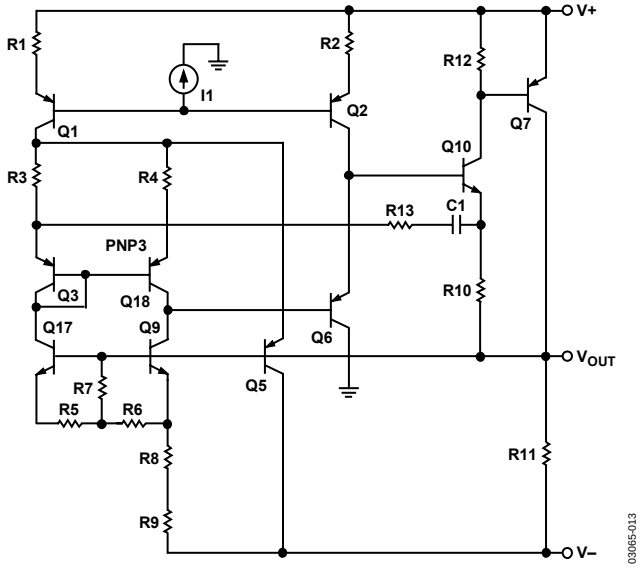

Figure 11. Simplified Architecture

APPLICATIONS INFORMATION

The ADR280 should be decoupled with a 0.1 µF ceramic capacitor at the output for optimum stability. It is also good practice to include 0.1 µF ceramic capacitors at the IC supply pin. These capacitors should be mounted close to their respective pins (see Figure 12).

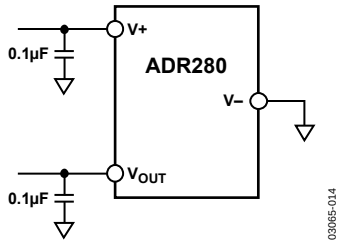

Figure 12. Basic Configuration

The low supply voltage input pin V– can be elevated above ground; a 1.2 V differential voltage can therefore be established above V– (see Figure 13).

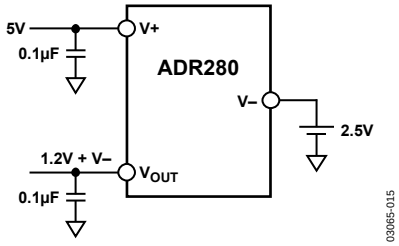

Figure 13. Floating References

The ADR280 provides the core 1.2 V band gap voltage and is able to drive a maximum load of only 100 µA. Users can simply buffer the output for high current or sink/source current applications, such as ADC or LCD driver references (see Figure 14).

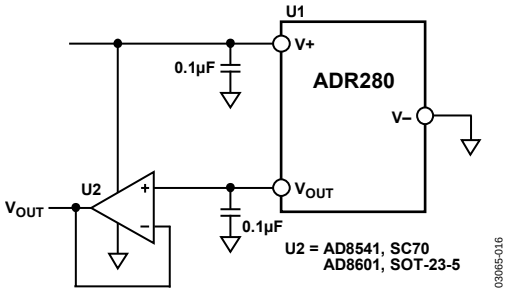

Figure 14. Buffered Output

Users can also tailor any specific need for voltage and dynamics with an external op amp and discrete components (see Figure 14 and Figure 15). Depending on the specific op amp and PCB layout, it may be necessary to add a compensation capacitor, C2, to prevent gain peaking and oscillation. The exact value of C2 needed requires some trial and error but usually falls in the range of a few picofarads.

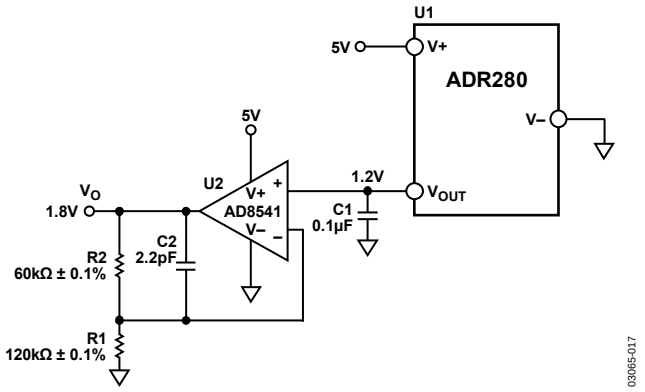

Figure 15. 1.8 V Reference

LOW COST, LOW POWER CURRENT SOURCE

Because of its low power characteristics, the ADR280 can be converted to a current source with just a setting resistor. In addition to the ADR280 current capability, the supply voltage and the load limit the maximum current. The circuit in Figure 16 produces 100 µA with 2 V compliance at a 5 V supply. The load current is the sum of I_{SET} and I_{GND}. I_{GND} increases slightly with load; a R_{SET} of 13.6 kΩ yields 100 µA of load current.

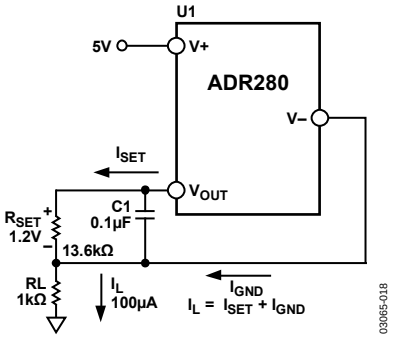

Figure 16. Low Cost Current Source

Precision Low Power Current Source

By adding a buffer to redirect the I_{GND} in Figure 17, a current can be precisely set by R_{SET} with the equation $I_L = 1.2\ V/R_{SET}$.

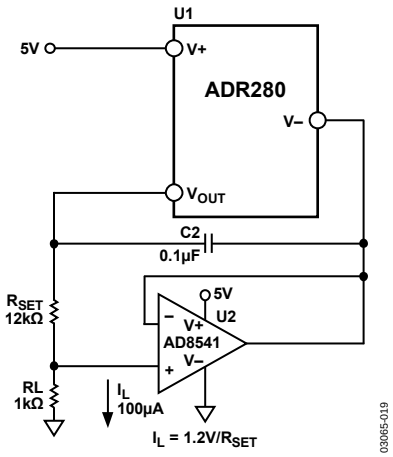

Figure 17. Precision Low Power Current Source

Boosted Current Source

Adding one more buffer to the previous circuit boosts the current to the level that is limited only by the buffer U2 current handling capability (see Figure 18).

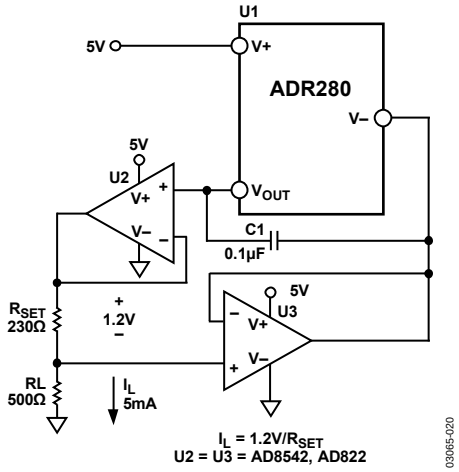

Figure 18. Precision Current Source

Negative Reference

A negative reference can be precisely configured without using any expensive tight tolerance resistors, as shown in Figure 19. The voltage difference between V_{OUT} and V– is 1.2 V. Since V_{OUT} is at virtual ground, U2 closes the loop by forcing the V– pin to be the negative reference output.

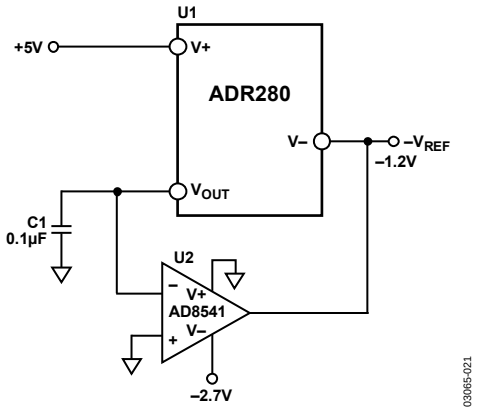

Figure 19. Negative Reference

Boosted Reference with Scalable Output

A precision user defined output with boosted current capability can be implemented with the circuit shown in Figure 20. In this circuit, U2 forces V_O to be equal to $V_{REF} \times (1 + R2/R1)$ by regulating the turn-on of M1; the load current is therefore furnished by the 5 V supply. For higher output voltage, U2 must be changed and the supply voltage of M1 and U2 must also be elevated and separated from the U1 input voltage. In this configuration, a 100 mA load is achievable at a 5 V supply. The higher the supply voltage, the lower the current handling is because of the heat generated on the MOSFET. For heavy capacitive loads, additional buffering is needed at the output to enhance the transient response.

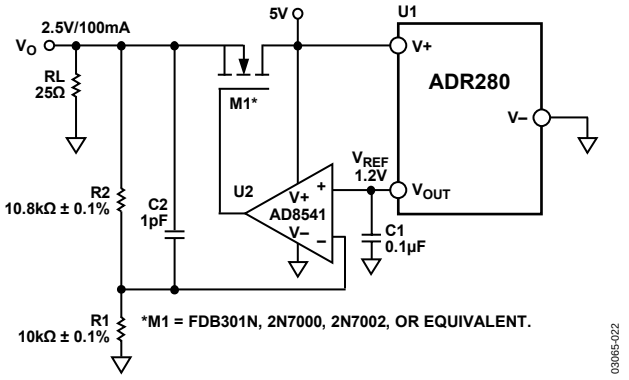

Figure 20. 2.5 V Boosted Reference

GSM and 3G Mobile Station Applications

The ADR280 voltage reference is ideal for use with analog baseband ICs in GSM and 3G mobile station applications. Figure 21 illustrates the use of the ADR280 with the AD6535 GSM analog baseband. The AD6535 provides all of the data converters and power management functions needed to implement a GSM mobile station, including baseband codecs, audio codecs, voltage regulators, and a battery charger. Besides low current consumption and a small footprint, the ADR280 is optimized for excellent PSRR, which is necessary for optimum AD6535 device performance when the main battery voltage fluctuates during RF power amplifier activity.

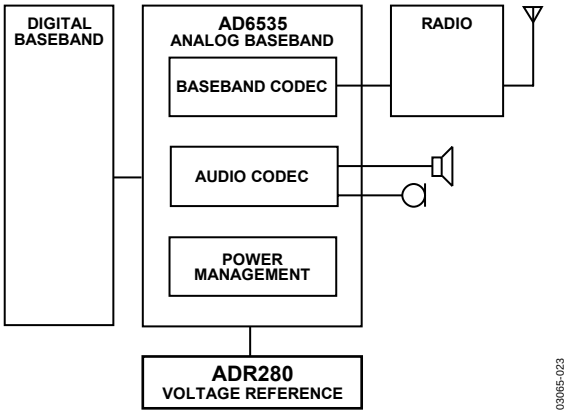

Figure 21. GSM Mobile Station Application

OUTLINE DIMENSIONS

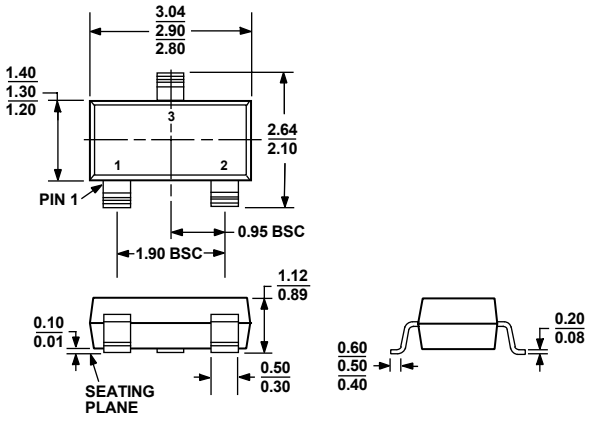

Figure 22. 3-Lead Small Outline Transistor Package [SOT-23-3]
(RT-3)
Dimensions shown in millimeters

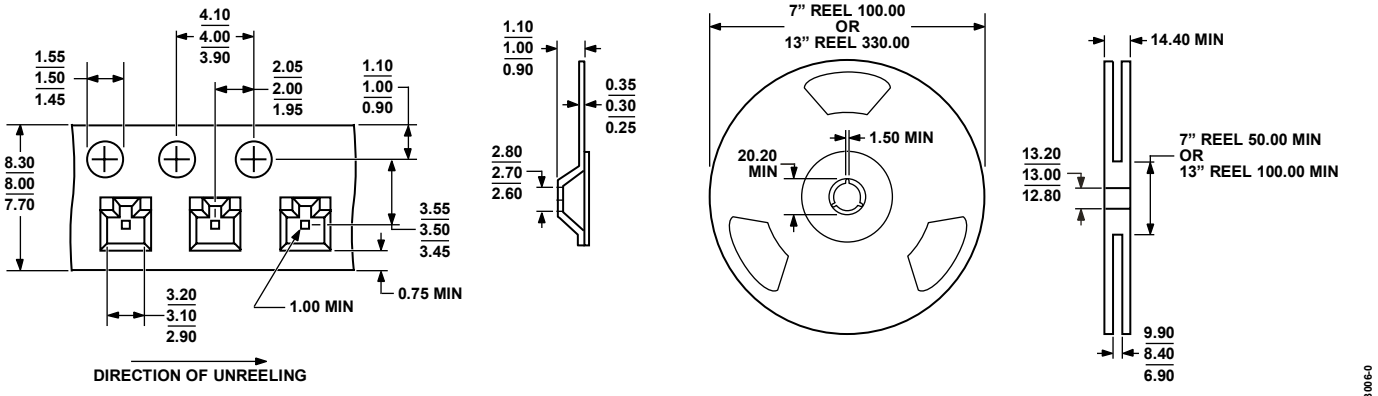

Figure 23. Tape and Reel Dimensions
(RT-3)
Dimensions shown in millimeters

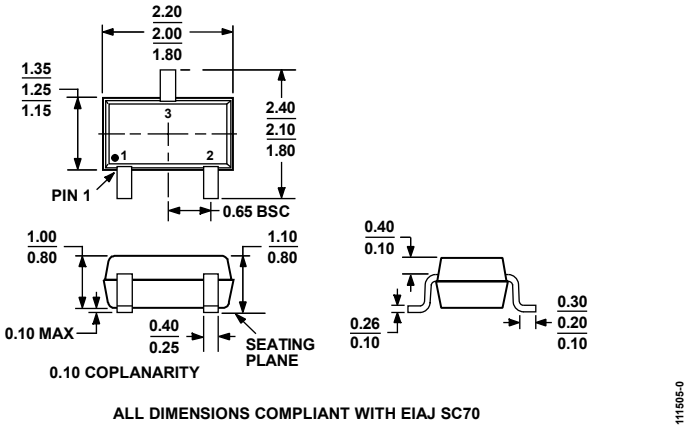

Figure 24. 3-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding	Output Voltage (V)	Ordering Quantity
ADR280AKS-R2	−40°C to +85°C	3-Lead SC70	KS-3	RBA	1.200	250
ADR280AKS-REEL	−40°C to +85°C	3-Lead SC70	KS-3	RBA	1.200	10,000
ADR280AKS-REEL7	−40°C to +85°C	3-Lead SC70	KS-3	RBA	1.200	3,000
ADR280AKSZ-R2[1]	−40°C to +85°C	3-Lead SC70	KS-3	L25	1.200	250
ADR280AKSZ-REEL7[1]	−40°C to +85°C	3-Lead SC70	KS-3	L25	1.200	3,000
ADR280ART-R2	−40°C to +85°C	3-Lead SOT-23	RT-3	RBA	1.200	250
ADR280ART-REEL	−40°C to +85°C	3-Lead SOT-23	RT-3	RBA	1.200	10,000
ADR280ART-REEL7	−40°C to +85°C	3-Lead SOT-23	RT-3	RBA	1.200	3,000
ADR280ARTZ-R2[1]	−40°C to +85°C	3-Lead SOT-23	RT-3	L25	1.200	250
ADR280ARTZ-REEL7[1]	−40°C to +85°C	3-Lead SOT-23	RT-3	L25	1.200	3,000

[1] Z = RoHS Compliant Part.

NOTES

C03065-0-4/07(C)