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REVISION HISTORY

8/2019—Rev. B to Rev. C

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4/2019—Rev. A to Rev. B

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Updated Outline Dimensions ... 24

12/2013—Rev. 0 to Rev. A

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11/2012—Revision 0: Initial Version

SPECIFICATIONS

V_S = 3.3 V, V_{CM} = 1.65 V, V_S = 5 V, V_{CM} = 2.5 V, R_L = 200 Ω differential, A_V = 16 dB, C_L = 1 pF differential, f = 100 MHz, T_A = 25°C, parameters specified as ac-coupled differential input and differential output, unless otherwise noted.

Table 1.

Parameter	Test Conditions/ Comments	3.3 V Min	3.3 V Typ	3.3 V Max	5 V Min	5 V Typ	5 V Max	Unit
DYNAMIC PERFORMANCE								
−3 dB Bandwidth	A_V = 16 dB, V_{OUT} ≤ 0.5 V p-p		4500			4500		MHz
Bandwidth 0.1 dB Flatness	V_{OUT} ≤ 1.0 V p-p		500			500		MHz
Gain Accuracy			±1			±1		dB
Gain Error	≤1000 MHz, Channel A to Channel B		≤0.02			≤0.02		dB
Phase Error	≤1000 MHz, Channel A to Channel B		≤0.5			≤0.5		Degrees
Gain Supply Sensitivity	V_S ± 5%		3.4			5.6		mdB/V
Gain Temperature Sensitivity	−40°C to +85°C		0.5			0.5		mdB/°C
Slew Rate	Rise, A_V = 16 dB, R_L = 200 Ω, V_{OUT} = 2 V step		16			18		V/ns
	Fall, A_V = 16 dB, R_L = 200 Ω, V_{OUT} = 2 V step		18			20		V/ns
Settling Time	2 V step to 1%		890			750		ps
Overdrive Recovery Time	V_{IN} = 4 V to 0 V step, V_{OUT} ≤ ±10 mV		2.5			2.5		ns
Reverse Isolation (S12)			75			75		dB
Channel Isolation	Channel A to Channel B A_V = 16 dB		82.5			82.5		dB
INPUT/OUTPUT CHARACTERISTICS								
Input Common-Mode Range		1.2		1.8	1.3		3.5	V
Input Resistance (Differential)	A_V = 16 dB		160			160		Ω
Input Resistance (Single-Ended)	A_V = 14 dB		150			150		Ω
Input Capacitance (Single-Ended)			1.1			1.1		pF
Input Bias Current			±5			±5		µA
CMRR			44			44		dB
Output Common-Mode Range		1.25		1.8	1.25		3	V
Output Common-Mode Offset	Referenced to VCC/2	−100		+20	−100		+20	mV
Output Common-Mode Drift	−40°C to +85°C		2			3.5		mV/°C
Output Differential Offset Voltage		−20		+20	−20		+20	mV
Output Differential Offset Drift	−40°C to +85°C		1.1			1.7		mV/°C
Output Resistance (Differential)			11			11		Ω
Maximum Output Voltage Swing	1 dB compressed		3.4			5		V p-p
POWER INTERFACE								
Supply Voltage		2.8	3.3	5.2	2.8	5	5.2	V
ENBL1/ENBL2 Threshold	Device disabled, ENBL low			0.5			0.6	V
	Device enabled, ENBL high	1.5			1.5			V
ENBL1/ENBL2 Input Bias Current	ENBL high		500			500		nA
	ENBL low		−165			−165		µA
Quiescent Current	ENBL high		140	150		160	175	mA
	ENBL low		7			9		mA

Parameter	Test Conditions/ Comments	3.3 V Min	3.3 V Typ	3.3 V Max	5 V Min	5 V Typ	5 V Max	Unit
NOISE/HARMONIC PERFORMANCE								
10 MHz								
Second/Third Harmonic Distortion (HD2/HD3)	A_V = 16 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−99.1/−111			−103.1/−107.3		dBc
Output IP3/Third-Order Intermodulation Distortion (OIP3/IMD3)	A_V = 16 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+50.2/−103.3			+49.4/−101.8		dBm/dBc
Output IP2 Second-Order Intermodulation Distortion (OIP2/IMD2)	A_V = 16 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+90.8/−92.1			+91.2/−92.5		dBm/dBc
1 dB Compression Point, RTO (OP1dB)	A_V = 16 dB		14			17.7		dBm
Noise Spectral Density, RTI (NSD)	A_V = 16 dB		1.28			1.32		nV/√Hz
Noise Figure (NF)	A_V = 16 dB		6.47			6.66		dB
100 MHz								
Second/Third Harmonic Distortion (HD2/HD3)	A_V = 16 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−89/−92.1			−94.7/−100		dBc
Output IP3/Third-Order Intermodulation Distortion (OIP3/IMD3)	A_V = 16 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+49.4/−101.9			+50.9/−104.7		dBm/dBc
Output IP2 Second-Order Intermodulation Distortion (OIP2/IMD2)	A_V = 16 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+96.9/−98.2			+98.9/−100.2		dBm/dBc
1 dB Compression Point, RTO (OP1dB)	A_V = 16 dB		14.2			17.8		dBm
Noise Spectral Density, RTI (NSD)	A_V = 16 dB		1.26			1.3		nV/√Hz
Noise Figure (NF)	A_V = 16 dB		6.36			6.58		dB
200 MHz								
Second/Third Harmonic Distortion (HD2/HD3)	A_V = 16 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−92.7/−80.2			−94.5/−87.2		dBc
Output IP3/Third-Order Intermodulation Distortion (OIP3/IMD3)	A_V = 16 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+45.9/−94.7			+46/−95		dBm/dBc
Output IP2 Second-Order Intermodulation Distortion (OIP2/IMD2)	A_V = 16 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+80.4/−81.7			+82.6/−83.9		dBm/dBc
1 dB Compression Point, RTO (OP1dB)	A_V = 16 dB		14.1			17.7		dBm
Noise Spectral Density, RTI (NSD)	A_V = 16 dB		1.25			1.28		nV/√Hz
Noise Figure (NF)	A_V = 16 dB		6.31			6.48		dB
500 MHz								
Second/Third Harmonic Distortion (HD2/HD3)	A_V = 16 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−82.6/−60.5			−82.8/−64.2		dBc
Output IP3/Third-Order Intermodulation Distortion (OIP3/IMD3)	A_V = 16 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+30.7/−64.7			+32.4/−67.8		dBm/dBc
Output IP2 Second-Order Intermodulation Distortion (OIP2/IMD2)	A_V = 16 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+74.2/−75.5			+75.8/−77.1		dBm/dBc
Noise Spectral Density, RTI (NSD)	A_V = 16 dB		1.32			1.35		nV/√Hz
Noise Figure (NF)	A_V = 16 dB		6.64			6.83		dB

Parameter	Test Conditions/ Comments	3.3 V Min	3.3 V Typ	3.3 V Max	5 V Min	5 V Typ	5 V Max	Unit
1000 MHz								
Second/Third Harmonic Distortion (HD2/HD3)	A_V = 16 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−57.6/−43			−57.1/−45.9		dBc
Output IP3/Third-Order Intermodulation Distortion (OIP3/IMD3)	A_V = 16 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+23.2/−49.4			+24.8/−52.6		dBm/dBc
Output IP2 Second-Order Intermodulation Distortion (OIP2/IMD2)	A_V = 16 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+56.1/−57.4			+55.9/−57.2		dBm/dBc
Noise Spectral Density, RTI (NSD)	A_V = 16 dB		1.93			1.99		nV/√Hz
Noise Figure (NF)	A_V = 16 dB		9.45			9.66		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Output Voltage Swing × Bandwidth Product	2300 V p-p MHz
Supply Voltage, V_{CC}	5.25 V
VIPx, VINx	V_{CC} + 0.5 V
$\pm I_{OUT}$ Maximum	±30 mA
Internal Power Dissipation	900 mW
Maximum Junction Temperature	135°C
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 3 lists the junction to air thermal resistance (θ_{JA}) and the junction to paddle thermal resistance (θ_{JC}) for the ADL5566.

Table 3. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
24-Lead LFCSP	34.0	1.8	°C/W

[1] Measured on Analog Devices evaluation board. For more information about board layout, see the Soldering Information and Recommended Land Pattern section.
[2] Based on simulation with JEDEC standard JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

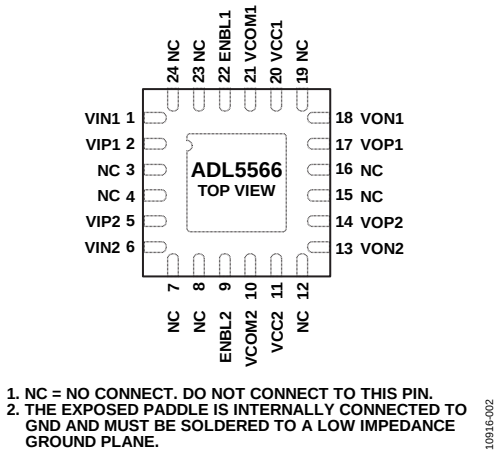


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIN1	Balanced Differential Input for Amplifier 1. Biased to $V_{CC}/2$, typically ac-coupled. Input for A_V = 16 dB.
2	VIP1	Balanced Differential Input for Amplifier 1. Biased to $V_{CC}/2$, typically ac-coupled. Input for A_V = 16 dB.
3, 4, 7, 8, 12, 15, 16, 19, 23, 24	NC	No Connect. Do not connect to this pin. Solder to ground.
5	VIP2	Balanced Differential Input for Amplifier 2. Biased to $V_{CC}/2$, typically ac-coupled. Input for A_V = 16 dB.
6	VIN2	Balanced Differential Input for Amplifier 2. Biased to $V_{CC}/2$, typically ac-coupled. Input for A_V = 16 dB.
9	ENBL2	Enable for Amplifier 2. Apply positive voltage (1.3 V < ENBL2 < VCC2) to activate device.
10	VCOM2	Common-Mode Voltage. A voltage applied to this pin sets the common-mode voltage of the inputs and outputs of Amplifier 2. If left open, VCOM2 = $V_{CC}/2$. Typically, it is decoupled to ground with a 0.1 µF capacitor.
11	VCC2	Positive Supply for Amplifier 2.
13	VON2	Balanced Differential Output for Amplifier 2. Biased to $V_{CC}/2$, typically ac-coupled.
14	VOP2	Balanced Differential Output for Amplifier 2. Biased to $V_{CC}/2$, typically ac-coupled.
17	VOP1	Balanced Differential Output for Amplifier 1. Biased to $V_{CC}/2$, typically ac-coupled.
18	VON1	Balanced Differential Output for Amplifier 1. Biased to $V_{CC}/2$, typically ac-coupled.
20	VCC1	Positive Supply for Amplifier 1.
21	VCOM1	Common-Mode Voltage. A voltage applied to this pin sets the common-mode voltage of the inputs and outputs of Amplifier 1. If left open, VCOM1 = $V_{CC}/2$. Typically, it is decoupled to ground with a 0.1 µF capacitor.
22	ENBL1	Enable for Amplifier 1. Apply positive voltage (1.3 V < ENBL1 < VCC1) to activate device.
	EP	The exposed paddle is internally connected to GND and must be soldered to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 3.3 V, V_{CM} = 1.65 V, R_L = 200 Ω differential, A_V = 16 dB, C_L = 1 pF differential, f = 100 MHz, T_A = 25°C, parameters specified as ac-coupled differential input and differential output, unless otherwise noted.

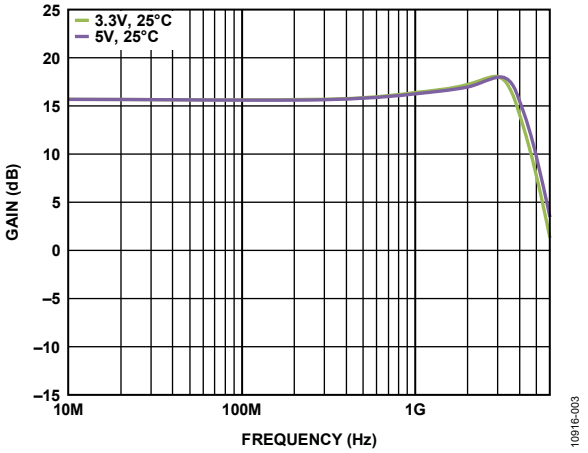


Figure 3. Gain vs. Frequency Response for 200 Ω Differential Load, V_{POS} = 3.3 V and V_{POS} = 5 V, 25°C

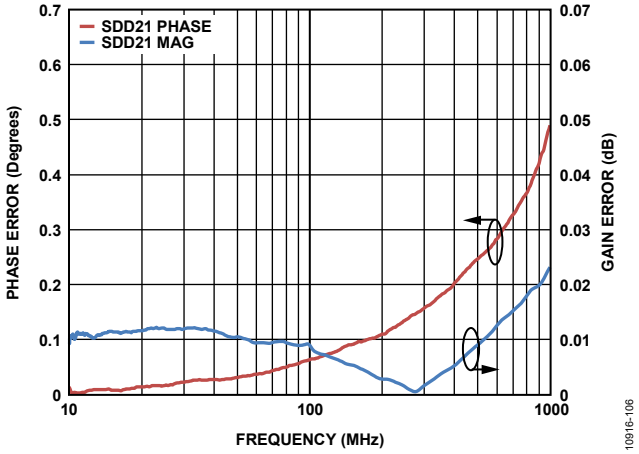


Figure 6. Channel-to-Channel Gain Error and Phase Error vs. Frequency

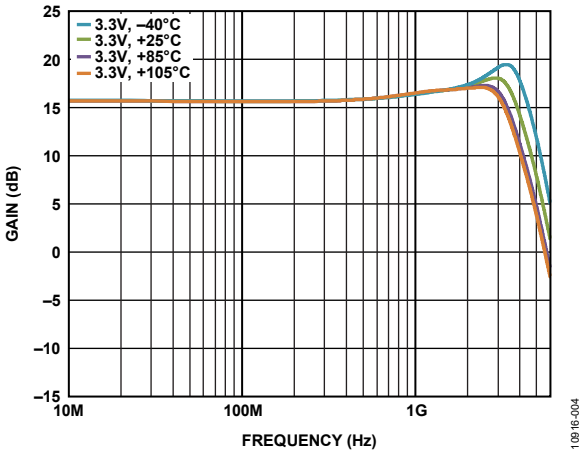


Figure 4. Gain vs. Frequency Response for 200 Ω Differential Load, Four Temperatures, V_{POS} = 3.3 V

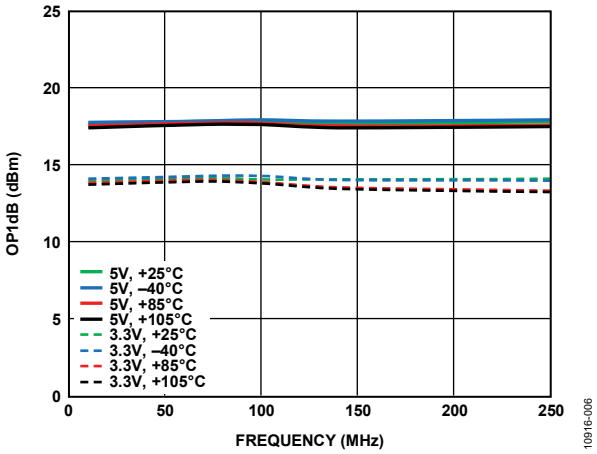


Figure 7. OP1dB vs. Frequency for 200 Ω Differential Load, Four Temperatures, V_{POS} = 3.3 V, V_{POS} = 5 V

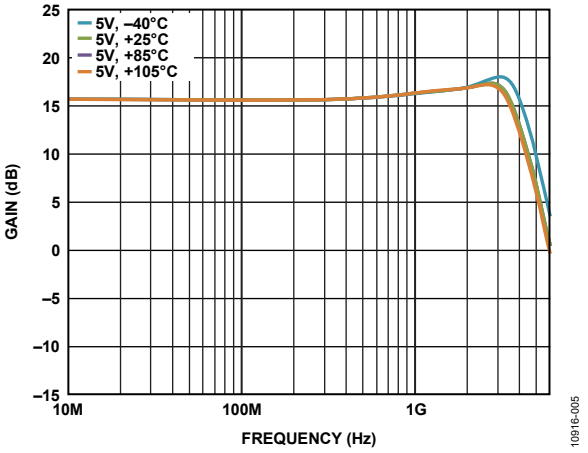


Figure 5. Gain vs. Frequency Response for 200 Ω Differential Load, Four Temperatures, V_{POS} = 5 V

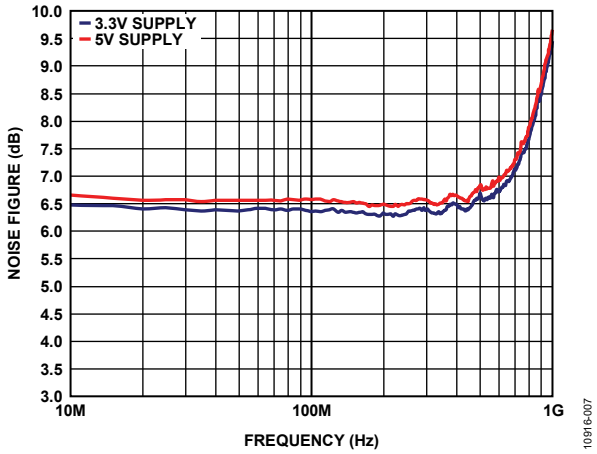


Figure 8. Noise Figure vs. Frequency at V_{POS} = 3.3 V, V_{POS} = 5 V, 25°C

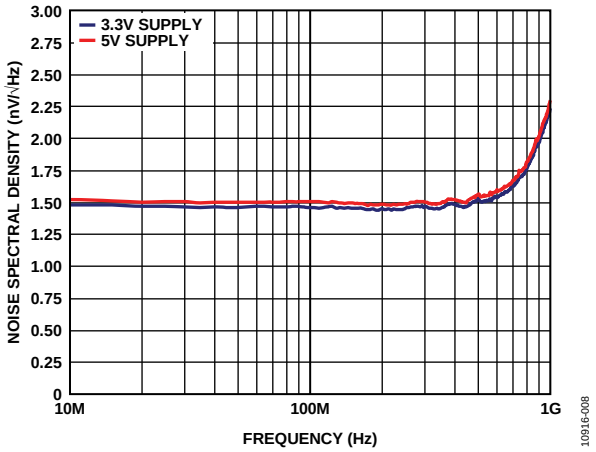


Figure 9. Noise Spectral Density vs. Frequency at V_{POS} = 3.3 V and V_{POS} = 5 V

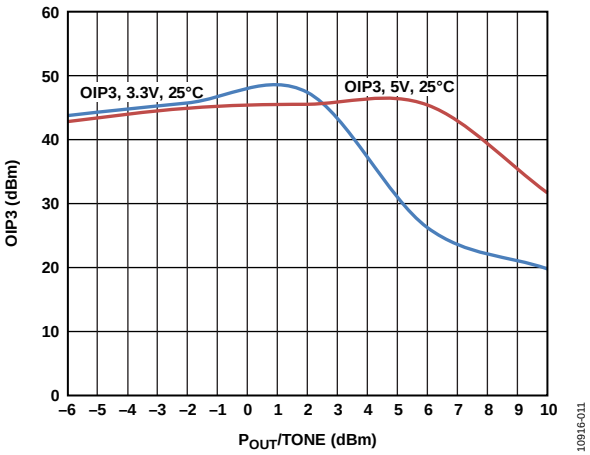


Figure 12. OIP3 vs. Output Power (P_{OUT}) per Tone, Frequency 200 MHz, V_{POS} = 3.3 V and V_{POS} = 5 V

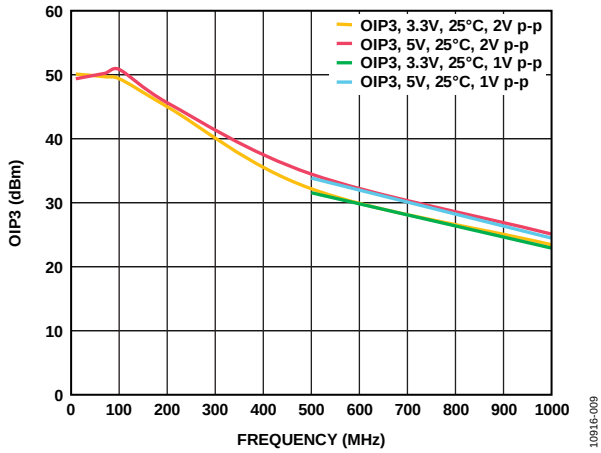


Figure 10. Output Third-Order Intercept (OIP3) at Output Level at 2 V p-p Composite, R_L = 200 Ω, V_{POS} = 3.3 V and V_{POS} = 5 V

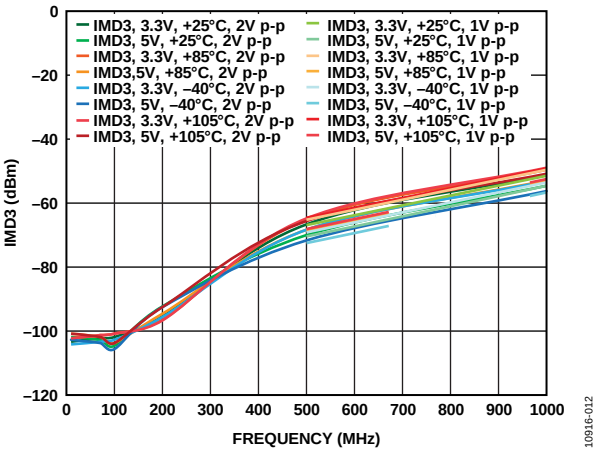


Figure 13. IMD3 vs. Frequency, Over Temperature, Output Level at 2 V p-p Composite, R_L = 200 Ω, V_{POS} = 3.3 V and V_{POS} = 5 V

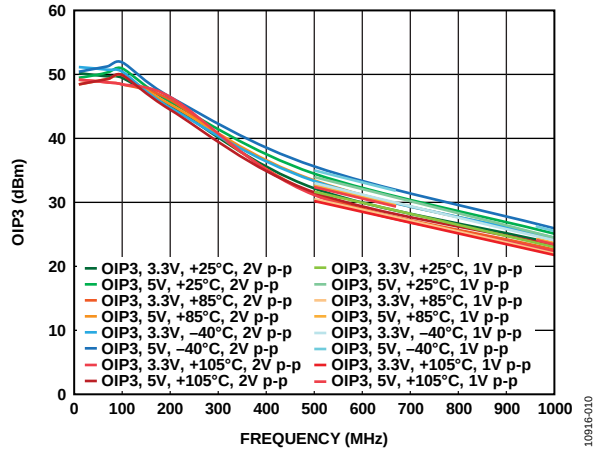


Figure 11. OIP3 vs. Frequency, Overtemperature, Output Level at 2 V p-p Composite, R_L = 200 Ω, V_{POS} = 3.3 V and V_{POS} = 5 V

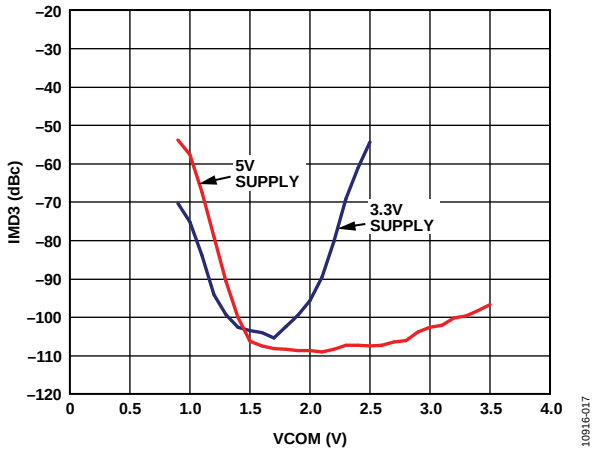


Figure 14. IMD3 vs. VCOM, Output Level at 2 V p-p Composite, R_L = 200 Ω, V_{POS} = 3.3 V and V_{POS} = 5 V, Frequency = 100 MHz

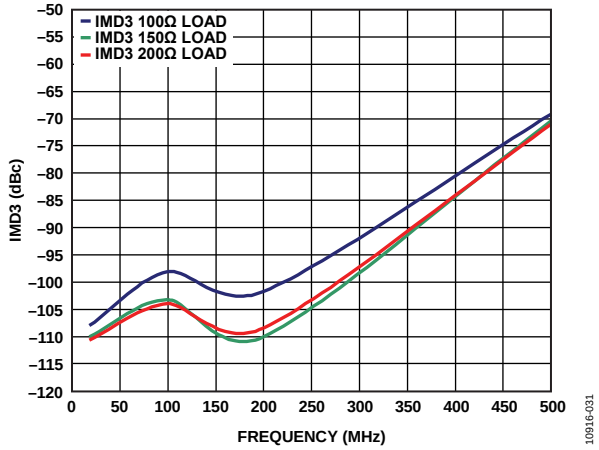


Figure 15. IMD3 vs. Frequency, R_L = 100 Ω, R_L = 150 Ω, and R_L = 200 Ω, V_{POS} = 3.3 V, Input Common-Mode = 1.65 V, Output Common-Mode = 1.25 V, V_{OUT} = 1.5 V p-p

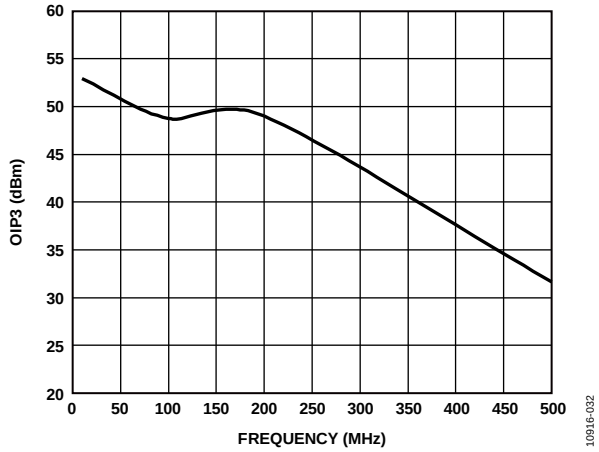


Figure 16. Single-Ended OIP3 vs. Frequency, V_{POS} = 3.3 V, 2 V p-p Composite Output, R_L = 200 Ω

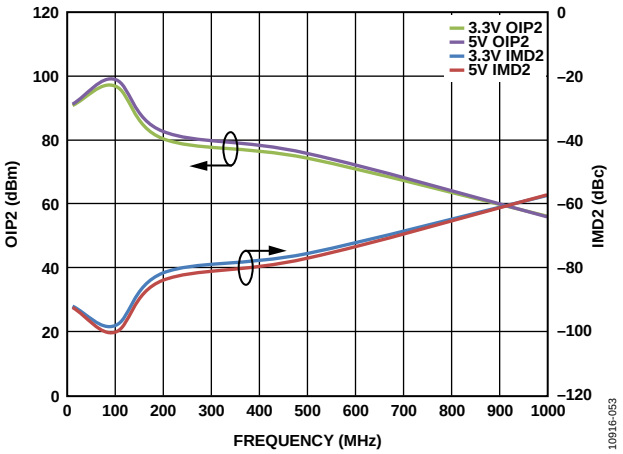


Figure 17. OIP2/IMD2 vs. Frequency

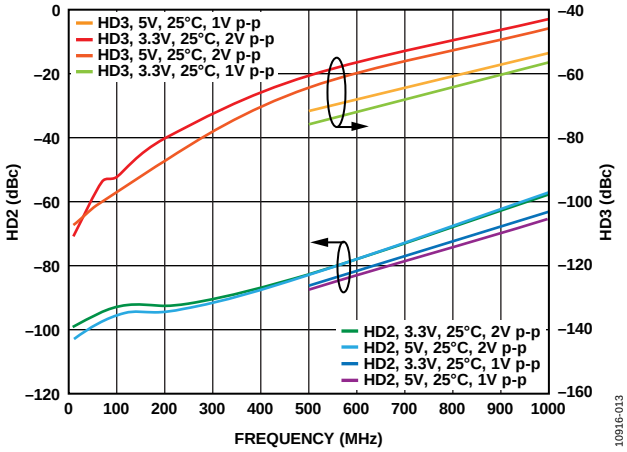


Figure 18. Harmonic Distortion (HD2/HD3) vs. Frequency, Output Level at 2 V p-p Composite, R_L = 200 Ω, V_{POS} = 3.3 V and V_{POS} = 5 V

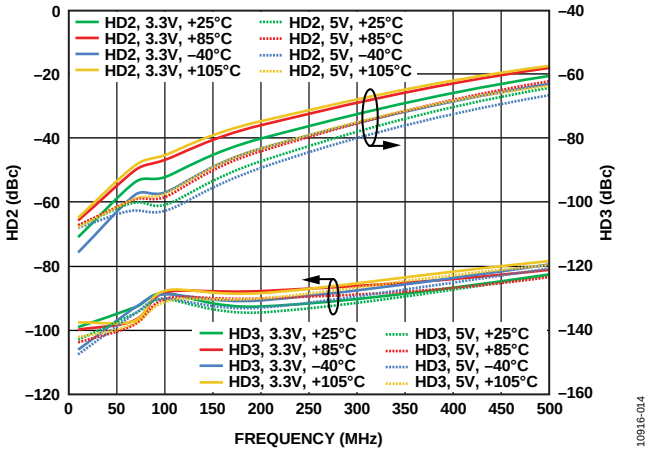


Figure 19. Harmonic Distortion (HD2/HD3) vs. Frequency, Output Level at 2 V p-p Composite, R_L = 200 Ω, V_{POS} = 3.3 V and V_{POS} = 5 V

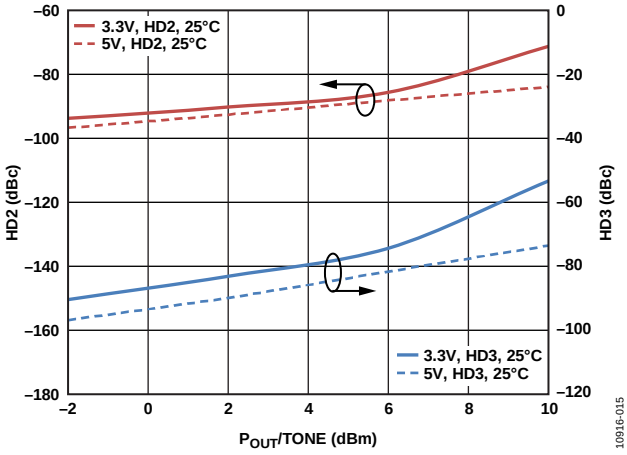


Figure 20. Harmonic Distortion (HD2/HD3) vs. Output Power (P_{OUT}) per Tone, Frequency = 200 MHz, R_L = 200 Ω, V_{POS} = 3.3 V and V_{POS} = 5 V

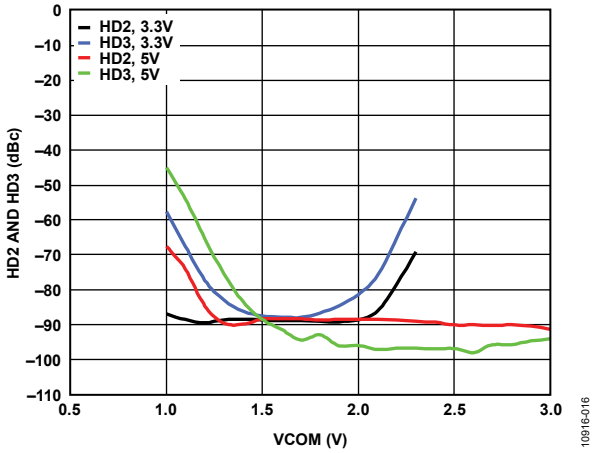


Figure 21. Harmonic Distortion (HD2/HD3) vs. VCOM, Output Level at 2 V p-p, R_L = 200 Ω, V_{POS} = 3.3 V and V_{POS} = 5 V, Frequency = 100 MHz

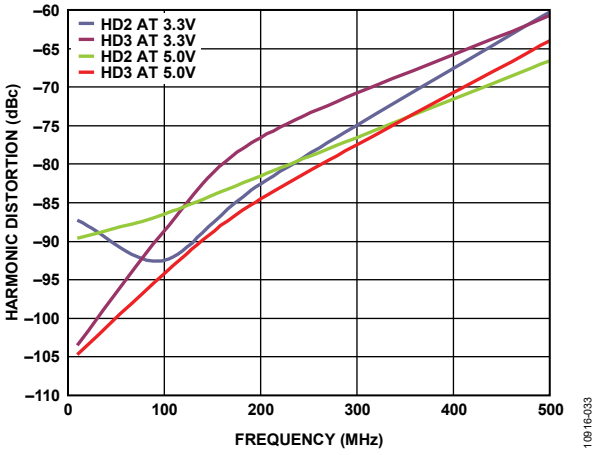


Figure 24. Single-Ended Harmonic Distortion (HD2/HD3) vs. Frequency, V_{POS} = 3.3 V and V_{POS} = 5 V, V_{OUT} = 2 V p-p, R_L = 200 Ω

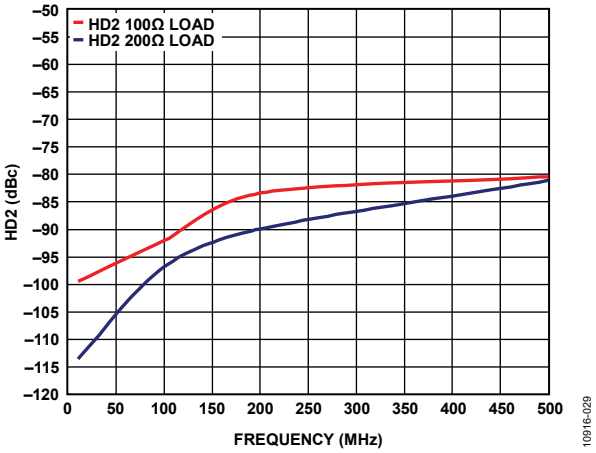


Figure 22. HD2 vs. Frequency, R_L = 100 Ω and R_L = 200 Ω, V_{POS} = 3.3 V, Input Common-Mode = 1.65 V, Output Common-Mode = 1.25 V, V_{OUT} = 1.5 V p-p

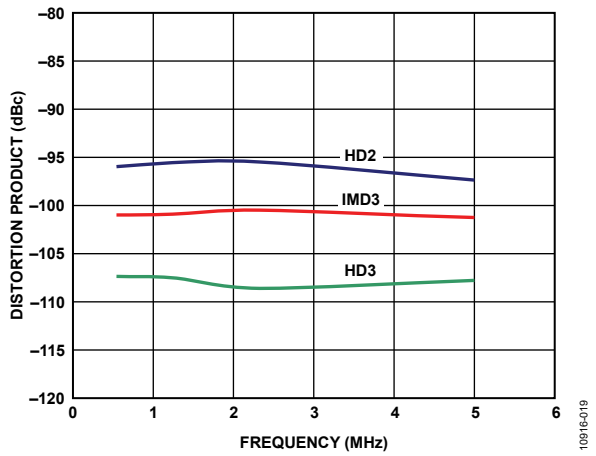


Figure 25. Low Frequency Distortion (HD2/HD3/IMD3) vs. Frequency, Output Level at 2 V p-p, R_L = 200 Ω, V_{POS} = 3.3 V

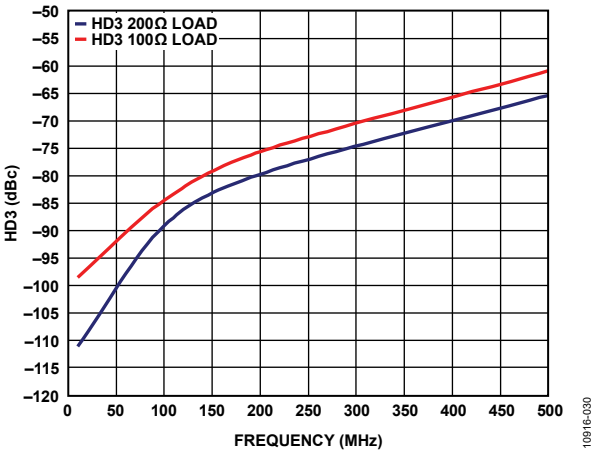


Figure 23. HD3 vs. Frequency, R_L = 100 Ω and R_L = 200 Ω, V_{POS} = 3.3 V, Input Common-Mode = 1.65 V, Output Common-Mode = 1.25 V, V_{OUT} = 1.5 V p-p

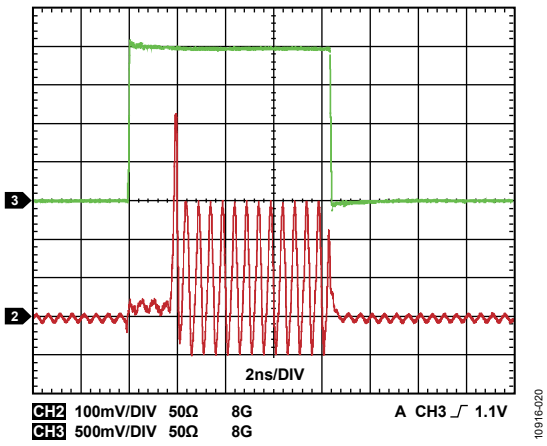


Figure 26. ENBLx Time Domain Response, V_{POS} = 3.3 V

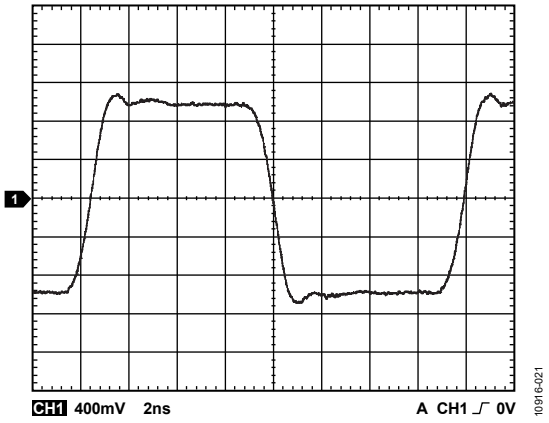


Figure 27. Large Signal Pulse Response Using a Slow Transient Signal Generator, 4 V p-p, V_{POS} = 3.3 V

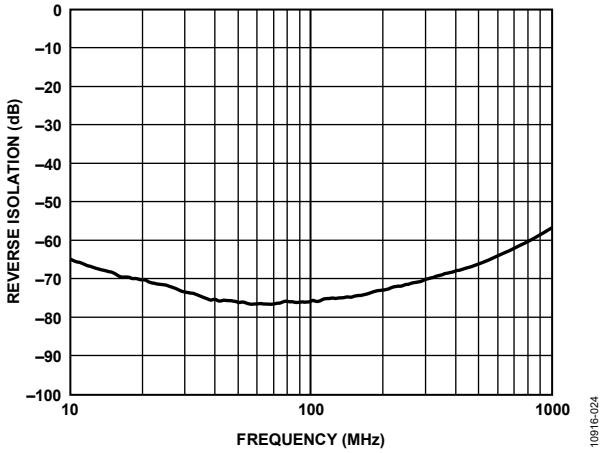


Figure 30. Reverse Isolation (S12) vs. Frequency

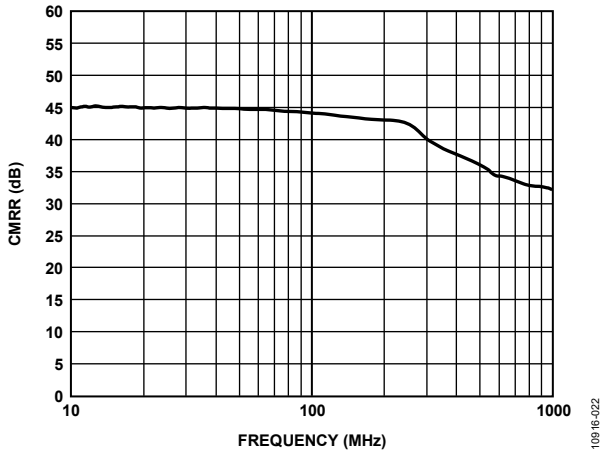


Figure 28. Common-Mode Rejection Ratio (CMRR) vs. Frequency

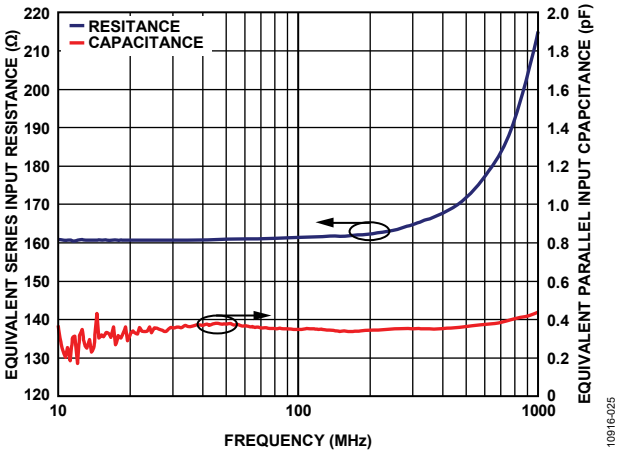


Figure 31. S11 Equivalent RLC Parallel Network

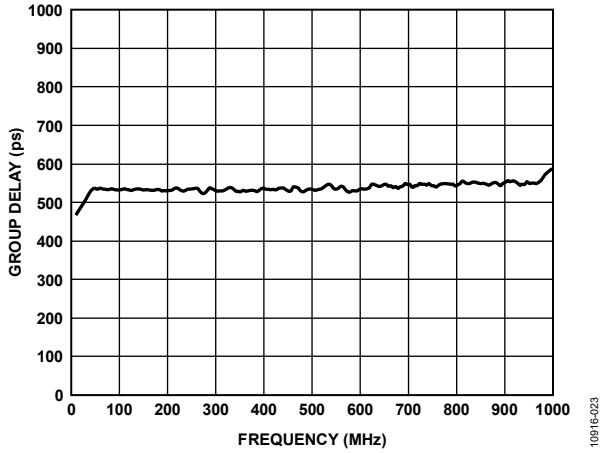


Figure 29. Group Delay vs. Frequency

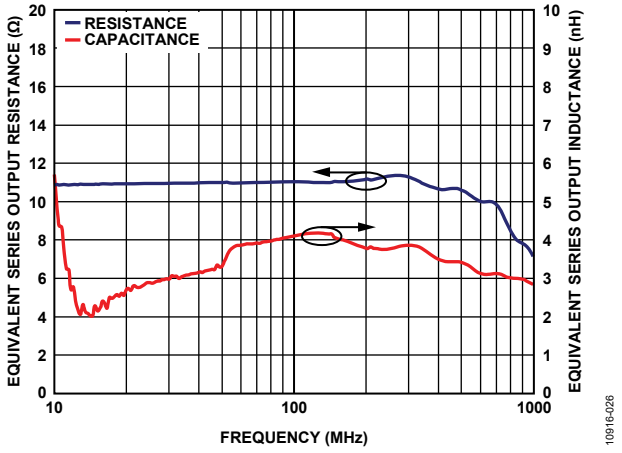


Figure 32. S22 Equivalent RLC Parallel Network

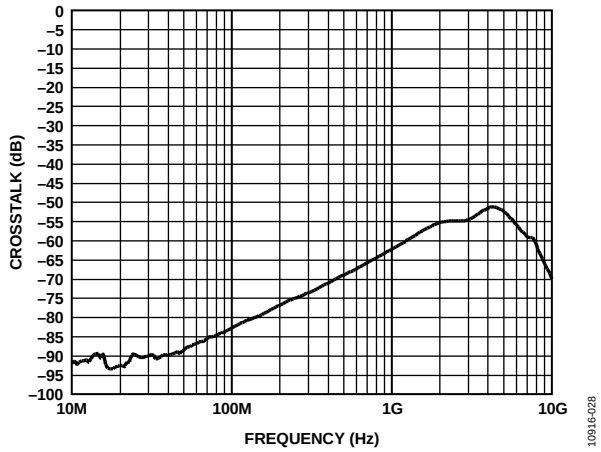


Figure 33. Output Referred Crosstalk, Channel A to Channel B, V_{POS} = 3.3 V, VCOM = 1.65 V

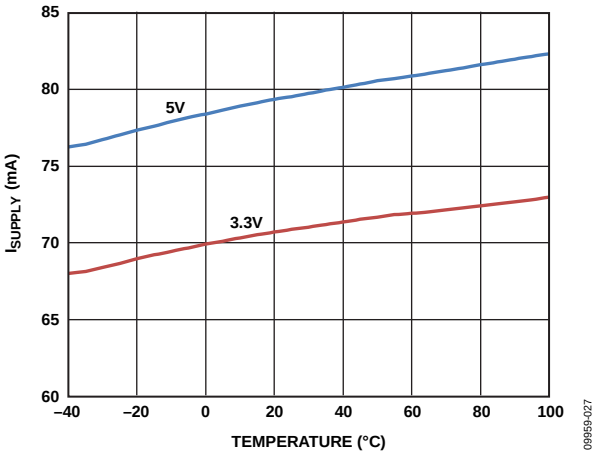


Figure 34. I_{SUPPLY} vs. Temperature, R_L = 200 Ω, V_{POS} = 3.3 V and V_{POS} = 5 V

CIRCUIT DESCRIPTION

The ADL5566 is a high gain, fully differential dual amplifier/ADC driver that uses a 2.8 V to 5 V supply. It provides a 16 dB gain that can be reduced by adding external series resistors. The 3 dB bandwidth is 4.5 GHz, and it has a differential input impedance of 160 Ω. It has a differential output impedance of 10 Ω and an output common-mode adjust voltage of 1.1 V to 1.8 V.

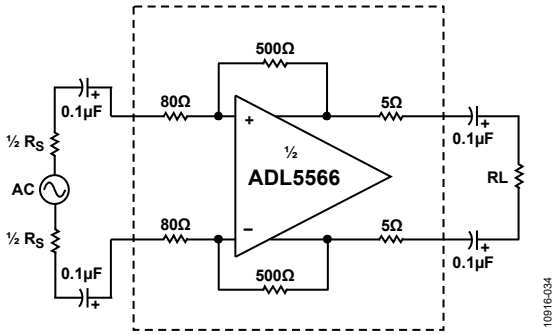


Figure 35. Basic Structure

The ADL5566 is composed of a dual fully differential amplifier with on-chip feedback and feed-forward resistors. The gain is fixed at 16 dB but can be reduced by adding two resistors in series with the two inputs (see the Gain Adjustment and Interfacing section). The amplifier is designed to provide a high differential open-loop gain and has an output common-mode circuit that enables the user to change the output common-mode voltage by applying a voltage to a VCOMx pin. The amplifier is designed to provide superior low distortion at frequencies to and beyond 300 MHz with low noise and low power consumption. The low distortion and noise are realized with a 3.3 V power supply at 140 mA. The dual amplifier has an extremely high gain bandwidth (GBW) product that results in distortion levels that are the best in the industry for power consumed at frequencies beyond 100 MHz. This amplifier achieves greater than −69 dBc IMD3 at 500 MHz and −100 dBc at 200 MHz for 2 V p-p operation. In addition, the ADL5566 can also deliver 5 V p-p operation under heavy loads. The internal gain is set at 16 dB, and the part has a noise figure of 6.5 dB and a RTI of 1.5 nV/√Hz. When comparing noise figure and distortion performance, this amplifier delivers the best in category spurious-free dynamic range (SFDR).

The ADL5566 is very flexible in terms of I/O coupling. It can be ac- or dc-coupled. For dc coupling, the output common-mode voltage (VCOMx) can be adjusted (using the VCOMx pin) from 1.1 V to 1.8 V output for VCCx at 3.3 V and up to 3 V with VCCx at 5 V. For the best distortion, the common-mode output should not go below 1.25 V at VCCx equal to 3.3 V and 1.35 V for 5 V VCCx operation. Note that the input common-mode voltage slaves to the VCOMx output voltage when ac-coupled at the inputs. For dc-coupled inputs, the input common-mode voltage should also stay between 1.25 V and 1.8 V for a 3.3 V supply and 1.35 V to 3.5 V for a 5 V supply. Note again that, for ac-coupled applications with series capacitors at the inputs, as in Figure 37, the output common-mode voltage, VCOMx, sets the common-mode input to the same level. Because of the wide input common-mode range, this part can easily be dc-coupled to many types of mixers, demodulators, and amplifiers. Forcing a higher input VCOMx does not affect the output VCOMx in dc-coupled mode. Note that, if the outputs are ac-coupled (see the ADC Interfacing section), no external VCOMx adjust is required because the amplifier common-mode outputs are set at VCCx/2.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 36 shows the basic connections for operating the ADL5566. Apply a voltage between 3 V and 5 V to the VCC1 and VCC2 pins through a 5.1 nH inductor and decouple the supply side of the inductor with at least one low inductance, 0.1 µF surface-mount ceramic capacitor. In addition, decouple the VCOM1 and VCOM2 pins (Pin 21 and Pin 10) using a 0.1 µF capacitor. The ENBL1 and ENBL2 pins (Pin 22 and Pin 9) are tied to their amplifiers VCC_x pin to enable each amplifier. A differential signal is applied to Amplifier 1 through Pin 1 (VIN1) and Pin 2 (VIP1) and to Amplifier 2 through Pin 5 (VIP2) and Pin 6 (VIN2). Each amplifier has a gain of 16 dB.

The input pins, Pin 1 (VIN1) and Pin 2 (VIP1), and the output pins, Pin 18 (VON1) and Pin 17 (VOP1), are biased by applying a voltage to Pin 21 (VCOM1). If VCOM1 is left open, VCOM1 equals ½ of VCC1. The input pins, Pin 5 (VIP2) and Pin 6 (VIN2), and the output pins, Pin 13 (VON2) and Pin 14 (VOP2), are biased by applying a voltage to VCOM2. If VCOM2 is left open, VCOM2 equals ½ of VCC2. The ADL5566 can be ac-coupled as shown in Figure 36 or can be dc-coupled if within the specified input and output common-mode voltage ranges (see the Circuit Description section). To enable the ADL5566, the ENBL1 and ENBL2 pins must be pulled high. Pulling the ENBL1/ENBL2 pins low puts the ADL5566 in sleep mode, reducing the current consumption to 7 mA at ambient.

A series 5.1 nH inductor can be connected to the VCCx pins with the V_{CC} decoupling capacitor connected to the V_{CC} bus side (see Figure 36 and Figure 53). This inductor with the internal capacitance of the amplifier results in a two pole low-pass network and reduces the amplifier V_{CC} noise.

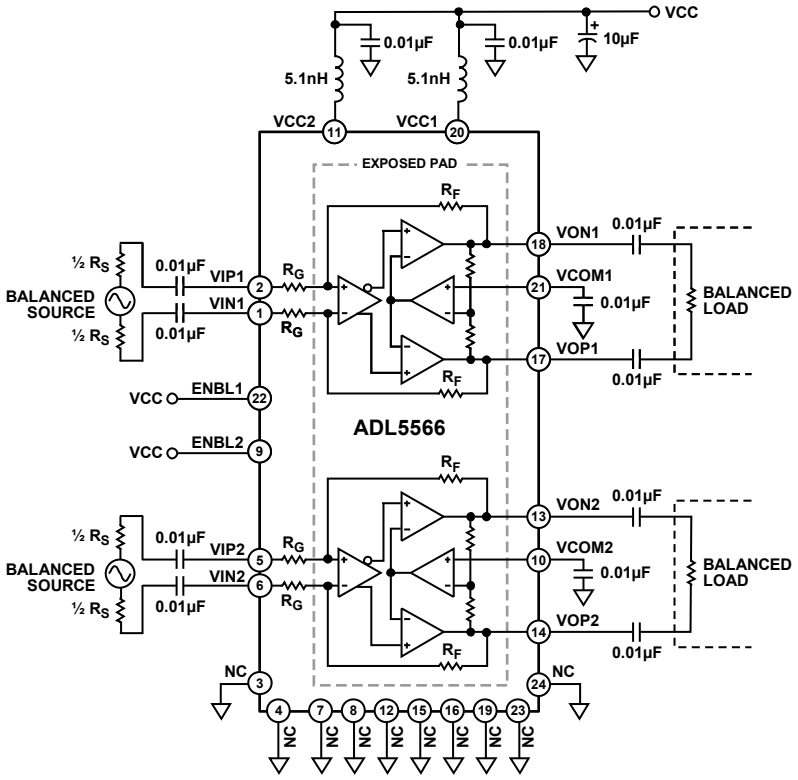


Figure 36. Basic Connections

INPUT AND OUTPUT INTERFACING

The ADL5566 can be configured as a differential input to differential output driver, as shown in Figure 37. The 36 Ω resistors, R1 and R2, combined with the ETC1-1-13 balun transformer, provide a 50 Ω input match for the 160 Ω input impedance. The input and output 0.1 µF capacitors isolate the $V_{CC}/2$ bias from the source and balanced load. The load should equal 200 Ω to provide the expected ac performance (see the Specifications section).

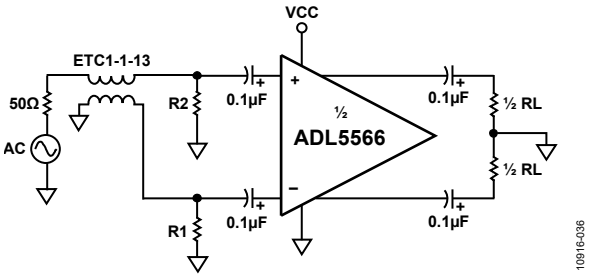


Figure 37. Differential Input to Differential Output Configuration

The differential gain of the ADL5566 is dependent on the source impedance and load, as shown in Figure 38.

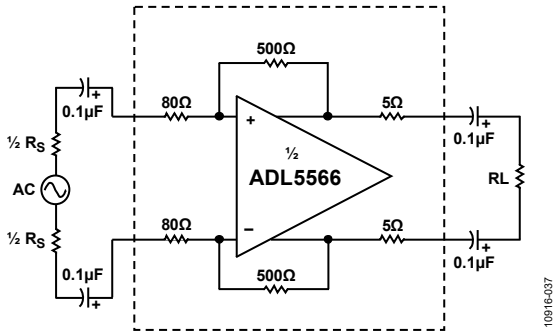


Figure 38. Differential Input Loading Circuit

The differential gain can be determined by

$$A_V = \frac{500}{80} \times \frac{R_L}{10 + R_L} \quad (1)$$

Single-Ended Input to Differential Output

The ADL5566 can also be configured in a single-ended input to differential output driver, as shown in Figure 39. In this configuration, the gain of the part is reduced due to the application of the signal to only one side of the amplifier. The input and output 0.1 µF capacitors isolate the $V_{CC}/2$ bias from the source and the balanced load. R2 is used to match the single-ended input impedance of the amplifier (131 Ω) with the 50 Ω source. R1 is selected to balance the input of the amplifier. See the Application Note AN-0990 for more information on terminating single-ended inputs. The performance for this configuration is shown in Figure 16 and Figure 24.

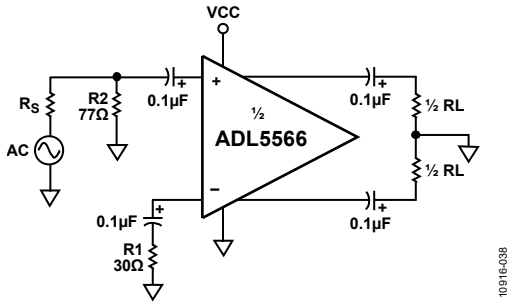


Figure 39. Single-Ended Input to Differential Output Configuration

The single-ended gain configuration of the ADL5566 is dependent on the source impedance and load, as shown in Figure 40.

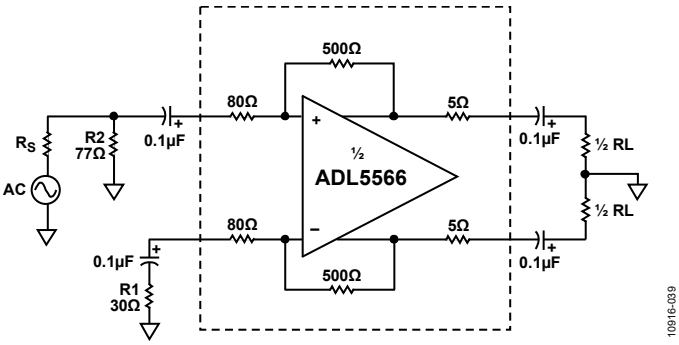


Figure 40. Single-Ended Input Loading Circuit

The single-ended gain can be determined by the following two equations:

$$R_{MATCH} = \frac{R2 \times 131}{R2 + 131}$$

$$A_{V1} = \frac{500}{80 + \left(\frac{R_S \times R2}{R_S + R2}\right)} \times \frac{R2}{R_S + R2} \times \frac{R_{MATCH} + R_S}{R_{MATCH}} \times \frac{R_L}{10 + R_L}$$

GAIN ADJUSTMENT AND INTERFACING

The effective gain of the ADL5566 can be reduced by adding two resistors in series with the inputs to reduce the 16 dB gain.

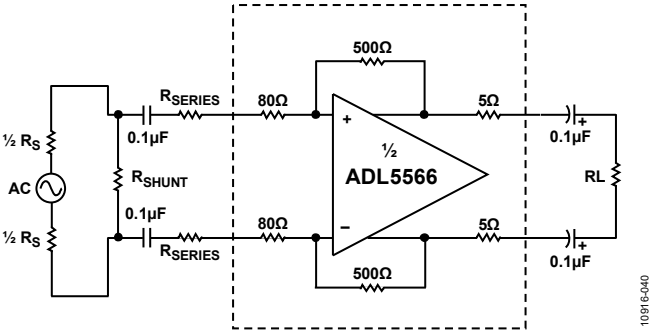


Figure 41. Gain Adjustment Using a Series Resistor Show

To find R_{SERIES} for a given A_V gain and R_L, use the following:

$$R_{SERIES} = \left[\frac{500}{\left[\frac{A_V}{\left(\frac{R_L}{10 + R_L} \right)} \right]} \right] - 80 \quad (3)$$

To calculate the A_V gain for a given R_{SERIES} and R_L, use the following:

$$A_{GAIN} = \left(\frac{500}{R_{SERIES} + 80} \right) \times \left(\frac{R_L}{10 + R_L} \right) \quad (4)$$

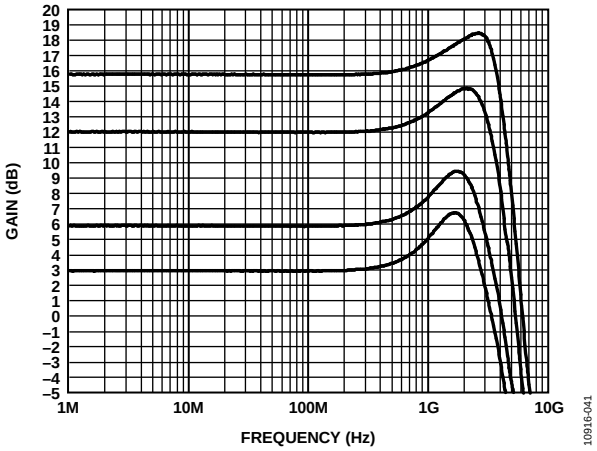


Figure 42. SDD21, V_{POS} = 3.3 V, Three Gains, 25°C

The necessary shunt component, R_{SHUNT}, to match to the source impedance, R_S, can be expressed with the following:

$$R_{SHUNT} = \frac{1}{\frac{1}{R_S} - \frac{1}{2R_{SERIES} + 160}} \quad (5)$$

The voltage gain for multiple shunt resistor values are summarized in Table 5. The source resistance and input impedance need careful attention when using Equation 5. The reactance of the input impedance of the ADL5566 and the ac coupling capacitors must be considered before assuming that they make a negligible contribution.

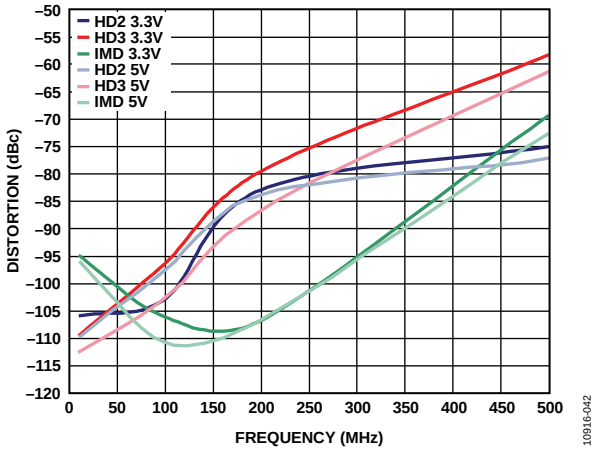


Figure 43. IMD, HD2, and HD3 vs. Frequency, A_V = 6 dB, 2 V p-p Output, V_{POS} = 3.3 and V_{POS} = 5 V

Table 5. Differential Gain Adjustment Using Series Resistor

Target Gain (dB)	Actual Gain (dB)	R_S (Ω)	R_{SERIES} (Ω)[1]	R_{SHUNT} (Ω)[1]
0	−0.1	50	396.2	52.8
1	+1.2	50	344.4	53.1
2	+2.1	50	298.3	53.5
3	+2.9	50	257.1	54
4	+4.1	50	220.5	54.5
5	+5.1	50	187.8	55.1
6	+6.1	50	158.7	55.8
7	+6.9	50	132.7	56.7
8	+8.1	50	109.6	57.6
9	+8.9	50	89	58.7
10	+10	50	70.6	60
11	+11.1	50	54.2	61.4
12	+12	50	39.6	63.2
13	+12.8	50	26.6	65.3
14	+14	50	15	67.9
15	+15.1	50	4.8	70.9
16	+15.8	50	0	72.7

[1] The resistor values are rounded to the nearest real resistor value.

ADC INTERFACING

The ADL5566 is a dual high output linearity amplifier that is optimized for ADC interfacing. One option of applying the ADL5566 to drive an ADC is shown in Figure 47. The wideband 1:1 transmission line balun provides a differential input to the amplifier, and the 36 Ω resistors provide a 50 Ω match to the source. The ADL5566 is ac-coupled from the input and output to avoid common-mode loading. A reference voltage is required to bias the AD9268 inputs and is delivered through the 200 Ω resistors. These, in parallel with the 400 Ω resistor, create the low frequency amplifier load of 200 Ω. The 56 nH inductors and the 56 pF capacitor are used to create a 70 MHz low-pass filter. The two 25 Ω resistors are added to raise the ADL5566 output impedance, which reduces peaking when the filter drives a light load. The two 25 Ω resistors provide isolation to the switching currents of the ADC sample-and-hold circuitry. The AD9268 dual ADC presents a 6 kΩ differential load impedance and requires a 1 V p-p to 2 V p-p input signal to reach full scale. The system frequency response is shown in Figure 46. By applying a 2 V p-p, 32 MHz single-tone signal from the ADL5566 in a gain of 16 dB, an SFDR of 94.6 dBc is achieved. By applying two half scale signals of 32 MHz and 33 MHz from the ADL5566 in a gain of 16 dB, an SFDR of 90.5 dBc is realized.

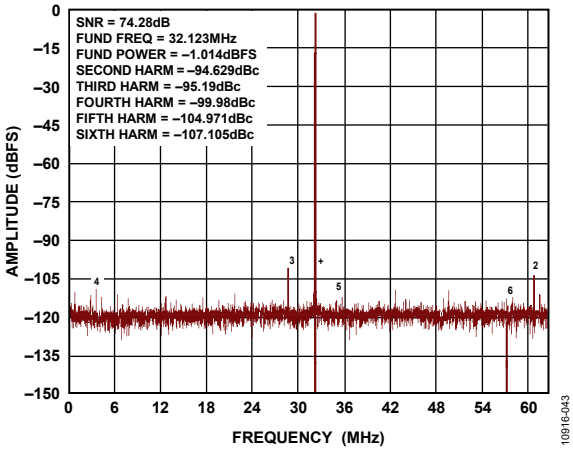


Figure 44. Measured Single-Tone Performance of the Circuit in Figure 47 for a 32 MHz Input Signal

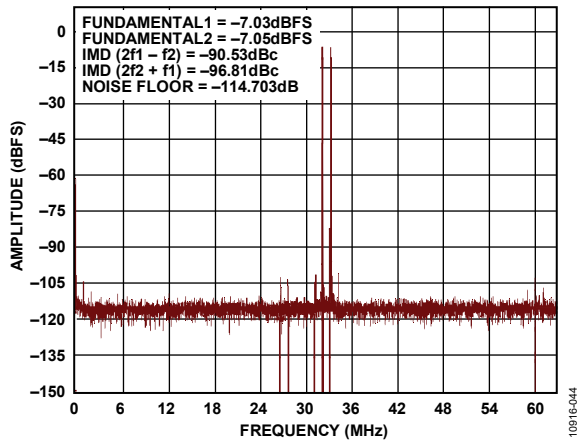


Figure 45. Measured Two-Tone Performance of the Circuit in Figure 47 for a 32 MHz and 33 MHz Input Signals

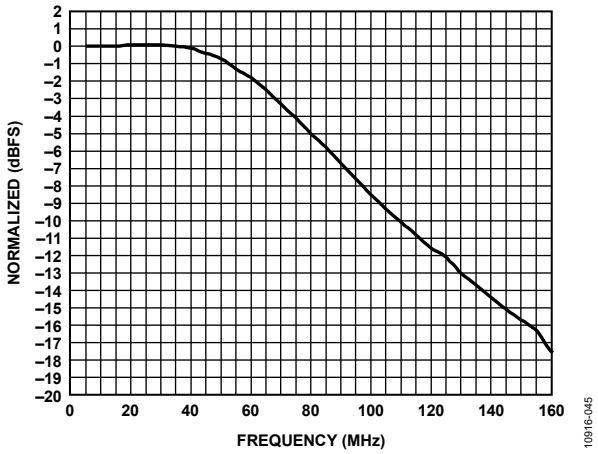


Figure 46. Measured Relative Frequency Response of the Wideband ADC Interface Depicted in Figure 47

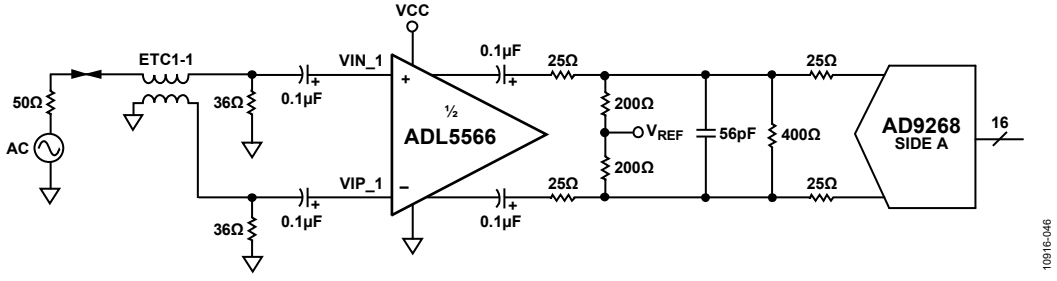


Figure 47. Wideband ADC Interfacing Example Featuring the AD9268

DC-COUPLED RECEIVER APPLICATION

The ADL5566 is well suited for dc-coupled applications, such as zero-IF direct conversion receivers. An example receiver configuration is shown in Figure 48, consisting of the ADL5380 quadrature demodulator and the ADL5566 dual differential amplifier. This is an ideal combination because of the wide RF input bandwidth from 400 MHz to 6 GHz, the high linearity of the ADL5566, and when operating on a 5 V supply, level shifting to align the common-mode voltage is not required.

The interface between the ADL5380 and the ADL5566 is straight forward because the impedance presented by the ADL5566 is sufficiently high enough to permit directly connecting the two devices without any degradation in performance. When using the ADL5566 as shown in Figure 48, the OIP3s at the outputs are improved due to the high OIP3 of the amplifier pair (see Table 6). In a real-world receiver where blockers are present, it is advantageous to insert a low-pass filter between the ADL5380 and the ADL5566 to remove these undesired signals.

If the ADL5566 is followed by an ADC, insert an antialiasing filter between the ADL5566 and the ADC to prevent broadband noise from aliasing back in band. For more information on this interface, see the ADC Interfacing section.

The cascade of the performance of the circuit shown in Figure 48 is presented in Table 6.

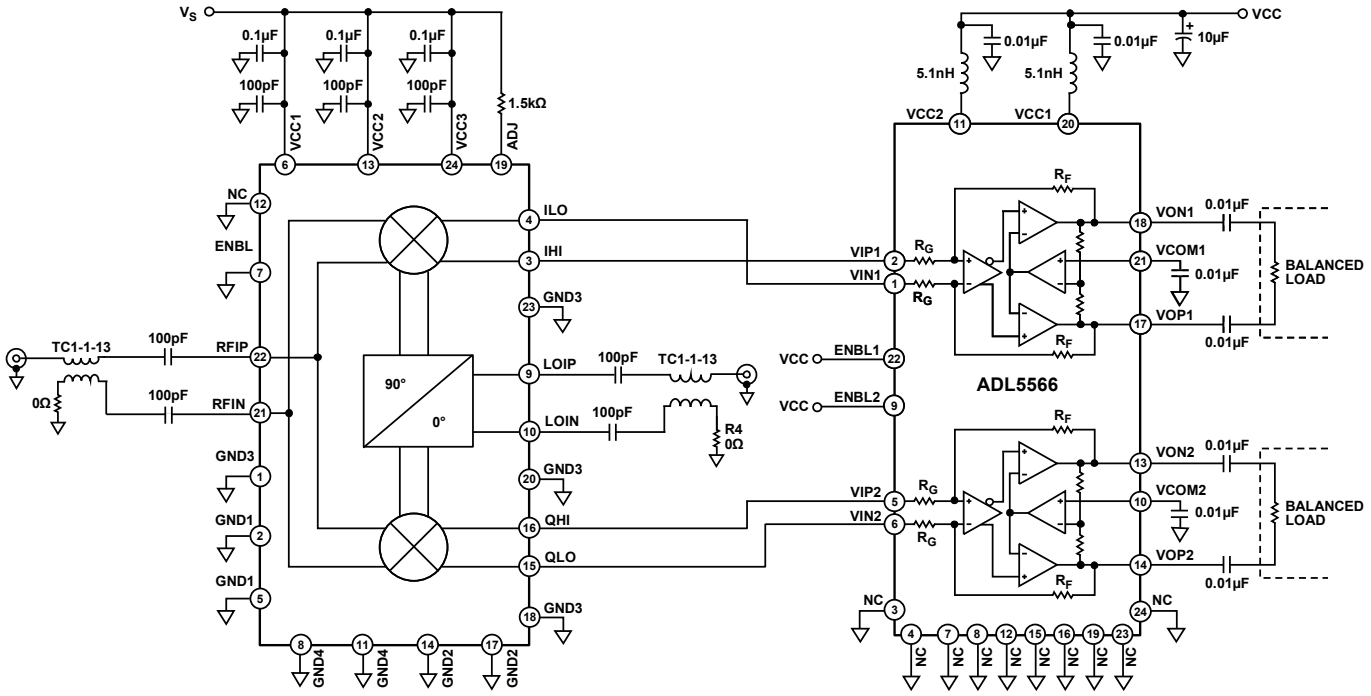


Figure 48. DC-Coupled Interface Example Featuring the ADL5380

Table 6. Cascade Performance of the ADL5380 and ADL5566

	IF Frequency = 200 MHz, R_L = 200 Ω, V_{OUT} = 2 V p-p Composite						
Frequency (MHz)	**HD2 (dBc)**	**HD3 (dBc)**	**OIP3 (dBm)**	**ADL5380 OIP3 (dBm)[1]**	**OIP2 (dBm)**	**Voltage Gain (dB)**	**Power Gain (dB)**
900	−79.3	−84.2	44.9	26.2	91.8	18.1	12.0
1900	−82.2	−80.5	40.8	26.5	83.9	18.1	12.0
2700	−80.7	−73.9	39.6	25.7	75.6	18.1	12.0

[1] Output referred IP3 of the ADL5380, P_{IN} = −14 dBm, and R_L = 200 Ω.

LAYOUT CONSIDERATIONS

High-Q inductive drives and loads, as well as stray transmission line capacitance in combination with package parasitics, can potentially form a resonant circuit at high frequencies, resulting in excessive gain peaking or possible oscillation. If RF transmission lines connecting the input or output are used, design them such that stray capacitance at the input/output pins is minimized. In many board designs, the signal trace widths should be minimal where the driver/receiver is no more than one-eighth of the wavelength from the amplifier. This nontransmission line configuration requires that underlying and adjacent ground and low impedance planes be dropped from the signal lines.

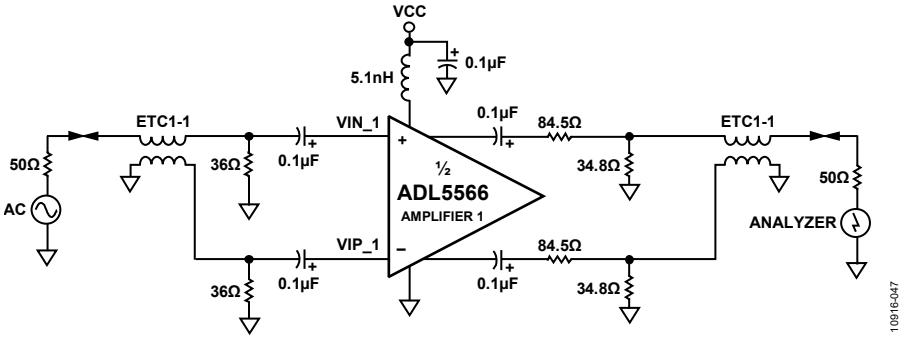


Figure 49. General-Purpose Characterization Circuit

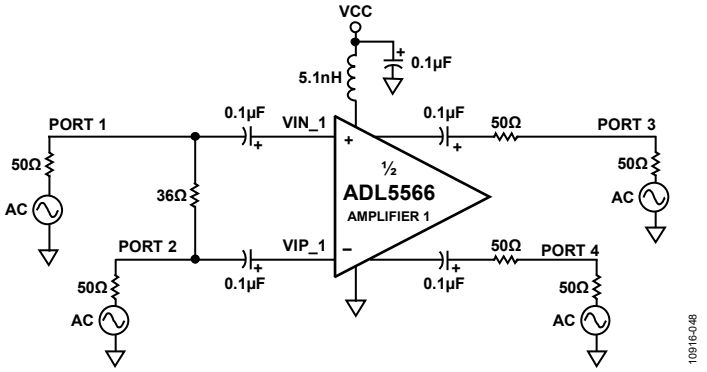


Figure 50. Differential Characterization Circuit Using Agilent E8357A Four-Port PNA

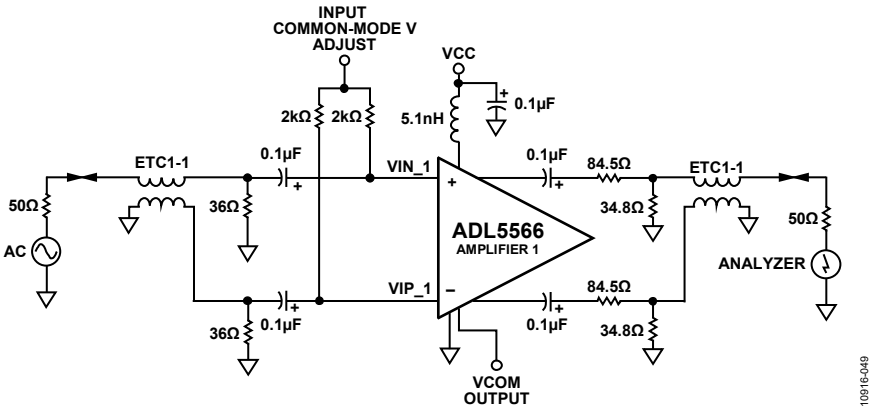


Figure 51. Distortion Measurement Circuit for Various Common-Mode Voltages

SOLDERING INFORMATION AND RECOMMENDED LAND PATTERN

Figure 52 shows the recommended land pattern for the ADL5566. The ADL5566 is contained in a 4 mm × 4 mm LFCSP package, which has an exposed ground paddle (EPAD). This paddle is internally connected to the ground of the chip. To minimize thermal impedance and ensure electrical performance, solder the paddle to the low impedance ground plane on the printed circuit board (PCB). To further reduce thermal impedance, it is recommended that the ground planes on all layers under the paddle be stitched together with vias.

For more information on land pattern design and layout, refer to the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

This land pattern, on the ADL5566 evaluation board, provides a measured thermal resistance (θ_{JA}) of 34.0°C/W. To measure θ_{JA}, the temperature at the top of the LFCSP package is found with an IR temperature gun. Thermal simulation suggests a junction temperature 1.5°C higher than the top of package temperature. With additional ambient temperature and I/O power measurements, θ_{JA} can be determined.

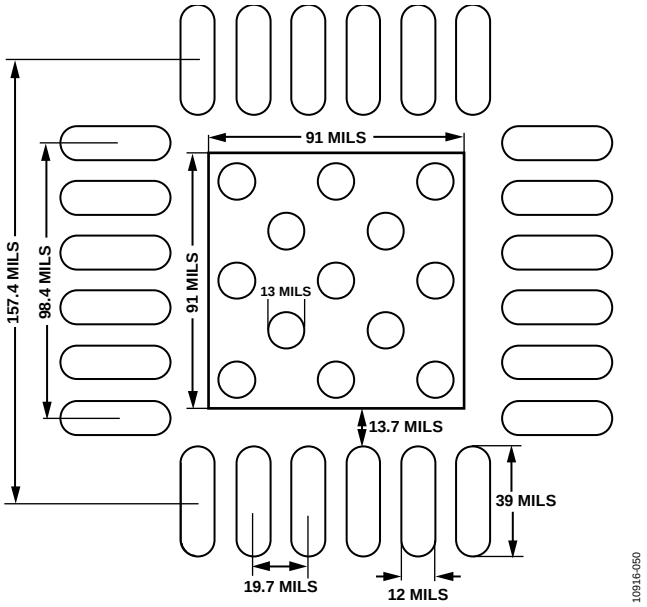


Figure 52. Recommended Land Pattern

EVALUATION BOARD

Figure 53 shows the schematic of the ADL5566 evaluation board. The board is powered by a single supply in the 3 V to 5 V range. The power supply is decoupled by 10 µF and 0.1 µF capacitors. The L1 and L2 inductors decouple the ADL5566 from the power supply.

Table 7 details the various configuration options of the evaluation board. Figure 54 and Figure 55 show the component and circuit side layouts of the evaluation board.

The balanced input and output interfaces are converted to single ended with a pair of baluns (M/A-COM ETC1-1-13). The baluns at the input, T1 and T2, provide a 50 Ω single-ended-to-differential transformation. The output baluns, T3 and T4, and the matching components are configured to provide a 200 Ω to 50 Ω impedance transformation with an insertion loss of about 11 dB.

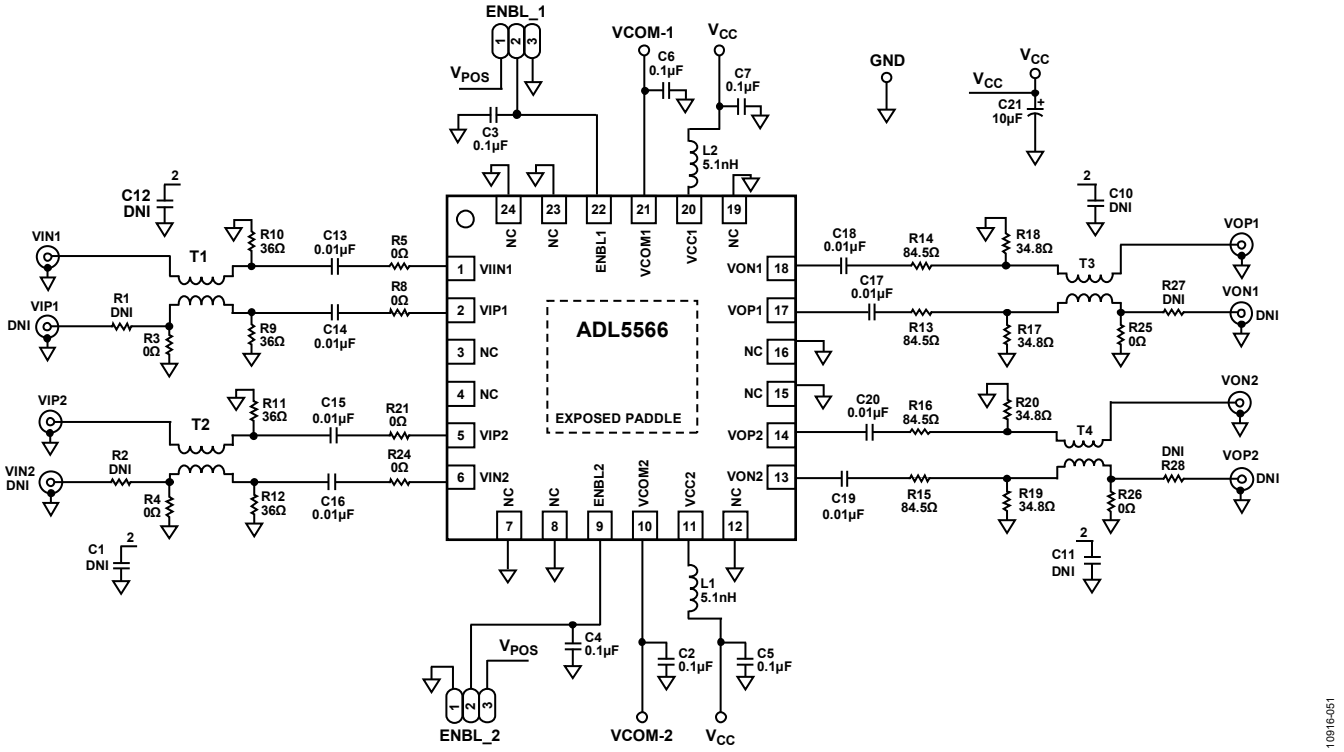


Figure 53. Evaluation Board Schematic

Table 7. Evaluation Board Configuration Options

Component	Description	Default Condition
V_{POS}, GND	Ground and supply test loops.	V_{POS}, GND = installed
C5, C7, C21, L1, L2	Power supply decoupling. The supply decoupling consists of a 10 µF capacitor (C21) and two 0.1µF capacitors, C5 and C7, connected between the supply lines and ground. L1 and L2 decouple the ADL5566 from the power supply.	C21 = 10 µF (Size D), C5, C7 = 0.1 µF (Size 0402), L1, L2 = 5.1 nH (Size 0603)
VIN1, VIP1, VIP2, VIN2, R1, R2, R3, R4, R5, R8, R9, R10, R11, R12, R21, R24, C13, C1, C12, C14, C15, C16, T1, T2	Input interface. The SMA labeled VIN1 is the input to Amplifier 1. T1 is a 1:1 impedance ratio balun to transform a single-ended input into a balanced differential signal. Removing R3, installing R1 (0 Ω), and installing an SMA connector (VIP1) allow driving from a differential source. C13 and C14 provide ac coupling. C12 is an optional bypass capacitor. R9 and R10 provide a differential 50 Ω input termination. The SMA labeled VIP2 is the input to Amplifier 2. T2 is a 1:1 impedance ratio balun to transform a single-ended input into a balanced differential signal. Removing R4, installing R2 (0 Ω), and installing an SMA connector (VIN2) allow driving from a differential source. C15 and C16 provide ac coupling. C1 is an optional by pass capacitor. R11 and R12 provide a differential 50 Ω input termination.	VIN1, VIP2 = installed, VIP1, VIN2 = not installed, R1, R2 = DNI, R3, R4, R5, R8, R21, R24 = 0 Ω (Size 0402), R9, R10, R11, R12 = 36 Ω (Size 0402), C13, C14, C15, C16 = 0.01 µF (Size 0402), C1, C12 = DNI, T1, T2 = ETC1-1-13 (M/A-COM)
VOP1, VON1, VON2, VOP2, C10, C11, C17, C18, C19, C20, R13, R14, R15, R16, R17, R18, R19, R20, R25, R26, R27, R28, T3, T4	Output interface. The SMA labeled VOP1 is the output for Amplifier 1. T3 is a 1:1 impedance ratio balun used to transform a balanced differential signal to a single-ended signal. Removing R25, installing R27 (0 Ω), and installing an SMA connector (VON1) allow differential loading. C10 is an optional bypass capacitor. C17 and C18 provide ac coupling. R13, R14, R17, and R16 are provided for generic placement of matching components. The SMA labeled VON2 is the output for Amplifier 2. T4 is a 1:1 impedance ratio balun used to transform a balanced differential signal to a single-ended signal. Removing R26, installing R28 (0 Ω), and installing an SMA connector (VOP2) allow differential loading. C11 is an optional bypass capacitor. C19 and C20 provide ac coupling. R15, R16, R19, and R20 are provided for generic placement of matching components. The evaluation board is configured to provide a 200 Ω to 50 Ω impedance transformation with an insertion loss of 11 dB.	VOP1, VON2 = installed, VON1, VOP2 = not installed, R13, R14, R15, R16 = 84.5 Ω (Size 0402), R17, R18, R19, R20 = 34.8 Ω (Size 0402), R25, R26 = 0 Ω (Size 0402), R27, R28 = DNI (Size 0402), C10, C11 = DNI (Size 0402), C17, C18 = 0.01 µF (Size 0402), C19, C20 = 0.01 µF (Size 0402), T3, T4 = ETC1-1-13 (M/A-COM)

Component	Description	Default Condition
ENBL_1, ENBL_2, C3, C4	Device enable. ENBL_1 is the enable for Amplifier 1. Connecting a jumper between Pin 2 and V_{POS} enables Amplifier 1. C3 is a bypass capacitor. ENBL_2 is the enable for Amplifier 2. Connecting a jumper between Pin 2 and V_{POS} enables Amplifier 2. C4 is a bypass capacitor.	ENBL_1, ENBL_2 = installed, C3, C4 = 0.1 µF (Size 0402)
VCOM-1, VCOM-2, C2, C6	Common-mode voltage interface. VCOM1 is the common-mode interface for Amplifier 1. A voltage applied to this pin sets the common-mode voltage of the output of Amplifier 1. VCOM2 is the common-mode interface for Amplifier 2. A voltage applied to this pin sets the common-mode voltage of the output of Amplifier 2. Typically decoupled to ground with a 0.1 µF capacitor (C2 and C6). With no reference applied, input and output common mode float to midsupply (V_{CC}/2).	VCOM-1, VCOM-2 = installed C2, C6 = 0.1 µF (Size 0402)

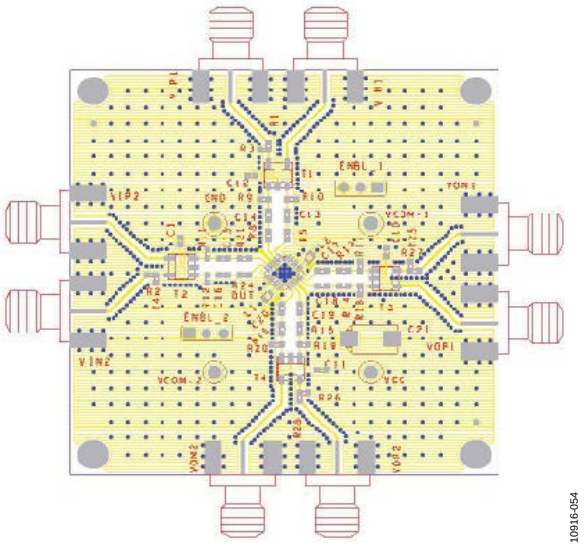


Figure 54. Layout of Evaluation Board, Component Side

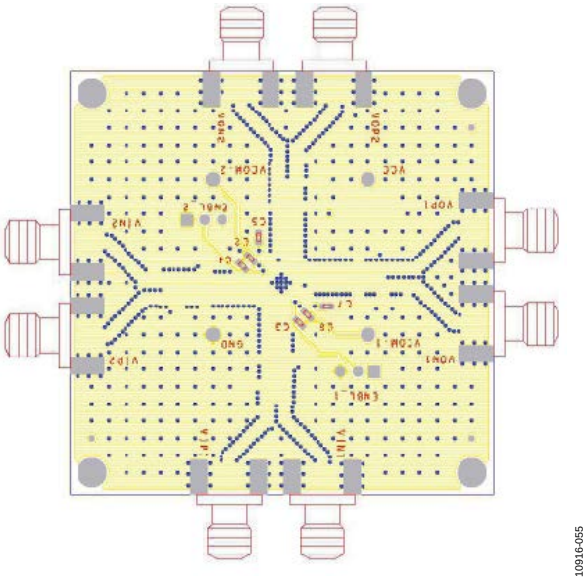
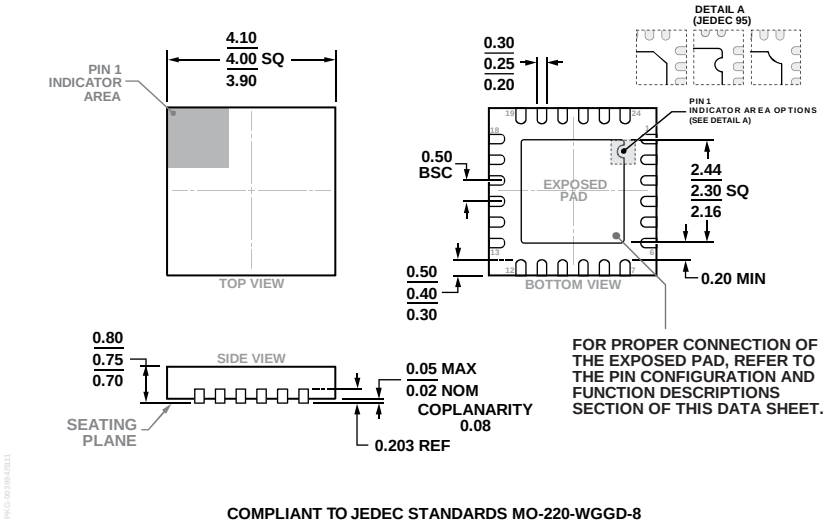


Figure 55. Layout of Evaluation Board, Circuit Side

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-8

Figure 56. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADL5566ACPZ-R7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP], 7″ Tape and Reel	CP-24-14
ADL5566-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.