

ADG608/ADG609—SPECIFICATIONS

DUAL SUPPLY¹ ($V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted)

Parameter	B Version +25°C −40°C to +85°C		T Version +25°C −55°C to +125°C		Units	Test Conditions/ Comments	
ANALOG SWITCH							
Analog Signal Range	V _{SS} to V _{DD}		V _{SS} to V _{DD}		V	−3.5 V ≤ V _S ≤ +3.5 V, I _S = −1 mA; V _{DD} = +4.5 V, V _{SS} = −4.5 V; Test Circuit 1	
R _{ON}	22 30		22 30		Ω typ Ω max		
ΔR _{ON}	5	6	5	6	Ω max		
R _{ON} Match	2	3	2	3	Ω max		
LEAKAGE CURRENTS							
Source OFF Leakage I _S (OFF)	±0.05 ±0.5	±2	±0.05 ±0.5	±10	nA typ nA max	V _{DD} = +5.5 V, V _{SS} = −5.5 V V _D = ±4.5 V, V _S = ∓4.5 V; Test Circuit 2	
Drain OFF Leakage I _D (OFF)	±0.05		±0.05		nA typ	V _D = ±4.5 V, V _S = ∓4.5 V;	
ADG608	±0.5	±2	±0.5	±10	nA max	Test Circuit 3	
ADG609	±0.5	±1	±0.5	±5	nA max		
Channel ON Leakage I _D , I _S (ON)	±0.05		±0.05		nA typ	V _S = V _D = ±4.5 V;	
ADG608	±0.5	±3	±0.5	±20	nA max	Test Circuit 4	
ADG609	±0.5	±1.5	±0.5	±10	nA max		
DIGITAL INPUTS							
Input High Voltage, V _{INH}	2.4		2.4		V min	V _{IN} = 0 or V _{DD}	
Input Low Voltage, V _{INL}	0.8		0.8		V max		
Input Current I _{INL} or I _{INH}	±1		±1		μA max		
C _{IN} , Digital Input Capacitance	5		5		pF typ		
DYNAMIC CHARACTERISTICS²							
t _{TRANSITION}	50 75	90	50 75	100	ns typ ns max	R _L = 300 Ω, C _L = 35 pF; V _{S1} = ±3.5 V, V _{S8} = ∓3.5 V; Test Circuit 5 R _L = 300 Ω, C _L = 35 pF; V _S = +3.5 V; Test Circuit 6 R _L = 300 Ω, C _L = 35 pF; V _S = +3.5 V; Test Circuit 7 R _L = 300 Ω, C _L = 35 pF; V _S = +3.5 V; Test Circuit 7 V _S = 0 V, R _S = 0 Ω, C _L = 1 nF; Test Circuit 8 R _L = 1 kΩ, C _L = 15 pF, f = 100 kHz; V _S = 3 V rms; Test Circuit 9 R _L = 1 kΩ, C _L = 15 pF, f = 100 kHz; Test Circuit 10	
t _{OPEN}	10		10		ns min		
t _{ON} (EN)	50 75	90	50 75	100	ns typ ns max		
t _{OFF} (EN)	30 45	60	30 45	75	ns typ ns max		
Charge Injection	6		6		pC typ		
OFF Isolation	85		85		dB typ		
Channel-to-Channel Crosstalk	85		85		dB typ		
C _S (OFF)	9		9		pF typ		
C _D (OFF)							
ADG608	40		40		pF typ		
ADG609	20		20		pF typ		
C _D (ON)							
ADG608	54		54		pF typ		
ADG609	34		34		pF typ		
POWER REQUIREMENTS							
I _{DD}	0.05 0.2	0.2 2	0.05 0.2	0.2 2	μA typ μA max		V _{IN} = 0 V or V _{DD}
I _{SS}	0.01 0.1	0.1 1	0.01 0.1	0.1 1	μA typ μA max		

NOTES

¹Temperature ranges are as follows: B Version: -40°C to $+85^\circ\text{C}$; T Version: -55°C to $+125^\circ\text{C}$.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SINGLE SUPPLY¹ ($V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted)

Parameter	B Version +25°C −40°C to +85°C		T Version +25°C −55°C to +125°C		Units	Test Conditions/ Comments	
ANALOG SWITCH							
Analog Signal Range	0 to V _{DD}		0 to V _{DD}		V	V _S = +3.5 V, I _S = −1 mA; V _{DD} = +4.5 V; Test Circuit 1 +1 V ≤ V _S ≤ +3 V, I _{DS} = −1 mA; V _{DD} = +5 V V _S = 0 V, I _{DS} = −1 mA; V _{DD} = +5 V	
R _{ON}	40 50		40 50		Ω typ Ω max		
ΔR _{ON}	5	6	5	6	Ω max		
R _{ON} Match	2	3	2	3	Ω max		
LEAKAGE CURRENTS							
Source OFF Leakage I _S (OFF)	±0.05 ±0.5	±2	±0.05 ±0.5	±10	nA typ nA max	V _{DD} = +5.5 V V _D = 4.5 V/0.1 V, V _S = 0.1 V/4.5 V; Test Circuit 2	
Drain OFF Leakage I _D (OFF)	±0.05 ±0.5	±2	±0.05 ±0.5	±10	nA typ nA max	V _D = 4.5 V/0.1 V, V _S = 0.1 V/4.5 V; Test Circuit 3	
ADG608	±0.5	±2	±0.5	±10	nA max		
ADG609	±0.5	±1	±0.5	±5	nA max		
Channel ON Leakage I _D , I _S (ON)	±0.05 ±0.5		±0.05 ±0.5		nA typ nA max	V _S = V _D = 4.5 V/0.1 V; Test Circuit 4	
ADG608	±0.5	±3	±0.5	±20	nA max		
ADG609	±0.5	±1.5	±0.5	±10	nA max		
DIGITAL INPUTS							
Input High Voltage, V _{INH}	2.4		2.4		V min	V _{IN} = 0 or V _{DD}	
Input Low Voltage, V _{INL}	0.8		0.8		V max		
Input Current							
I _{INL} or I _{INH}	±1		±1		μA max		
C _{IN} , Digital Input Capacitance	5		5		pF typ		
DYNAMIC CHARACTERISTICS ²							
t _{TRANSITION}	80 100	130	80 100	150	ns typ ns max	R _L = 300 Ω, C _L = 35 pF; V _{S1} = 3.5 V/0 V, V _{S8} = 0 V/3.5 V; Test Circuit 5 R _L = 300 Ω, C _L = 35 pF; V _S = +3.5 V; Test Circuit 6 R _L = 300 Ω, C _L = 35 pF; V _S = +3.5 V; Test Circuit 7 R _L = 300 Ω, C _L = 35 pF; V _S = +3.5 V; Test Circuit 7 V _S = 0 V, R _S = 0 Ω, C _L = 1 nF; Test Circuit 8 R _L = 1 kΩ, C _L = 15 pF, f = 100 kHz; V _S = 1.5 V rms; Test Circuit 9 R _L = 1 kΩ, C _L = 15 pF, f = 100 kHz; Test Circuit 10	
t _{OPEN}	10		10		ns min		
t _{ON} (EN)	80 100	130	80 100	150	ns typ ns max		
t _{OFF} (EN)	40 50	60	40 50	75	ns typ ns max		
Charge Injection	0.5 3		0.5 3		pC typ pC max		
OFF Isolation	85		85		dB typ		
Channel-to-Channel Crosstalk	85		85		dB typ		
C _S (OFF)	9		9		pF typ		
C _D (OFF)							
ADG608	40		40		pF typ		
ADG609	20		20		pF typ		
C _D (ON)							
ADG608	54		54		pF typ		
ADG609	34		34		pF typ		
POWER REQUIREMENTS							
I _{DD}	0.05 0.2	0.2 2	0.05 0.2	0.2 2	μA typ μA max		V _{IN} = 0 V or V _{DD}

NOTES

¹Temperature ranges are as follows: B Version: -40°C to $+85^\circ\text{C}$; T Version: -55°C to $+125^\circ\text{C}$.

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ADG608/ADG609—SPECIFICATIONS

SINGLE SUPPLY¹ ($V_{DD} = +3.3 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$, $\text{GND} = 0 \text{ V}$, unless otherwise noted)

Parameter	B Version +25°C –40°C to +85°C		T Version +25°C –55°C to +125°C		Units	Test Conditions/ Comments
ANALOG SWITCH						
Analog Signal Range		0 to V _{DD}		0 to V _{DD}	V	
R _{ON}	60		60		Ω typ	V _S = +1.5 V, I _S = –1 mA;
	90	100	90	120	Ω max	V _{DD} = +3 V; Test Circuit 1
R _{ON} Match	3	3	3	3	Ω max	V _S = 0 V, I _{DS} = –1 mA, V _{DD} = +3.3 V
LEAKAGE CURRENTS						
Source OFF Leakage I _S (OFF)	±0.05		±0.05		nA typ	V _{DD} = +3.6 V
	±0.5	±2	±0.5	±10	nA max	V _D = 2.6 V/0.1 V, V _S = 0.1 V/2.6 V;
Drain OFF Leakage I _D (OFF)	±0.05		±0.05		nA typ	Test Circuit 2
ADG608	±0.5	±2	±0.5	±10	nA max	V _D = 2.6 V/0.1 V, V _S = 0.1 V/2.6 V;
ADG609	±0.5	±1	±0.5	±5	nA max	Test Circuit 3
Channel ON Leakage I _D , I _S (ON)	±0.05		±0.05		nA typ	V _S = V _D = 2.6 V/0.1 V;
ADG608	±0.5	±3	±0.5	±20	nA max	Test Circuit 4
ADG609	±0.5	±1.5	±0.5	±10	nA max	
DIGITAL INPUTS						
Input High Voltage, V _{INH}		2.4		2.4	V min	
Input Low Voltage, V _{INL}		0.8		0.8	V max	
Input Current						
I _{INL} or I _{INH}		±1		±1	μA max	V _{IN} = 0 or V _{DD}
C _{IN} , Digital Input Capacitance	5		5		pF typ	
DYNAMIC CHARACTERISTICS²						
t _{TRANSITION}	120		120		ns typ	R _L = 300 Ω, C _L = 35 pF;
	170	225	170	250	ns max	V _{S1} = 1.5 V/0 V, V _{S8} = 0 V/1.5 V;
						Test Circuit 5
t _{OPEN}	10		10		ns min	R _L = 300 Ω, C _L = 35 pF;
						V _S = +1.5 V; Test Circuit 6
t _{ON} (EN)	120		120		ns typ	R _L = 300 Ω, C _L = 35 pF;
	170	225	170	250	ns max	V _S = +1.5 V; Test Circuit 7
t _{OFF} (EN)	40		40		ns typ	R _L = 300 Ω, C _L = 35 pF;
	60	75	60	90	ns max	V _S = +1.5 V; Test Circuit 7
Charge Injection	0.5		0.5		pC typ	V _S = 0 V, R _S = 0 Ω, C _L = 1 nF;
	3		3		pC max	Test Circuit 8
OFF Isolation	85		85		dB typ	R _L = 1 kΩ, C _L = 15 pF, f = 100 kHz;
						V _S = 1 V rms; Test Circuit 9
Channel-to-Channel Crosstalk	85		85		dB typ	R _L = 1 kΩ, C _L = 15 pF, f = 100 kHz;
						Test Circuit 10
C _S (OFF)	9		9		pF typ	
C _D (OFF)						
ADG608	40		40		pF typ	
ADG609	20		20		pF typ	
C _D (ON)						
ADG608	54		54		pF typ	
ADG609	34		34		pF typ	
POWER REQUIREMENTS						
I _{DD}	0.05	0.2	0.05	0.2	μA typ	V _{IN} = 0 V or V _{DD}
	0.2	2	0.2	2	μA max	

NOTES

¹Temperature ranges are as follows: B Version: –40°C to +85°C; T Version: –55°C to +125°C.

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ABSOLUTE MAXIMUM RATINGS¹(T_A = +25°C unless otherwise noted)

V _{DD} to V _{SS}	+13 V
V _{DD} to GND	–0.3 V to +6.5 V
V _{SS} to GND	+0.3 V to –6.5 V
Analog, Digital Inputs ²	–0.3 V to V _{DD} + 2 V or 20 mA, Whichever Occurs First
Continuous Current, S or D	20 mA
Peak Current, S or D	(Pulsed at 1 ms, 10% Duty Cycle Max) 40 mA
Operating Temperature Range	
Industrial (B Version)	–40°C to +85°C
Extended (T Version)	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
Plastic DIP Package	
θ _{JA} , Thermal Impedance	117°C/W
Lead Temperature, Soldering (10 sec)	+260°C

SOIC Package

θ _{JA} , Thermal Impedance	77°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

TSSOP Package

θ _{JA} , Thermal Impedance	158°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

ESD Rating >5000 V

NOTES

¹Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at A, S, D or EN will be clamped by internal diodes. Current should be limited to the maximum ratings given.

Table I. ADG608 Truth Table

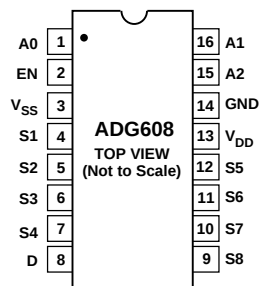
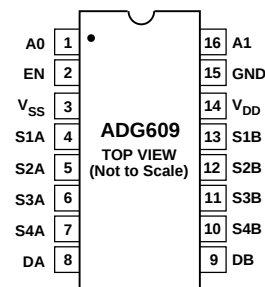
A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

Table II. ADG609 Truth Table

A1	A0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

X = Don't Care

PIN CONFIGURATIONS**DIP/SOIC/TSSOP****DIP/SOIC/TSSOP**

ADG608/ADG609—Typical Performance Characteristics

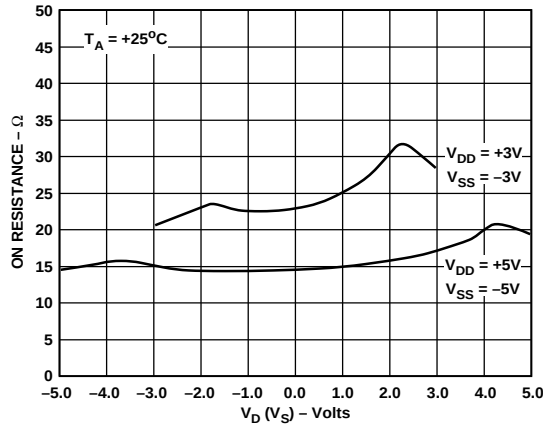


Figure 1. R_{ON} as a Function of V_D (V_S): Dual Supply Voltage

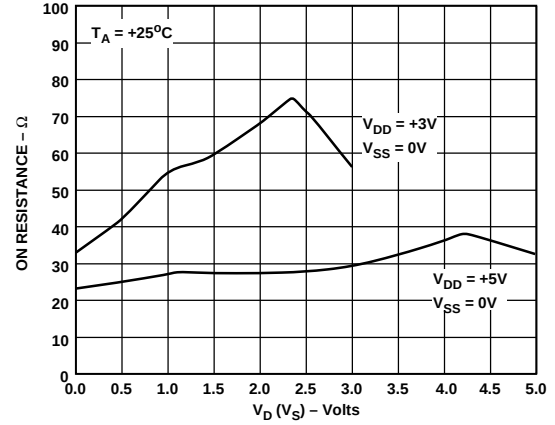


Figure 4. R_{ON} as a Function of V_D (V_S): Single Supply Voltage

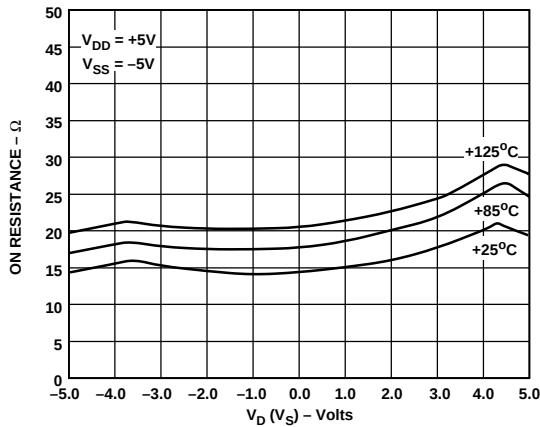


Figure 2. R_{ON} as a Function of V_D (V_S) for Different Temperatures

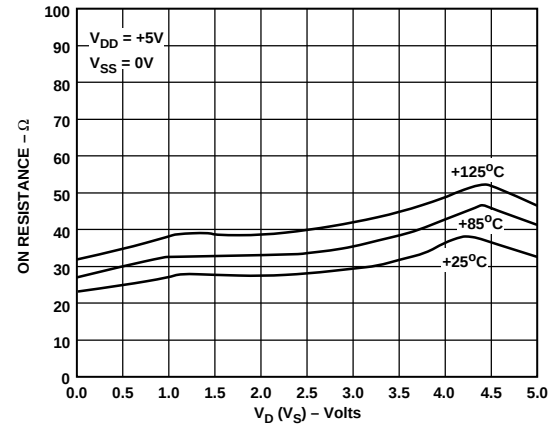


Figure 5. R_{ON} as a Function of V_D (V_S) for Different Temperatures

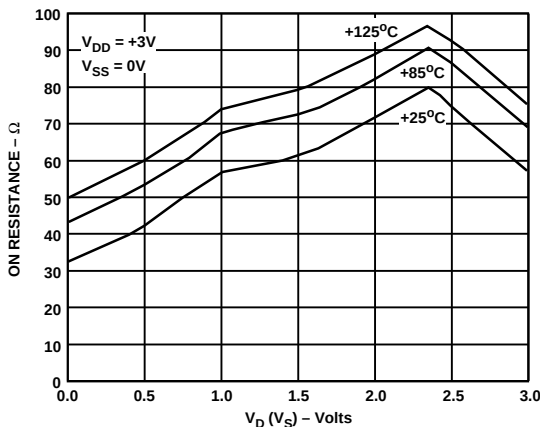


Figure 3. R_{ON} as a Function of V_D (V_S) for Different Temperatures

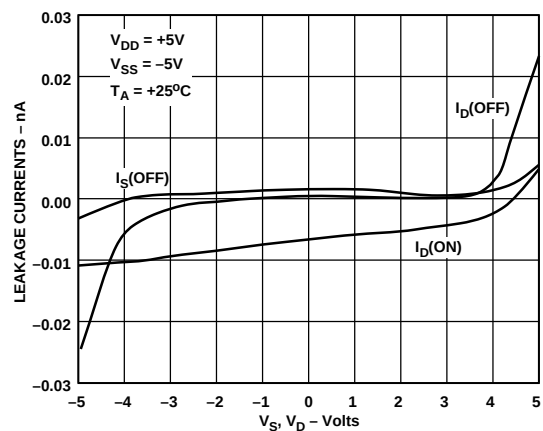


Figure 6. Leakage Currents as a Function of V_D (V_S)

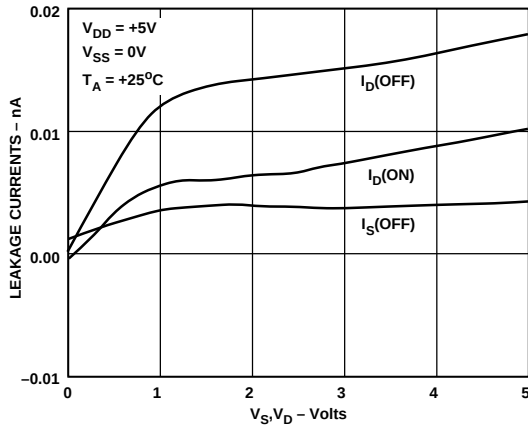


Figure 7. Leakage Currents as a Function of V_D (V_S)

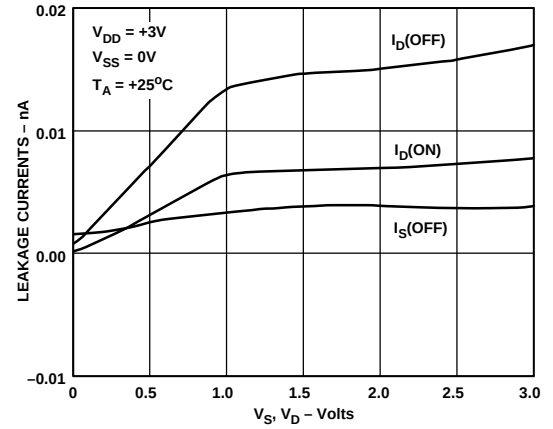


Figure 10. Leakage Currents as a Function of V_D (V_S)

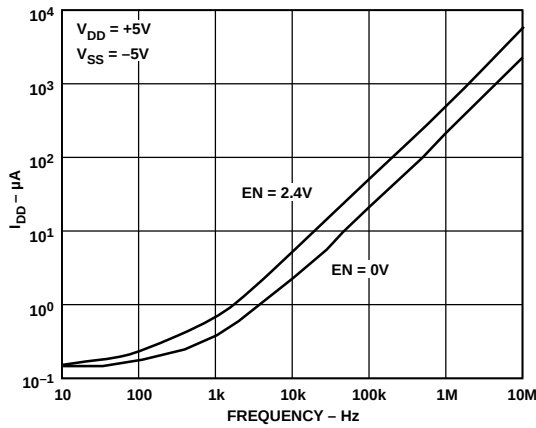


Figure 8. Positive Supply Current vs. Switching Frequency

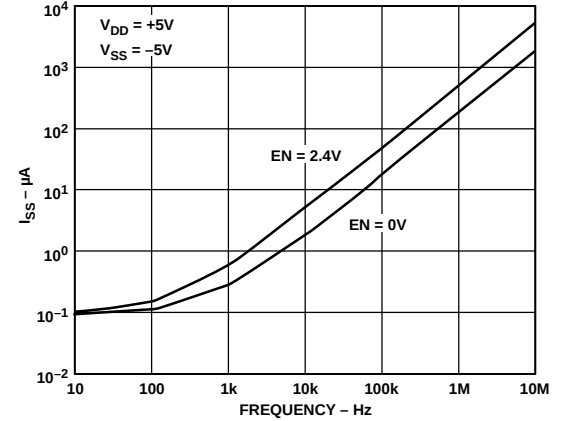


Figure 11. Negative Supply Current vs. Switching Frequency

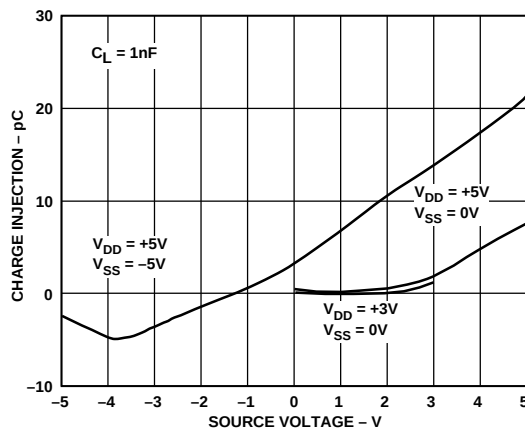


Figure 9. Charge Injection vs. Analog Voltage V_S

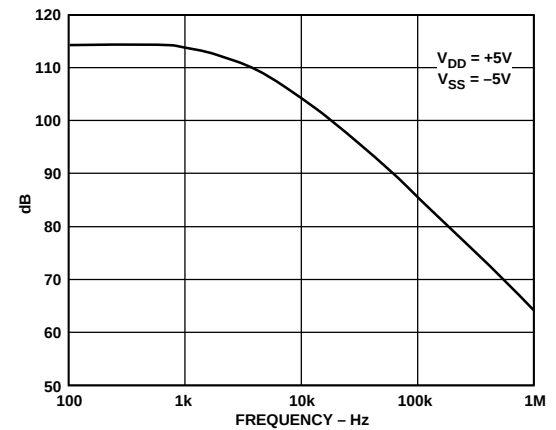
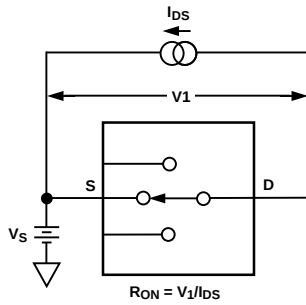


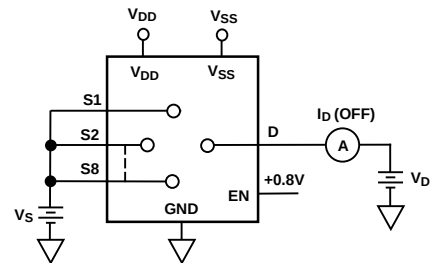
Figure 12. Crosstalk and Off Isolation vs. Frequency

ADG608/ADG609

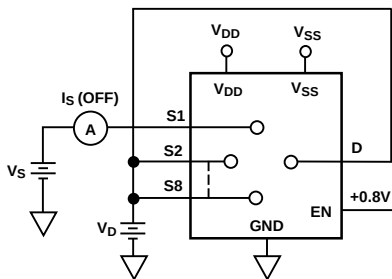
Test Circuits



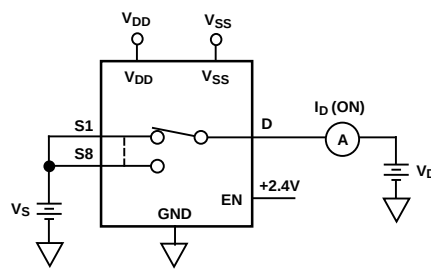
Test Circuit 1. On Resistance



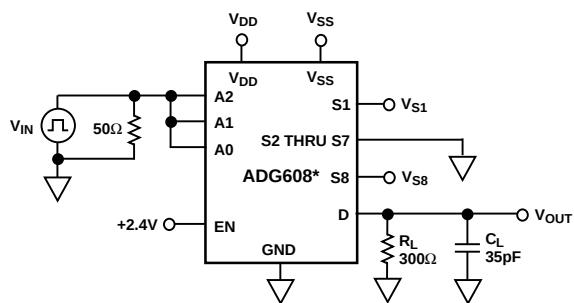
Test Circuit 3. I_D (OFF)



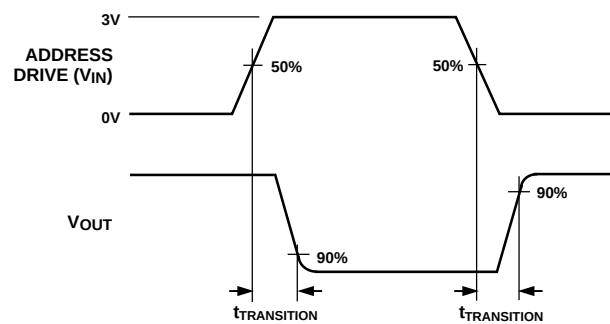
Test Circuit 2. I_S (OFF)

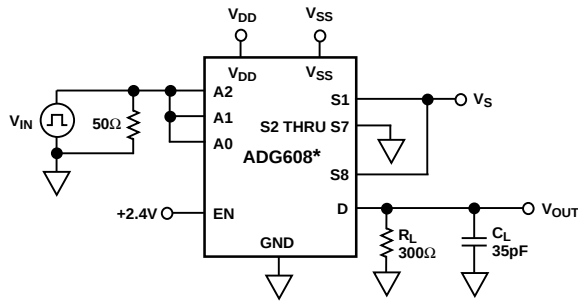


Test Circuit 4. I_D (ON)

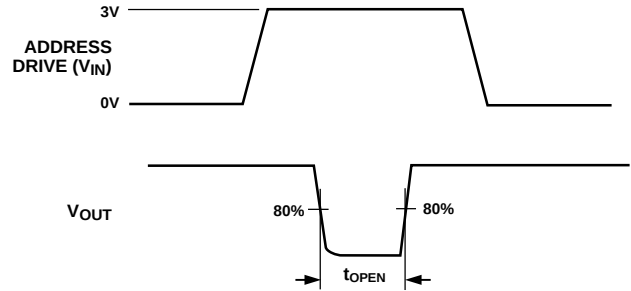


Test Circuit 5. Switching Time of Multiplexer, $t_{\text{TRANSITION}}$

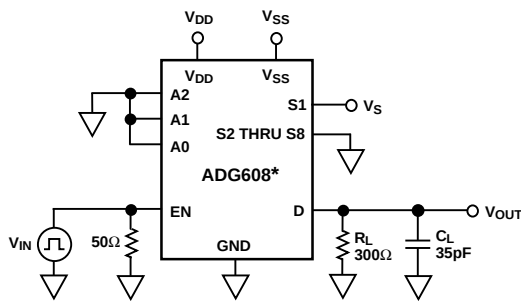




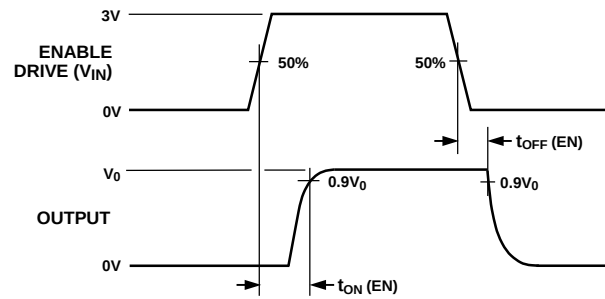
* SIMILAR CONNECTION FOR ADG609



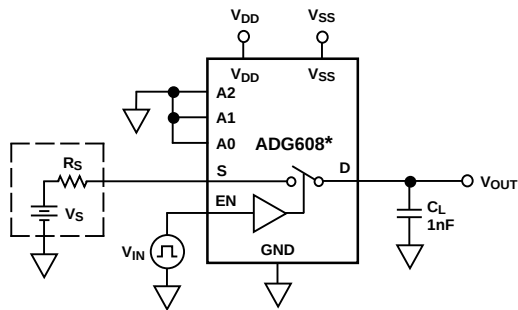
Test Circuit 6. Break-Before-Make Delay, t_{OPEN}



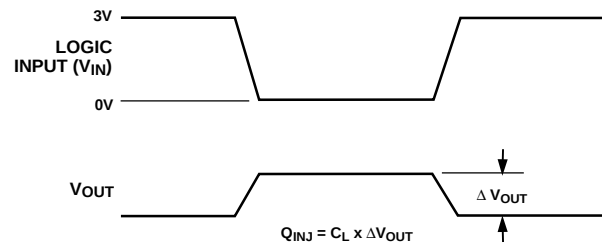
* SIMILAR CONNECTION FOR ADG609



Test Circuit 7. Enable Delay, $t_{ON} (EN)$, $t_{OFF} (EN)$

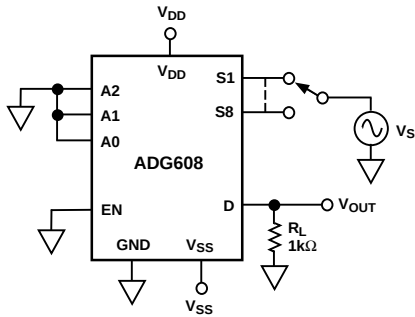


* SIMILAR CONNECTION FOR ADG609

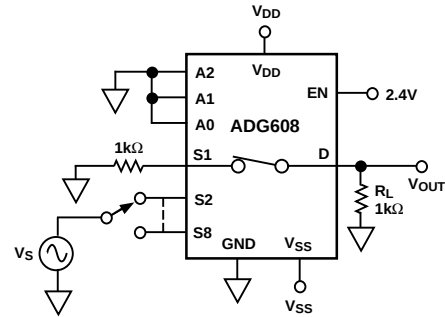


Test Circuit 8. Charge Injection

ADG608/ADG609



Test Circuit 9. OFF Isolation



Test Circuit 10. Channel-to-Channel Crosstalk

TERMINOLOGY

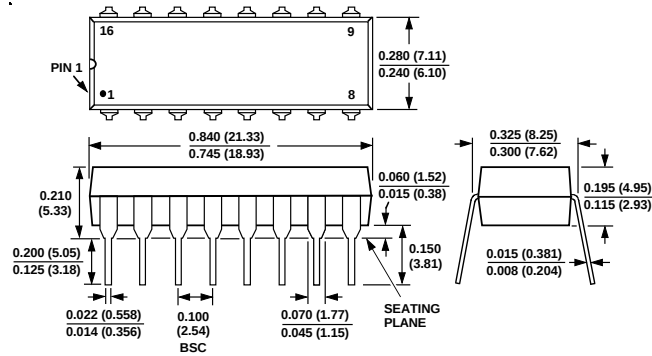
V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to ground.
GND	Ground (0 V) reference.
R_{ON}	Ohmic resistance between D and S.
ΔR_{ON}	R_{ON} variation due to a change in the analog input voltage with a constant load current.
R_{ON} Match	Difference between the R_{ON} of any two channels.
I_S (OFF)	Source leakage current when the switch is off.
I_D (OFF)	Drain leakage current when the switch is off.
I_D, I_S (ON)	Channel leakage current when the switch is on.
V_D, V_S	Analog voltage on terminals D, S.
C_S (OFF)	Channel input capacitance for “OFF” condition.
C_D (OFF)	Channel output capacitance for “OFF” condition.
C_D, C_S (ON)	“ON” switch capacitance.
C_{IN}	Digital input capacitance.
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch “ON” condition.

t_{OFF} (EN)	Delay time between the 50% and 90% points of the digital input and switch “OFF” condition.
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and the switch “ON” condition when switching from one address state to another.
t_{OPEN}	“OFF” time measured between the 80% points of both switches when switching from one address state to another.
V_{INL}	Maximum input voltage for logic “0.”
V_{INH}	Minimum input voltage for logic “1.”
I_{INL} (I_{INH})	Input current of the digital input.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an “OFF” channel.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
I_{DD}	Positive supply current.
I_{SS}	Negative supply current.

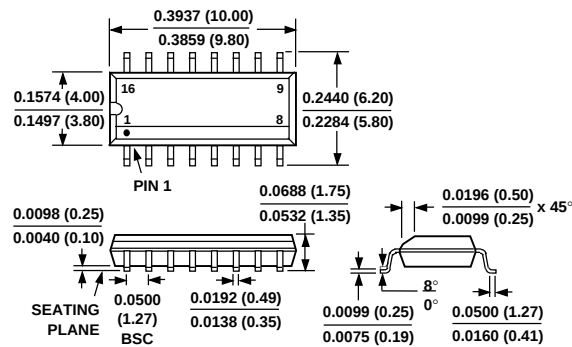
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Pin Plastic (N-16)



16-Pin SOIC (R-16A)



16-Pin TSSOP (RU-16)

