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- UG-476: PLL Software Installation Guide

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- ADF4156 FMC-SDP Interposer & Evaluation Board / Xilinx KC705 Reference Design
- BeMicro FPGA Project for ADF4156 with Nios driver

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- ADIsimRF

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- CN0174

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- RF, Microwave, and Millimeter Wave IC Selection Guide 2017

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5/06—Revision 0: Initial Version

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SPECIFICATIONS

AV_{DD} = DV_{DD} = 2.7 V to 3.3 V, V_P = AV_{DD} to 5.5 V, AGND = DGND = 0 V, T_A = T_{MIN} to T_{MAX}, dBm referred to 50 Ω, unless otherwise noted.

Table 1.

Parameter	B Version	Unit	Test Conditions/Comments[1]
RF CHARACTERISTICS			
RF Input Frequency (RF_{IN})	0.5/6.2	GHz min/max	−10 dBm min to 0 dBm max. For lower frequencies, ensure slew rate (SR) > 400 V/µs.
REFERENCE CHARACTERISTICS			
REF_{IN} Input Frequency	10/250	MHz min/max	For f < 10 MHz, use a dc-coupled CMOS-compatible square wave, slew rate > 25 V/µs.
REF_{IN} Input Sensitivity	0.4/AV_{DD}	V p-p min/max	Biased at AV_{DD}/2.[2]
REF_{IN} Input Capacitance	10	pF max	
REF_{IN} Input Current	±100	µA max	
PHASE DETECTOR			
Phase Detector Frequency[3]	32	MHz max	
CHARGE PUMP			
I_{CP} Sink/Source			Programmable.
High Value	5	mA typ	With R_{SET} = 5.1 kΩ.
Low Value	312.5	µA typ	
Absolute Accuracy	2.5	% typ	With R_{SET} = 5.1 kΩ.
R_{SET} Range	2.7/10	kΩ min/max	
I_{CP} Three-State Leakage Current	1	nA typ	Sink and source current.
Matching	2	% typ	0.5 V < V_{CP} < V_P − 0.5.
I_{CP} vs. V_{CP}	2	% typ	0.5 V < V_{CP} < V_P − 0.5.
I_{CP} vs. Temperature	2	% typ	V_{CP} = V_P/2.
LOGIC INPUTS			
V_{INH}, Input High Voltage	1.4	V min	
V_{INL}, Input Low Voltage	0.6	V max	
I_{INH}/I_{INL}, Input Current	±1	µA max	
C_{IN}, Input Capacitance	10	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	1.4	V min	Open-drain output chosen; 1 kΩ pull-up to 1.8 V.
V_{OH}, Output High Voltage	V_{DD} − 0.4	V min	CMOS output chosen.
I_{OH}, Output High Current	100	µA max	
V_{OL}, Output Low Voltage	0.4	V max	I_{OL} = 500 µA.
POWER SUPPLIES			
AV_{DD}	2.7/3.3	V min/max	
DV_{DD}	AV_{DD}		
V_P	AV_{DD}/5.5	V min/max	
I_{DD}	32	mA max	26 mA typical.
Low Power Sleep Mode	1	µA typ	
NOISE CHARACTERISTICS			
Normalized Phase Noise Floor (PN_{SYNTH})[4]	−220	dBc/Hz typ	PLL loop BW = 500 kHz. Measured at 100 kHz offset.
Normalized 1/f Noise (PN_{1_f})[5]	−110	dBc/Hz typ	10 kHz offset; normalized to 1 GHz.
Phase Noise Performance[6]			At VCO output.
5800 MHz Output[7]	−89	dBc/Hz typ	At 5 kHz offset, 25 MHz PFD frequency.

[1] Operating temperature for B version: −40°C to +85°C.
[2] AC coupling ensures AV_{DD}/2 bias.
[3] Guaranteed by design. Sample tested to ensure compliance.
[4] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log(N) (where N is the N divider value) and 10 log(F_{PFD}). PN_{SYNTH} = PN_{TOT} − 10 log(F_{PFD}) − 20 log(N).
[5] The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency, F_{RF}, and at a frequency offset f is given by PN = PN_{1_f} + 10 log(10 kHz/f) + 20 log(F_{RF}/1 GHz). Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL.
[6] The phase noise is measured with the EV-ADF4156SD1Z evaluation board and the Agilent E5500 phase noise system.
[7] f_{REFIN} = 100 MHz, f_{PFD} = 25 MHz, offset frequency = 5 kHz, RF_{OUT} = 5800 MHz, N = 232, loop bandwidth = 20 kHz, I_{CP} = 313 µA, and lowest noise mode.

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TIMING SPECIFICATIONS

AV_{DD} = DV_{DD} = 2.7 V to 3.3 V, V_P = AV_{DD} to 5.5 V, AGND = DGND = 0 V, T_A = T_{MIN} to T_{MAX}, dBm referred to 50 Ω, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	20	ns min	LE setup time
t_2	10	ns min	DATA to CLOCK setup time
t_3	10	ns min	DATA to CLOCK hold time
t_4	25	ns min	CLOCK high duration
t_5	25	ns min	CLOCK low duration
t_6	10	ns min	CLOCK to LE setup time
t_7	20	ns min	LE pulse width

Timing Diagram

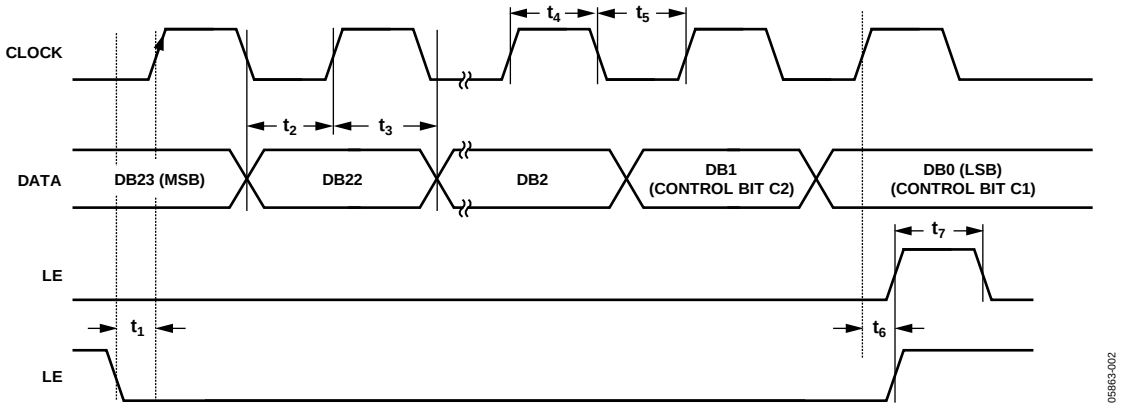

Figure 2. Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, GND = AGND = DGND = 0 V, V_{DD} = AV_{DD} = DV_{DD}, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +4 V
V_{DD} to V_{DD}	−0.3 V to +0.3 V
V_P to GND	−0.3 V to +5.8 V
V_P to V_{DD}	−0.3 V to +5.8 V
Digital I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
REF_{IN}, RF_{IN} to GND	−0.3 V to V_{DD} + 0.3 V
$RF_{IN}A$ to $RF_{IN}B$	±600 mV
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
Maximum Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

THERMAL IMPEDANCE

Table 4. Thermal Impedance

Package Type	θ_{JA}	Unit
TSSOP	112	°C/W
LFCSP_VQ (Paddle Soldered)	30.4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

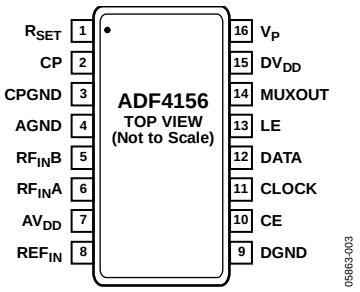

Figure 3. TSSOP Pin Configuration

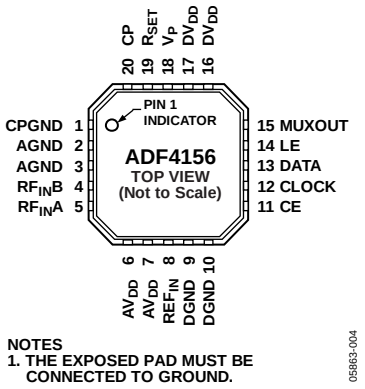

Figure 4. LFCSP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	19	R_{SET}	Connecting a resistor between this pin and ground sets the maximum charge-pump output current. The relationship between I_{CP} and R_{SET} is $I_{CPmax} = \frac{25.5}{R_{SET}}$ where R_{SET} = 5.1 kΩ and I_{CPmax} = 5 mA.
2	20	CP	Charge-Pump Output. When enabled, this pin provides ±I_{CP} to the external loop filter, which in turn drives the external VCO.
3	1	CPGND	Charge-Pump Ground. This is the ground return path for the charge pump.
4	2, 3	AGND	Analog Ground. This is the ground return path of the prescaler.
5	4	$RF_{IN}B$	Complementary Input to the RF Prescaler. Decouple this point to the ground plane with a small bypass capacitor, typically 100 pF.
6	5	$RF_{IN}A$	Input to the RF Prescaler. This small-signal input is normally ac-coupled from the VCO.
7	6, 7	AV_{DD}	Positive Power Supply for the RF Section. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. AV_{DD} has a value of 3 V ± 10%. AV_{DD} must have the same voltage as DV_{DD}.
8	8	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of V_{DD}/2 and an equivalent input resistance of 100 kΩ. This input can be driven from a TTL or CMOS crystal oscillator, or it can be ac-coupled.
9	9, 10	DGND	Digital Ground.
10	11	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge-pump output into three-state mode.
11	12	CLOCK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the shift register on the CLOCK rising edge. This input is a high impedance CMOS input.
12	13	DATA	Serial Data Input. The serial data is loaded MSB first with the three LSBs serving as the control bits. This input is a high impedance CMOS input.
13	14	LE	Load Enable, CMOS Input. When LE is high, the data stored in the shift registers is loaded into one of the five latches. The control bits are used to select the latch.
14	15	MUXOUT	Multiplexer Output. This multiplexer output allows either the RF lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
15	16, 17	DV_{DD}	Positive Power Supply for the Digital Section. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV_{DD} has a value of 3 V ± 10%. DV_{DD} must have the same voltage as AV_{DD}.
16	18	V_P	Charge-Pump Power Supply. This should be greater than or equal to V_{DD}. In systems where V_{DD} is 3 V, it can be set to 5.5 V and used to drive a VCO with a tuning range of up to 5.5 V.
		EPAD	The exposed pad must be connected to ground.

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TYPICAL PERFORMANCE CHARACTERISTICS

PFD = 25 MHz, loop bandwidth = 20 kHz, reference = 100 MHz, I_{CP} = 313 µA, phase noise measurements taken on the Agilent E5500 phase noise system.

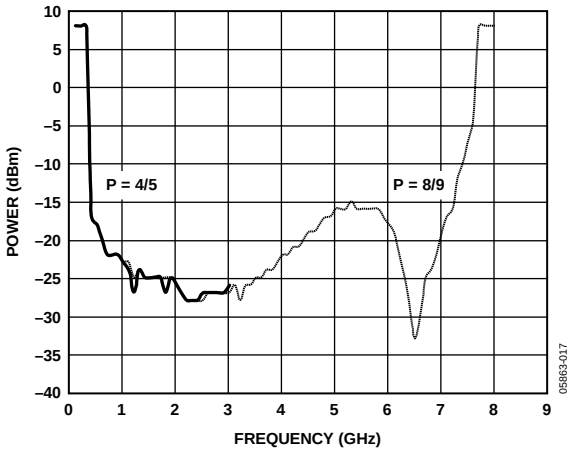

Figure 5. RF Input Sensitivity

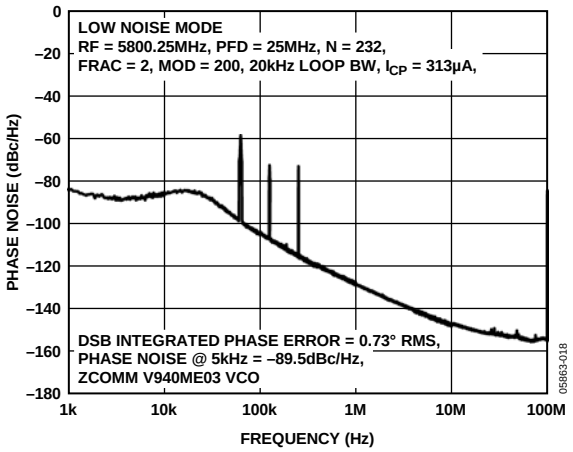

Figure 6. Phase Noise and Spurs, Low Noise Mode

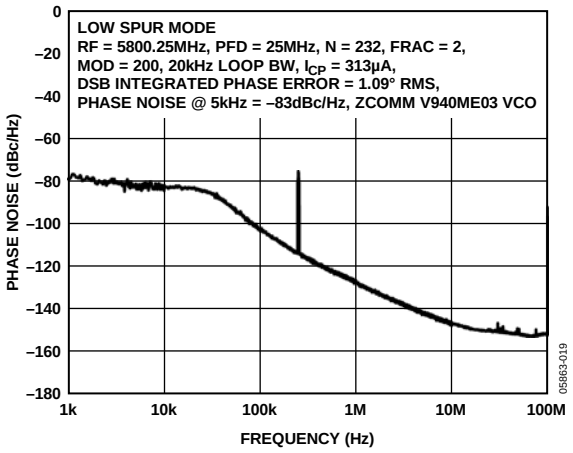

Figure 7. Phase Noise and Spurs, Low Spur Mode
(Note that Fractional Spurs Are Removed and Only
the Integer Boundary Spur Remains in Low Spur Mode)

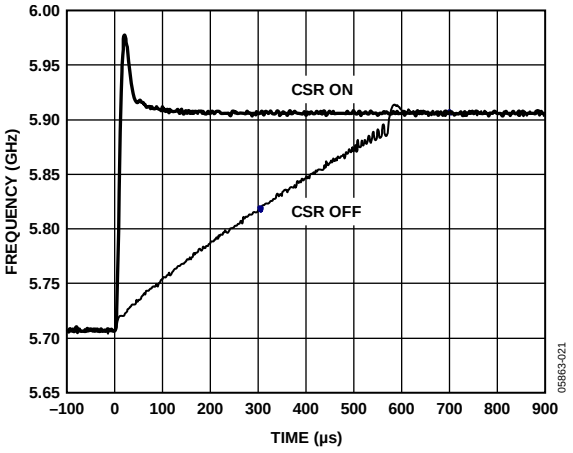

Figure 8. Lock Time for 200 MHz Jump, from 5705 MHz to 5905 MHz, with CSR On and Off

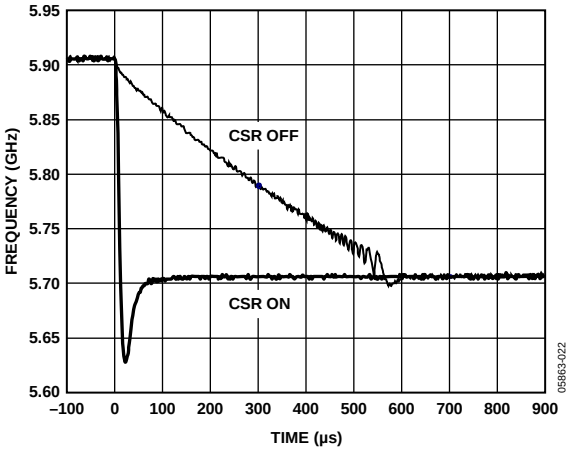

Figure 9. Lock Time for 200 MHz Jump, from 5905 MHz to 5705 MHz, with CSR On and Off

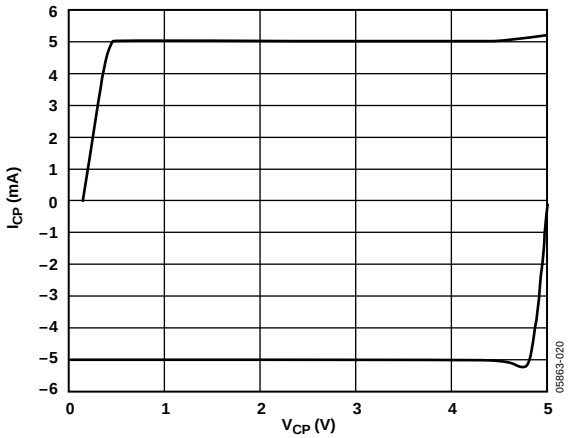

Figure 10. Charge-Pump Output Characteristics

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CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 11. While the device is operating, SW1 and SW2 are usually closed switches and SW3 is open. When a power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that the REF_{IN} pin is not loaded while the device is powered down.

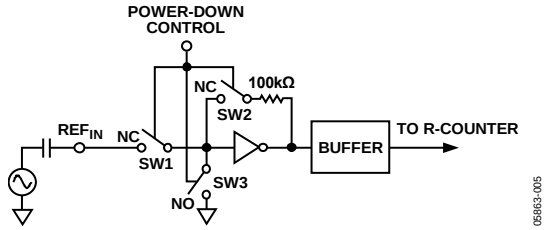

Figure 11. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 12. It is followed by a two-stage limiting amplifier to generate the current-mode logic (CML) clock levels needed for the prescaler.

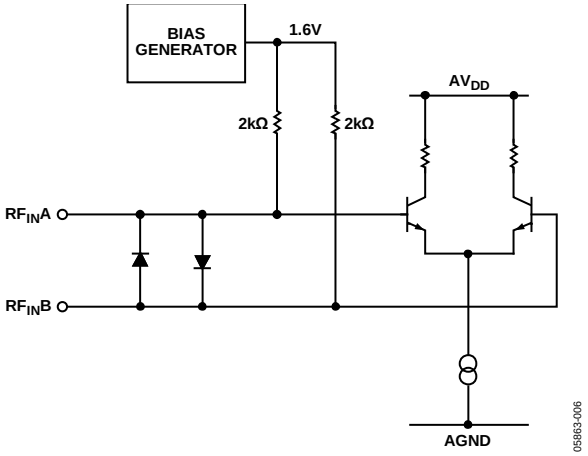

Figure 12. RF Input Stage

RF INT DIVIDER

The RF INT counter allows a division ratio in the PLL feedback counter. Division ratios from 23 to 4095 are allowed.

INT, FRAC, MOD, AND R RELATIONSHIP

The INT, FRAC, and MOD values, in conjunction with the R-counter, enable generating output frequencies that are spaced by fractions of the phase frequency detector (PFD). See the RF Synthesizer: A Worked Example section for more information. The RF VCO frequency (RF_{OUT}) equation is

$$RF_{OUT} = F_{PFD} \times (INT + (FRAC/MOD)) \quad (1)$$

where RF_{OUT} is the output frequency of an external voltage-controlled oscillator (VCO).

$$F_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (2)$$

where:
REF_{IN} is the reference input frequency.
D is the REF_{IN} doubler bit.
T is the REF_{IN} divide-by-2 bit (0 or 1).
R is the preset divide ratio of the binary 5-bit programmable reference counter (1 to 32).
INT is the preset divide ratio of the binary 12-bit counter (23 to 4095).
MOD is the preset fractional modulus (2 to 4095).
$FRAC$ is the numerator of the fractional division (0 to MOD − 1).

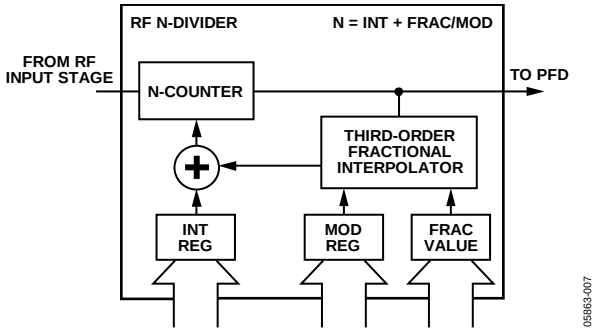

Figure 13. RF INT Divider

RF R-COUNTER

The 5-bit RF R-counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 32 are allowed.

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PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R-counter and N-counter and produces an output proportional to the phase and frequency difference between them. Figure 14 is a simplified schematic of the phase frequency detector. The PFD includes a fixed-delay element that sets the width of the antibacklash pulse, which is typically 3 ns. This pulse ensures that there is no dead zone in the PFD transfer function and results in a consistent reference spur level.

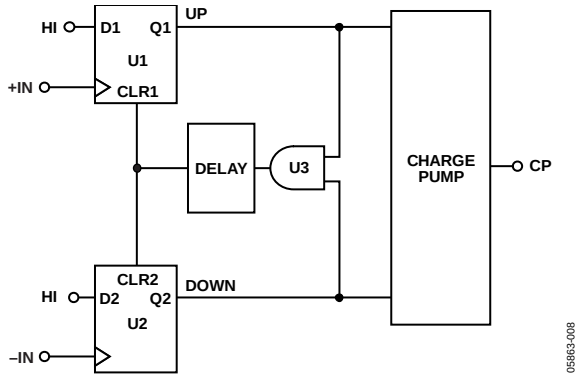

Figure 14. PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4156 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M4, M3, M2, and M1 (for details, see Figure 16). Figure 15 shows the MUXOUT section in block diagram form.

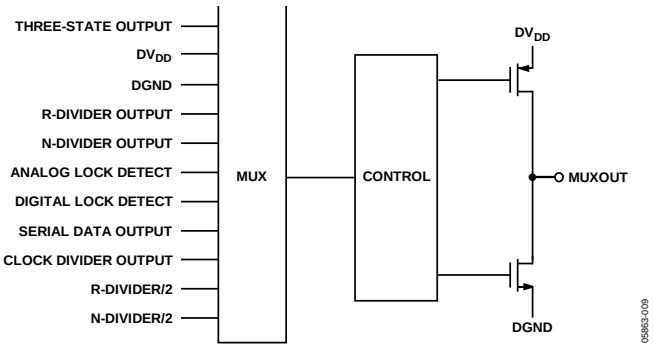

Figure 15. MUXOUT Schematic

INPUT SHIFT REGISTERS

The ADF4156 digital section includes a 5-bit RF R-counter, a 12-bit RF N-counter, a 12-bit FRAC counter, and a 12-bit modulus counter. Data is clocked into the 32-bit shift register on each rising edge of CLOCK. The data is clocked in MSB first. Data is transferred from the shift register to one of five latches on the rising edge of LE. The destination latch is determined by the state of the three control bits (C3, C2, and C1) in the shift register. These bits are the three LSBs (DB2, DB1, and DB0), as shown in Figure 2. The truth table for these bits is shown in Table 6. Figure 16 shows a summary of how the latches are programmed.

PROGRAM MODES

Table 6 and Figure 16 through Figure 21 show how to set up the program modes in the ADF4156.

Several settings in the ADF4156 are double buffered, including the modulus value, phase value, R-counter value, reference doubler, reference divide-by-2, and current setting. This means that two events must occur before the part can use a new value for any of the double buffered settings. The new value must first be latched into the device by writing to the appropriate register, and then a new write must be performed on Register R0. For example, after the modulus value is updated, Register R0 must be written to in order to ensure that the modulus value is loaded correctly.

Table 6. C3, C2, and C1 Truth Table

Control Bits			
C3	**C2**	**C1**	**Register**
0	0	0	Register R0
0	0	1	Register R1
0	1	0	Register R2
0	1	1	Register R3
1	0	0	Register R4

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REGISTER MAPS

FRAC/INT REGISTER (R0)

RE-SERVED	MUXOUT CONTROL				12-BIT INTEGER VALUE (INT)												12-BIT FRACTIONAL VALUE (FRAC)												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	M4	M3	M2	M1	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C3(0)	C2(0)	C1(0)

PHASE REGISTER (R1)

RESERVED																	12-BIT PHASE VALUE (PHASE)[1]												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	C3(0)	C2(0)	C1(1)

MOD/R REGISTER (R2)

RESERVED	NOISE MODE		CSR EN	CURRENT SETTING[1]				RESERVED	PRESCALER	RDIV2[1]	REFERENCE DOUBLER[1]	5-BIT R COUNTER[1]					12-BIT MODULUS WORD[1]												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	L2	L1	C1	CPI4	CPI3	CPI2	CPI1	0	P1	U2	U1	R5	R4	R3	R2	R1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C3(0)	C2(1)	C1(0)

FUNCTION REGISTER (R3)

RESERVED																	Σ-Δ RESET	RESERVED						LDP	PD POLARITY	PD	CP THREE-STATE	COUNTER RESET	CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	U12	0	0	0	0	0	0	U7	U6	U5	U4	U3	C3(0)	C2(1)	C1(1)

CLK DIV REGISTER (R4)

RESERVED											CLK DIV MODE		12-BIT CLOCK DIVIDER VALUE												RESERVED				CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	M2	M1	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	0	0	0	0	C3(1)	C2(0)	C1(0)

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[1]DOUBLE BUFFERED BIT.

Figure 16. Register Summary

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FRAC/INT REGISTER, R0

With the control bits (Bits[2:0]) of Register R0 set to 000, the on-chip FRAC/INT register is programmed. Figure 17 shows the input data format for programming this register.

12-Bit Integer Value (INT)

These 12 bits control what is loaded as the INT value. This determines the overall feedback division factor. It is used in Equation 1 (see the INT, FRAC, MOD, and R Relationship section).

12-Bit Fractional Value (FRAC)

These 12 bits control what is loaded as the FRAC value into the fractional interpolator. This is part of what determines the overall feedback division factor. It is also used in Equation 1. The FRAC value must be less than the value loaded into the MOD register.

MUXOUT

The on-chip multiplexer is controlled by DB30, DB29, DB28, and DB27 on the ADF4156. See Figure 17 for the truth table.

RE-SERVED	MUXOUT CONTROL				12-BIT INTEGER VALUE (INT)												12-BIT FRACTIONAL VALUE (FRAC)												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	M4	M3	M2	M1	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C3(0)	C2(0)	C1(0)

M4	M3	M2	M1	OUTPUT
0	0	0	0	THREE-STATE OUTPUT
0	0	0	1	DV_{DD}
0	0	1	0	DGND
0	0	1	1	R-DIVIDER OUTPUT
0	1	0	0	N-DIVIDER OUTPUT
0	1	0	1	ANALOG LOCK DETECT
0	1	1	0	DIGITAL LOCK DETECT
0	1	1	1	SERIAL DATA OUTPUT
1	0	0	0	RESERVED
1	0	0	1	RESERVED
1	0	1	0	CLOCK DIVIDER
1	0	1	1	RESERVED
1	1	0	0	FAST-LOCK SWITCH
1	1	0	1	R-DIVIDER/2
1	1	1	0	N-DIVIDER/2
1	1	1	1	RESERVED

F12	F11	.....	F2	F1	FRACTIONAL VALUE (FRAC)
0	0	.....	0	0	0
0	0	.....	0	1	1
0	0	.....	1	0	2
0	0	.....	1	1	3
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	4092
1	1	.....	0	1	4093
1	1	.....	1	0	4094
1	1	.....	1	1	4095

N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	INTEGER VALUE (INT)
0	0	0	0	0	0	0	1	0	1	1	1	23
0	0	0	0	0	0	0	1	1	0	0	0	24
0	0	0	0	0	0	0	1	1	0	0	1	25
0	0	0	0	0	0	0	1	1	0	1	0	26
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	0	1	4093
1	1	1	1	1	1	1	1	1	1	1	0	4094
1	1	1	1	1	1	1	1	1	1	1	1	4095

05663-011

Figure 17. FRAC/INT Register (R0) Map

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PHASE REGISTER, R1

With the control bits (Bits[2:0]) of Register R1 set to 001, the on-chip phase register is programmed. Figure 18 shows the input data format for programming this register.

12-Bit Phase Value

These 12 bits control what is loaded as the phase word. The word must be less than the MOD value programmed in the MOD/R register (R2). The word is used to program the RF output phase from 0° to 360° with a resolution of 360°/MOD.

See the Phase Resync section for more information. In most applications, the phase relationship between the RF signal and the reference is not important. In such applications, the phase value can be used to optimize the fractional and subfractional spur levels. See the Spur Consistency and Fractional Spur Optimization section for more information.

If neither the phase resync nor the spurious optimization functions are being used, it is recommended that the phase value be set to 1.

RESERVED																	12-BIT PHASE VALUE (PHASE)												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	C3(0)	C2(0)	C1(1)

P12	P11	.....	P2	P1	PHASE VALUE (PHASE)
0	0	.....	0	0	0
0	0	.....	0	1	1 (RECOMMENDED)
0	0	.....	1	0	2
0	0	.....	1	1	3
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	4092
1	1	.....	0	1	4093
1	1	.....	1	0	4094
1	1	.....	1	1	4095

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Figure 18. Phase Register (R1) Map

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MOD/R REGISTER, R2

With the control bits (Bits[2:0]) of Register R1 set to 010, the on-chip MOD/R register is programmed. Figure 19 shows the input data format for programming this register.

Noise and Spur Mode

The noise modes on the ADF4156 are controlled by DB30 and DB29 in the MOD/R register. See Figure 19 for the truth table. The noise modes allow the user to optimize a design either for improved spurious performance or for improved phase noise performance.

When the lowest spur setting is chosen, dither is enabled. This randomizes the fractional quantization noise so that it resembles white noise, rather than spurious noise. As a result, the part is optimized for improved spurious performance. This operation is typically used when the PLL closed-loop bandwidth is wide for fast-locking applications. Wide loop bandwidth is defined as a loop bandwidth greater than 1/10 of the RF_{OUT} channel step resolution (f_{RES}). A wide loop filter does not attenuate the spurs to the same level as a narrow loop bandwidth.

For best noise performance, use the lowest noise setting option. As well as disabling the dither, using the lowest noise setting ensures that the charge pump is operating in an optimum region for noise performance. This setting is useful if a narrow loop filter bandwidth is available. The synthesizer ensures extremely low noise, and the filter attenuates the spurs. The typical performance characteristics show the trade-offs in a typical WCDMA setup for various noise and spur settings.

CSR Enable

Setting this bit to 1 enables cycle slip reduction, which can improve lock times. Note that the signal at the phase frequency detector (PFD) must have a 50% duty cycle for cycle slip reduction to work. The charge-pump current setting must also be set to a minimum value. See the Fast Lock Times section for more information. Note that CSR cannot be used if the phase detector polarity is set to negative.

Charge-Pump Current Setting

DB[27:24] set the charge-pump current setting. These bits should be set to the charge-pump current as indicated by the loop filter design (see Figure 19).

Prescaler (P/P + 1)

The dual-modulus prescaler (P/P + 1), along with the INT, FRAC, and MOD counters, determines the overall division ratio from the RF_{IN} to the PFD input.

Operating at CML levels, the prescaler uses the clock from the RF input stage and divides it down for the counters. The prescaler is based on a synchronous 4/5 core. When it is set to 4/5, the maximum RF frequency allowed is 3 GHz. Therefore, when operating the ADF4156 with frequencies greater than 3 GHz, the prescaler must be set to 8/9. The prescaler limits the INT value as follows:

With $P = 4/5$, $N_{MIN} = 23$
With $P = 8/9$, $N_{MIN} = 75$

RDIV/2

Setting this bit to 1 inserts a divide-by-2 toggle flip-flop between the R-counter and PFD, which extends the maximum REF_{IN} input rate.

Reference Doubler

Setting DB20 to 0 feeds the REF_{IN} signal directly into the 5-bit RF R-counter, disabling the doubler. Setting this bit to 1 multiplies the REF_{IN} frequency by a factor of 2 before feeding it into the 5-bit R-counter. When the doubler is disabled, the REF_{IN} falling edge is the active edge at the PFD input to the fractional synthesizer. When the doubler is enabled, both the rising and falling edges of REF_{IN} become active edges at the PFD input.

When the doubler is enabled and the lowest spur mode is chosen, the in-band phase noise performance is sensitive to the REF_{IN} duty cycle. The phase noise degradation can be as much as 5 dB for REF_{IN} duty cycles that are outside a 45% to 55% range. The phase noise is insensitive to the REF_{IN} duty cycle when the device is in the lowest noise mode and when the doubler is disabled. The maximum allowable REF_{IN} frequency when the doubler is enabled is 30 MHz.

5-Bit R-Counter

The 5-bit R-counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 32 are allowed.

12-Bit Interpolator MOD Value

This programmable register sets the fractional modulus, which is the ratio of the PFD frequency to the channel step resolution on the RF output. Refer to the RF Synthesizer: A Worked Example section for more information.

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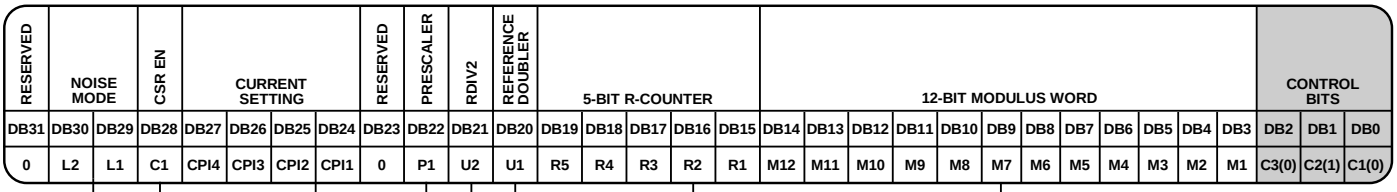

RESERVED	NOISE MODE		CSR EN	CURRENT SETTING				RESERVED	PRESCALER	RDIV2	REFERENCE DOUBLER	5-BIT R-COUNTER					12-BIT MODULUS WORD											CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	L2	L1	C1	CPI4	CPI3	CPI2	CPI1	0	P1	U2	U1	R5	R4	R3	R2	R1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C3(0)	C2(1)	C1(0)

C1	CYCLE SLIP REDUCTION
0	DISABLED
1	ENABLED[1]

U1	REFERENCE DOUBLER
0	DISABLED
1	ENABLED

M12	M11	.....	M2	M1	INTERPOLATOR MODULUS (MOD)
0	0	.....	1	0	2
0	0	.....	1	1	3
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	4092
1	1	.....	0	1	4093
1	1	.....	1	0	4094
1	1	.....	1	1	4095

L2	L1	NOISE MODE
0	0	LOW NOISE MODE
0	1	RESERVED
1	0	RESERVED
1	1	LOW SPUR MODE

U2	R-DIVIDER
0	DISABLED
1	ENABLED

P1	PRESCALER
0	4/5
1	8/9

CPI4	CPI3	CPI2	CPI1	I_{CP} (mA) 5.1kΩ
0	0	0	0	0.31
0	0	0	1	0.63
0	0	1	0	0.94
0	0	1	1	1.25
0	1	0	0	1.57
0	1	0	1	1.88
0	1	1	0	2.19
0	1	1	1	2.5
1	0	0	0	2.81
1	0	0	1	3.13
1	0	1	0	3.44
1	0	1	1	3.75
1	1	0	0	4.06
1	1	0	1	4.38
1	1	1	0	4.69
1	1	1	1	5.0

R5	R4	R3	R2	R1	R-COUNTER DIVIDE RATIO
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
1	1	1	0	1	29
1	1	1	1	.	30
1	1	1	1	1	31
0	0	0	0	0	32

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[1]CYCLE SLIP REDUCTION CANNOT BE USED IF THE PHASE DETECTOR POLARITY IS SET TO NEGATIVE.

Figure 19. MOD/R Register (R2) Map

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FUNCTION REGISTER, R3

With the control bits (Bits[2:0]) of Register R2 set to 011, the on-chip function register is programmed. Figure 20 shows the input data format for programming this register.

Counter Reset

DB3 is the counter reset bit for the ADF4156. When this bit is set to 1, the synthesizer counters are held in reset. For normal operation, this bit should be 0.

Charge-Pump Three-State

When programmed to 1, DB4 puts the charge pump into three-state mode. This bit should be set to 0 for normal operation.

Power-Down

DB5 on the ADF4156 provides the programmable power-down mode. Setting this bit to 1 performs a power-down. Setting this bit to 0 returns the synthesizer to normal operation. While in software power-down mode, the part retains all information in its registers. Only when supplies are removed are the register contents lost.

When a power-down is activated, the following events occur:

1. The synthesizer counters are forced to their load state conditions.
2. The charge pump is forced into three-state mode.
3. The digital lock detect circuitry is reset.
4. The RF_{IN} input is debiased.
5. The input register remains active and capable of loading and latching data.

Phase Detector Polarity

DB6 in the ADF4156 sets the phase detector polarity. When the VCO characteristics are positive, this bit should be set to 1. When the characteristics are negative, DB6 should be set to 0. Note that the cycle slip reduction function cannot be used if the phase detector polarity is set to negative.

Lock Detect Precision (LDP)

When DB7 is programmed to 0, the digital lock detect is set high when the phase error on 40 consecutive phase detector cycles is less than 10 ns each. When this bit is programmed to 1, 40 consecutive phase detector cycles of less than 6 ns each must occur before the digital lock detect is set.

Σ-Δ Reset

For most applications, DB14 should be programmed to 0. When DB14 is programmed to 0, the Σ-Δ modulator is reset to its starting point, or starting phase word, on every write to Register R0. This has the effect of producing consistent spur levels.

If it is not required that the Σ-Δ modulator be reset on each write to Register R0, DB14 should be set to 1.

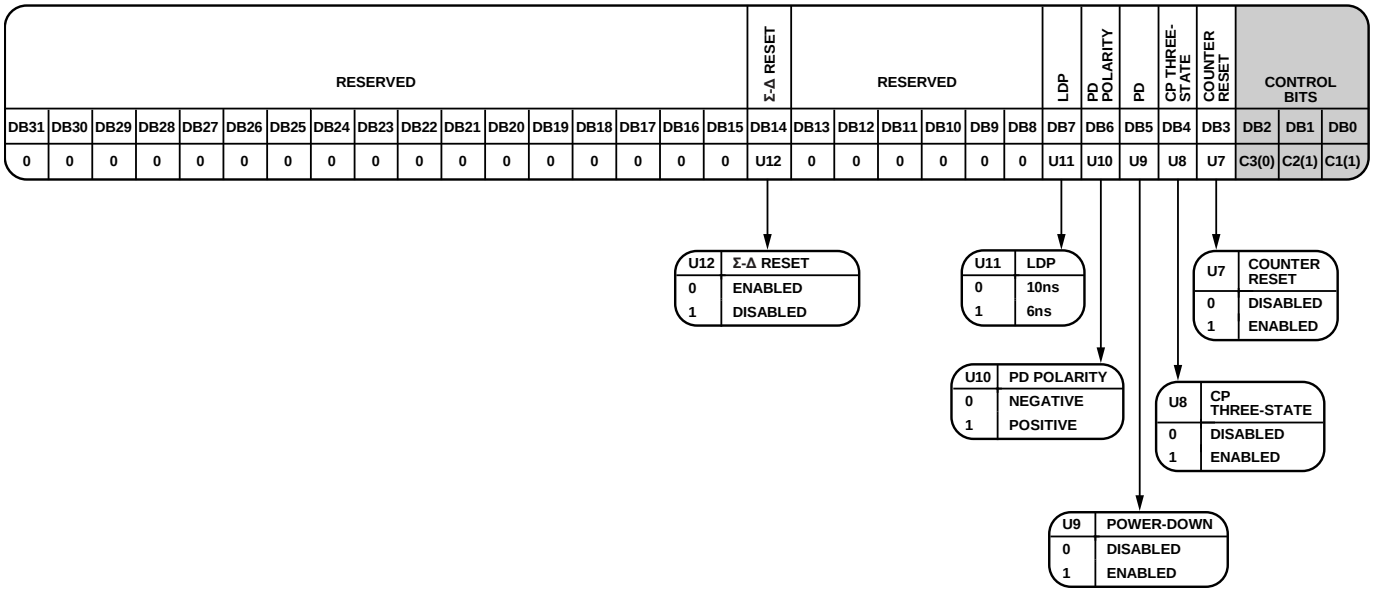

Figure 20. Function Register (R3) Map

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CLK DIV REGISTER, R4

With the control bits (Bits[2:0]) of Register R3 set to 100, the on-chip clock divider register (R4) is programmed. Figure 21 shows the input data format for programming this register.

12-Bit Clock Divider Value

The 12-bit clock divider value sets the timeout counter for activation of the fast-lock mode or a phase resync. See the Phase Resync section for more information.

Clock Divider Mode

DB[20:19] control the mode of the clock divider in the ADF4156. These bits should be set to 01 to activate the fast-lock mode, or to 10 to activate a phase resync. In most applications, neither a fast lock nor a phase resync is required. In this case, DB[20:19] should be set to 00.

RESERVED BITS

All reserved bits should be set to 0 for normal operation.

INITIALIZATION SEQUENCE

After powering up the part, the correct register programming sequence is as follows:

1. CLK DIV register (R4)
2. Function register (R3)
3. MOD/R register (R2)
4. Phase register (R1)
5. FRAC/INT register (R0)

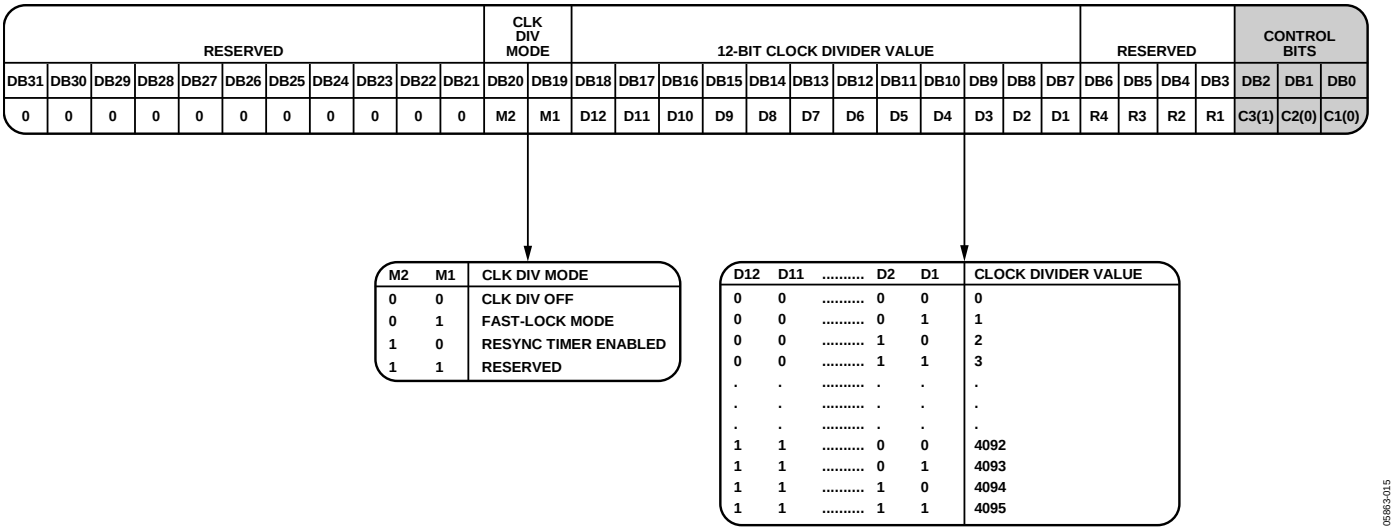

Figure 21. CLK DIV Register (R4) Map

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RF SYNTHESIZER: A WORKED EXAMPLE

The following equation governs how the synthesizer should be programmed:

$$RF_{OUT} = [INT + (FRAC/MOD)] \times [F_{PFD}] \quad (3)$$

where:
RF_{OUT} is the RF frequency output.
INT is the integer division factor.
$FRAC$ is the fractionality.
MOD is the modulus.

The PFD frequency can be calculated as follows:

$$F_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (4)$$

where:
REF_{IN} is the reference frequency input.
D is the RF REF_{IN} doubler bit.
T is the reference divide-by-2 bit, which is set to 0 or 1.
R is the RF reference division factor.

For example, in a GSM 1800 system, 1.8 GHz RF frequency output (RF_{OUT}) is required, 13 MHz reference frequency input (REF_{IN}) is available, and 200 kHz channel resolution (f_{RES}) is required on the RF output.

$$MOD = REF_{IN}/f_{RES}$$

$$MOD = 13 \text{ MHz}/200 \text{ kHz} = 65$$

Therefore, from Equation 4,

$$F_{PFD} = [13 \text{ MHz} \times (1 + 0)/1] = 13 \text{ MHz} \quad (5)$$

$$1.8 \text{ GHz} = 13 \text{ MHz} \times (INT + FRAC/65) \quad (6)$$

where $INT = 138$ and $FRAC = 30$.

MODULUS

The choice of modulus (MOD) depends on the reference signal (REF_{IN}) available and the channel resolution (f_{RES}) required at the RF output. For example, a GSM system with 13 MHz REF_{IN} sets the modulus to 65, resulting in the required RF output resolution (f_{RES}) of 200 kHz (13 MHz/65). With dither off, the fractional spur interval depends on the modulus values chosen. See Table 7 for more information.

REFERENCE DOUBLER AND REFERENCE DIVIDER

The on-chip reference doubler allows the input reference signal to be doubled. This is useful for increasing the PFD comparison frequency, which in turn improves the noise performance of the system. Doubling the PFD frequency usually improves noise performance by 3 dB. It is important to note that the PFD cannot operate with frequencies greater than 32 MHz due to a limitation in the speed of the Σ-Δ circuit of the N-divider.

The reference divide-by-2 divides the reference signal by 2, resulting in a 50% duty cycle PFD frequency. This is necessary for the correct operation of the cycle slip reduction (CSR) function. See the Fast Lock Times section for more information.

12-BIT PROGRAMMABLE MODULUS

Unlike most other fractional-N PLLs, the ADF4156 allows the user to program the modulus over a 12-bit range. Therefore, several configurations of the ADF4156 are possible for an application by varying the modulus value, the reference doubler, and the 5-bit R-counter.

For example, consider an application that requires 1.75 GHz RF and 200 kHz channel step resolution. The system has a 13 MHz reference signal.

One possible setup is feeding the 13 MHz directly into the PFD and programming the modulus to divide by 65. This results in the required 200 kHz resolution.

Another possible setup is using the reference doubler to create 26 MHz from the 13 MHz input signal. The 26 MHz signal is then fed into the PFD, which programs the modulus to divide by 130. This setup also results in 200 kHz resolution, but offers superior phase noise performance compared with the previous setup.

The programmable modulus is also useful for multistandard applications. If a dual-mode phone requires PDC and GSM 1800 standards, the programmable modulus is a great benefit. The PDC requires 25 kHz channel step resolution, whereas GSM 1800 requires 200 kHz channel step resolution.

A 13 MHz reference signal can be fed directly into the PFD, and the modulus can be programmed to 520 when in PDC mode (13 MHz/520 = 25 kHz). However, the modulus must be reprogrammed to 65 for GSM 1800 operation (13 MHz/65 = 200 kHz).

It is important that the PFD frequency remains constant (13 MHz). This allows the user to design one loop filter that can be used in both setups without running into stability issues. It is the ratio of the RF frequency to the PFD frequency that affects the loop design. By keeping this relationship constant, the same loop filter can be used in both applications.

FAST LOCK TIMES WITH THE ADF4156

As mentioned in the Noise and Spur Mode section, the ADF4156 can be optimized for noise performance. However, in fast-locking applications, the loop bandwidth needs to be wide; therefore, the filter does not provide much attenuation of the spurs.

There are two methods of achieving a fast lock time for the ADF4156: using cycle slip reduction or using dynamic bandwidth switching mode. In both cases, the idea is to keep the loop bandwidth narrow to attenuate spurs while obtaining a fast lock time.

Cycle slip reduction mode is the preferred technique because it does not require modifications to the loop filter or optimization of the timeout counter values and is therefore easier to implement.

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In most cases, this method also provides faster lock times than the bandwidth switching mode method. In extreme cases, where cycle slips do not exist in the settling transient, the bandwidth switching mode can be used.

Cycle Slip Reduction Mode

Cycle slips occur in integer-N/fractional-N synthesizers when the loop bandwidth is narrow compared with the PFD frequency. The phase error at the PFD inputs accumulates too fast for the PLL to correct, and the charge pump temporarily pumps in the wrong direction. This slows down the lock time dramatically. The ADF4156 contains a cycle slip reduction circuit to extend the linear range of the PFD, allowing faster lock times without requiring loop filter changes.

When the ADF4156 detects that a cycle slip is about to occur, it turns on an extra charge-pump current cell. This either outputs a constant current to the loop filter or removes a constant current from the loop filter, depending on whether the VCO tuning voltage needs to increase or decrease to acquire the new frequency. As a result, the linear range of the PFD is increased. Stability is maintained because the current is constant, not pulsed.

If the phase error increases to a point where another cycle slip is likely, the ADF4156 turns on another charge-pump cell. This process continues until the ADF4156 detects that the VCO frequency is beyond the desired frequency. The extra charge-pump cells then begin to turn off one by one until they are all turned off and the frequency is settled.

Up to seven extra charge-pump cells can be turned on. In most applications, this is sufficient to eliminate cycle slips altogether, resulting in much faster lock times.

Setting Bit DB28 in the MOD/R register (R2) to 1 enables cycle slip reduction. A 45% to 55% duty cycle is needed on the signal at the PFD for CSR to operate correctly. Note that CSR cannot be used if the phase detector polarity is set to negative; therefore, a noninverting loop filter topology should be used with CSR.

Dynamic Bandwidth Switching Mode

The dynamic bandwidth switching mode involves increasing the loop filter bandwidth for a set time at the beginning of the locking transient. This is achieved by boosting the charge-pump current from the set value in Register R2 to the maximum setting. To maintain loop stability during this period, it is necessary to modify the loop filter by adding a switch and resistor. When the new frequency is programmed to the ADF4156 in this mode, three events occur simultaneously to put the device in wideband mode:

- A timeout counter is started.
- The charge-pump current is boosted from its set current to the maximum setting.
- The fast-lock switch (available via MUXOUT) is activated.

The timeout counter in Register R4 defines the period that the device is kept in wideband mode. During wideband mode, the PLL acquires lock faster due to the wider loop filter bandwidth. Stability is maintained at the optimal 45° setting due to the use of the extra resistor in the loop filter.

When the timeout counter times out, the charge-pump current is reduced from the maximum setting to its set current, and the fast-lock switch is deactivated. The device is then in narrow-band mode, and spurs are attenuated.

To ensure optimum lock time, the timeout counter should be set to time out when the PLL is close to the final frequency. If the switch is deactivated, a spike in the settling transient will be observed due to charge insertion from the switch. Because the PLL is in narrow-band mode, this spike can take some time to settle out. This is one of the disadvantages of the bandwidth switching mode compared with the cycle slip reduction mode.

Fast Lock: An Example

If a PLL has a reference frequency of 13 MHz, a f_{PFD} of 13 MHz, and a required lock time of 50 µs, the PLL is set to wide bandwidth for 40 µs.

If the time set for the wide bandwidth is 40 µs, then

$$Fast\text{-}Lock\ Timer\ Value = Time\ in\ Wide\ Bandwidth \times f_{PFD}$$

$$Fast\text{-}Lock\ Timer\ Value = 40\ \mu s \times 13\ MHz = 520$$

Therefore, 520 must be loaded into Bits DB[18:7] of Register R4. The clock divider mode bits (DB[20:19]) in Register R4 must also be set to 01 to activate this mode. To activate the fast-lock switch on the MUXOUT pin, the MUXOUT control bits (DB[30:27]) in Register R0 must be set to 1100.

Fast Lock: Loop Filter Topology

To use fast-lock mode, an extra connection from the PLL to the loop filter is needed. The damping resistor in the loop filter must be reduced to ¼ of its value while in wide bandwidth mode. This is required because the charge-pump current is increased by 16 while in wide bandwidth mode and stability must be ensured. When the ADF4156 is in fast-lock mode (that is, when the fast-lock switch is programmed to appear at the MUXOUT pin), the MUXOUT pin is automatically shorted to ground. The following two topologies can be used:

- Topology 1: Divide the damping resistor (R1) into two values (R1 and R1A) that have a ratio of 1:3 (see Figure 22).
- Topology 2: Connect an extra resistor (R1A) directly from MUXOUT, as shown in Figure 23. The extra resistor must be chosen such that the parallel combination of an extra resistor and the damping resistor (R1) is reduced to ¼ of the original value of R1 (see Figure 23).

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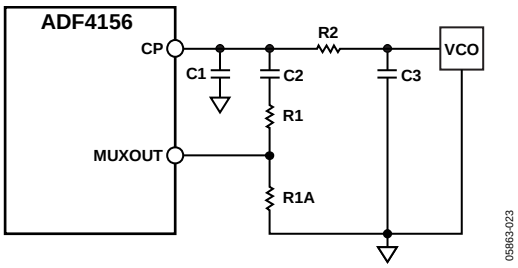

Figure 22. Topology 1—Fast-Lock Loop Filter Topology

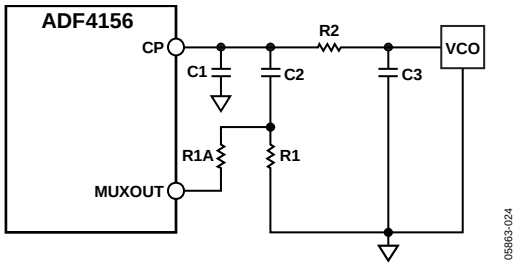

Figure 23. Topology 2—Fast-Lock Loop Filter Topology

SPUR MECHANISMS

This section describes the three spur mechanisms that arise with a fractional-N synthesizer and how to minimize these spurs in the ADF4156.

Fractional Spurs

The fractional interpolator in the ADF4156 is a third-order Σ-Δ modulator with a modulus (MOD) that is programmable to any integer value from 2 to 4095. In low spur mode (dither enabled), the minimum allowable value of MOD is 50. The Σ-Δ modulator is clocked at the PFD reference rate (f_{PFD}) that allows PLL output frequencies to be synthesized at a channel step resolution of f_{PFD}/MOD.

In low noise mode (dither off), the quantization noise from the Σ-Δ modulator appears as fractional spurs. The interval between spurs is f_{PFD}/L, where L is the repeat length of the code sequence in the digital Σ-Δ modulator. For the third-order modulator used in the ADF4156, the repeat length depends on the value of MOD, as listed in Table 7.

Table 7. Fractional Spurs with Dither Off

Condition	Repeat Length	Spur Interval
If MOD is divisible by 2, but not 3	2 × MOD	Channel step/2
If MOD is divisible by 3, but not 2	3 × MOD	Channel step/3
If MOD is divisible by 6	6 × MOD	Channel step/6
Otherwise	MOD	Channel step

In low spur mode (dither enabled), the repeat length is extended to 2^{21} cycles, regardless of the value of MOD, which makes the quantization error spectrum look like broadband noise. As a result, the in-band phase noise at the PLL output can be degraded by as much as 10 dB. Therefore, for lowest noise, keeping dither off is a better choice, particularly when the final loop bandwidth is low enough to attenuate even the lowest frequency fractional spur.

Integer Boundary Spurs

Another mechanism for fractional spur creation is interactions between the RF VCO frequency and the reference frequency. When these frequencies are not integer related (as is the case with fractional-N synthesizers), spur sidebands appear on the VCO output spectrum at an offset frequency that corresponds to the beat note or the difference in frequency between an integer multiple of the reference and the VCO frequency.

These spurs are attenuated by the loop filter and are more noticeable on channels close to integer multiples of the reference, where the difference frequency can be inside the loop bandwidth, hence the name integer boundary spurs.

Reference Spurs

Reference spurs are generally not a problem in fractional-N synthesizers because the reference offset is far outside the loop bandwidth. However, any reference feedthrough mechanism that bypasses the loop can cause a problem. One such mechanism is feedthrough of low levels of switching noise from the on-chip reference through the RF_{IN} pin and back to the VCO, resulting in reference spur levels as high as −90 dBc. Care should be taken in the PCB layout to ensure that the VCO is well separated from the input reference to avoid a possible feedthrough path on the board.

SPUR CONSISTENCY AND FRACTIONAL SPUR OPTIMIZATION

With dither off, the fractional spur pattern due to the quantization noise of the Σ-Δ modulator also depends on the phase word set as the starting point of the modulator. Setting the Σ-Δ reset bit (DB14 in Register R3) to 0 ensures that this starting point is used for the Σ-Δ modulator on every write to Register R0.

The phase word can be varied to optimize the fractional and subfractional spur levels on any particular frequency. Therefore, a look-up table of phase values corresponding to each frequency can be constructed for use when programming the ADF4156.

The evaluation software has a sweep function to sweep the phase word so that the user can observe the spur levels on a spectrum analyzer.

If a look-up table is not used, keep the phase word at a constant value to ensure consistent spur levels on a particular frequency.

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PHASE RESYNC

The output of a fractional-N PLL can settle to any MOD phase offset with respect to the input reference, where MOD is the fractional modulus. The phase resync feature in the ADF4156 is used to produce a consistent output phase offset with respect to the input reference. This is necessary in applications where the output phase and frequency are important, such as digital beam forming. See the Phase Programmability section for information about how to program a specific RF output phase when using the phase resync feature.

Phase resync is enabled by setting Bits DB[20:19] in Register R4 to 10. When phase resync is enabled, an internal timer generates sync signals at intervals of t_{SYNC} as indicated by the following formula:

$$t_{SYNC} = CLK_DIV_VALUE \times MOD \times t_{PFD}$$

where:
t_{PFD} is the PFD reference period.
CLK_DIV_VALUE is the decimal value programmed in Bit DB[18:7] of Register R4. This value can be any integer in the range of 1 to 4095.
MOD is the modulus value programmed in Bit DB[14:3] of Register R2.

When a new frequency is programmed, the second sync pulse after the LE rising edge is used to resynchronize the output phase to the reference. The t_{SYNC} time should be programmed to a value that is at least as long as the worst-case lock time. Doing so guarantees that the phase resync occurs after the last cycle slip in the PLL settling transient.

In the example shown in Figure 24, the PFD reference is 25 MHz and the MOD value is 125 for a 200 kHz channel spacing. Therefore, t_{SYNC} is set to 400 µs by programming CLK_DIV_VALUE to 80.

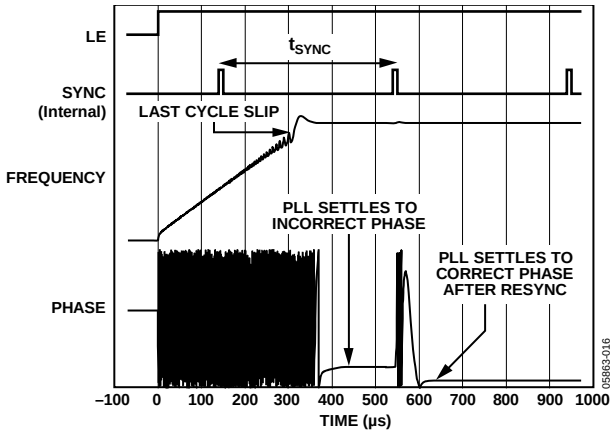

Figure 24. Phase Resync Example

Phase Programmability

To program a specific RF output phase, change the phase word in Register R1. As this word is swept from 0 to MOD, the RF output phase sweeps over a 360°/MOD range in steps of 360°/MOD.

LOW FREQUENCY APPLICATIONS

The specification on the RF input is 0.5 GHz minimum; however, lower RF frequencies can be used if the minimum slew rate specification of 400 V/µs is met. An appropriate LVDS driver, such as the FIN1001 from Fairchild Semiconductor, can be used to square up the RF signal before it is fed back into the ADF4156 RF input.

FILTER DESIGN—ADIsimPLL

A filter design and analysis program is available to help implement the PLL design. Visit www.analog.com/pll for a free download of the ADIsimPLL™ software. This software designs, simulates, and analyzes the entire PLL frequency domain and time domain response. Various passive and active filter architectures are allowed. When designing the loop filter, keep the ratio of the PFD frequency to the loop bandwidth >200:1 to attenuate the Σ-Δ modulator noise.

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INTERFACING

The ADF4156 has a simple SPI-compatible serial interface for writing to the device. CLOCK, DATA, and LE control the data transfer. When latch enable (LE) is high, the 29 bits that have been clocked into the input register on each rising edge of serial clock are transferred to the appropriate latch. The maximum allowable serial clock rate is 20 MHz. See Figure 2 for the timing diagram and Table 6 for the latch truth table.

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

The lands on the lead frame chip scale package (CP-20-6) are rectangular. The printed circuit board pad for these lands should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The package land should be centered on the pad to ensure that the solder joint size is maximized.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern to ensure that shorting is avoided.

Thermal vias can be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad on a 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz of copper to plug the via. In addition, the printed circuit board thermal pad should be connected to AGND.

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OUTLINE DIMENSIONS

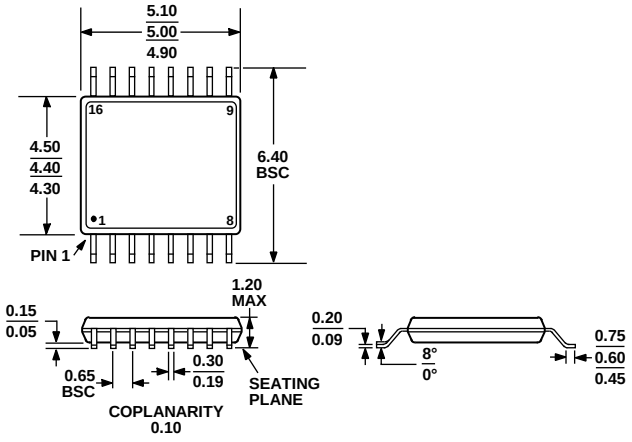

Figure 25. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

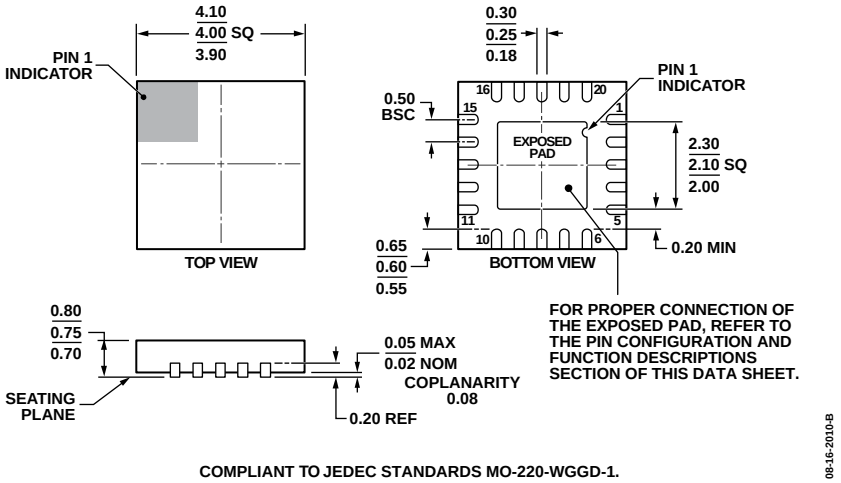

Figure 26. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-20-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADF4156BRUZ	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4156BRUZ-RL	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4156BRUZ-RL7	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4156BCPZ	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4156BCPZ-RL	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4156BCPZ-RL7	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
EV-ADF4156SD1Z		Evaluation Board	

[1] Z = RoHS Compliant Part.

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NOTES

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NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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