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REVISION HISTORY

8/05—Rev. 0 to Rev. A
Changes to Ordering Guide 15

7/05—Revision 0: Initial Version

SPECIFICATIONS

V_S = +5 V (@T_A = 25°C, G = +2, R_L = 150 Ω, unless otherwise noted).

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O = 0.2 V p-p		300		MHz
	V_O = 2 V p-p		200		MHz
G = +1	V_O = 0.2 V p-p		620		MHz
Bandwidth for 0.1 dB Flatness	V_O = 2 V p-p		65		MHz
+Slew Rate (Rising Edge)	V_O = 2 V p-p		750		V/µs
−Slew Rate (Falling Edge)	V_O = 2 V p-p		600		V/µs
Settling Time to 0.5%	V_O = 2 V step		9		ns
DISTORTION/NOISE PERFORMANCE					
Harmonic Distortion HD2	f_C = 1 MHz, V_O = 2 V p-p		−81		dBc
Harmonic Distortion HD3	f_C = 1 MHz, V_O = 2 V p-p		−88		dBc
Harmonic Distortion HD2	f_C = 5 MHz, V_O = 2 V p-p		−68		dBc
Harmonic Distortion HD3	f_C = 5 MHz, V_O = 2 V p-p		−76		dBc
Voltage Noise (RTO)	f = 100 kHz		10.6		nV/√Hz
Current Noise (RTI)	f = 100 kHz, +IN		1.4		pA/√Hz
Differential Gain			0.02		%
Differential Phase			0.03		Degrees
Crosstalk	Amplifier 1 driven, Amplifier 2 output measured, f = 1 MHz		−75		dB
DC PERFORMANCE					
Offset Voltage (RTO)	Referred to output (RTO)	−25	+3.5	+25	mV
+Input Bias Current		−2.5	−0.6	+1	µA
Gain Accuracy		1.9	2	2.1	V/V
INPUT CHARACTERISTICS					
Input Resistance	+IN		13		MΩ
Input Capacitance	+IN		2		pF
Input Common-Mode Voltage Range	G = +1		1 to 4		V
POWER DOWN PIN					
Input Voltage	Enabled		0.6		V
	Power down		1.8		V
Bias Current	Enabled		−3		µA
	Power down		115		µA
Turn-On Time			3.5		µs
Turn-Off Time			200		ns
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rise/Fall)	V_{IN} = +2.25 V to −0.25 V		85/50		ns
Output Voltage Swing	R_L = 150 Ω		1.2 to 3.8		V
Output Voltage Swing	R_L = 1 kΩ		1 to 4		V
Short-Circuit Current	Sinking or sourcing		65		mA
POWER SUPPLY					
Operating Range		5		12	V
Total Quiescent Current	Enabled	14	16	18	mA
Quiescent Current /Amplifier	Power down = $+V_S$		0.2	0.33	mA
Power Supply Rejection Ratio (RTO)					dB
+PSR	$+V_S$ = 2 V to 3 V, $-V_S$ = −2.5 V	−52	−55		dB
−PSR	$+V_S$ = 2.5 V, $-V_S$ = −2 V to −3 V Power Down pin = $-V_S$	−49	−52		dB

V_S = ±5 V (@T_A = +25°C, G = +2, R_L = 150 Ω, unless otherwise noted).

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O = 0.2 V p-p		310		MHz
	V_O = 2 V p-p		260		MHz
G = +1	V_O = 0.2 V p-p		720		MHz
Bandwidth for 0.1 dB Flatness	V_O = 2 V p-p		54		MHz
+Slew Rate (Rising Edge)	V_O = 2 V p-p		1050		V/µs
−Slew Rate (Falling Edge)	V_O = 2 V p-p		830		V/µs
Settling Time to 0.5%	V_O = 2 V step		9		ns
DISTORTION/NOISE PERFORMANCE					
Harmonic Distortion HD2	f_C = 1 MHz, V_O = 2 V p-p		−87		dBc
Harmonic Distortion HD3	f_C = 1 MHz, V_O = 2 V p-p		−100		dBc
Harmonic Distortion HD2	f_C = 5 MHz, V_O = 2 V p-p		−74		dBc
Harmonic Distortion HD3	f_C = 5 MHz, V_O = 2 V p-p		−90		dBc
Voltage Noise (RTO)	f = 100 kHz		10.6		nV/√Hz
Current Noise (RTI)	f = 100 kHz, +IN		1.4		pA/√Hz
Differential Gain			0.01		%
Differential Phase			0.02		Degrees
Crosstalk	Amplifier 1 driven, Amplifier 2 output measured, f = 1 MHz		−75		dB
DC PERFORMANCE					
Offset Voltage (RTO)		−25	+2	+25	mV
+Input Bias Current		−2.5	−0.6	+1	µA
Gain Accuracy		1.9	2	2.1	V/V
INPUT CHARACTERISTICS					
Input Resistance	+IN		14		MΩ
Input Capacitance	+IN		2		pF
Input Common-Mode Voltage Range	G = +1		−3.7 to +3.8		V
POWER DOWN PIN					
Input Voltage	Enabled		−4.4		V
	Power down		−3.2		V
Bias Current	Enabled		−3		µA
	Power down		250		µA
Turn-On Time			3.5		µs
Turn-Off Time			200		ns
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rise/Fall)	V_{IN} = ±3.0 V		85/40		ns
Output Voltage Swing	R_L = 150 Ω		−3.5 to +3.5		V
Output Voltage Swing	R_L = 1 kΩ		−3.9 to +3.9		V
Short-Circuit Current	Sinking or sourcing		115		mA
POWER SUPPLY					
Operating Range		5		12	V
Total Quiescent Current	Enabled	14.5	17.9	20.5	mA
Quiescent Current/Amplifier	Power down = +V_S		0.3	0.5	mA
Power Supply Rejection Ratio (RTO)					dB
+PSR	+V_S = 4 V to 6 V, −V_S = −5 V	−54	−57		dB
−PSR	+V_S = 5 V, −V_S = −4 V to −6 V, Power Down pin = −V_S	+50.5	−54		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	12.6 V
Power Dissipation	See Figure 3
Common-Mode Input Voltage	$\pm V_S$
Storage Temperature	−65°C to +125°C
Operating Temperature Range	−40°C to +105°C
Lead Temperature	JEDEC J-STD-20
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
14-lead SOIC	90	°C/W

Maximum Power Dissipation

The maximum safe power dissipation for the ADA4862-3 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a junction temperature of 150°C for an extended period can result in changes in silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the die due to the amplifier's drive at the output. The quiescent power is the voltage between the supply pins (V_S) × the quiescent current (I_S).

$$P_D = \textit{Quiescent Power} + (\textit{Total Drive Power} - \textit{Load Power})$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

RMS output voltages should be considered.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads and through holes under the device reduces θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 14-lead SOIC (90°C/W) on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

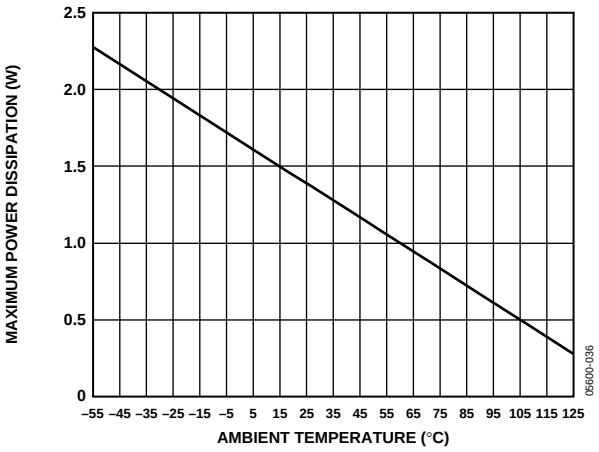


Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

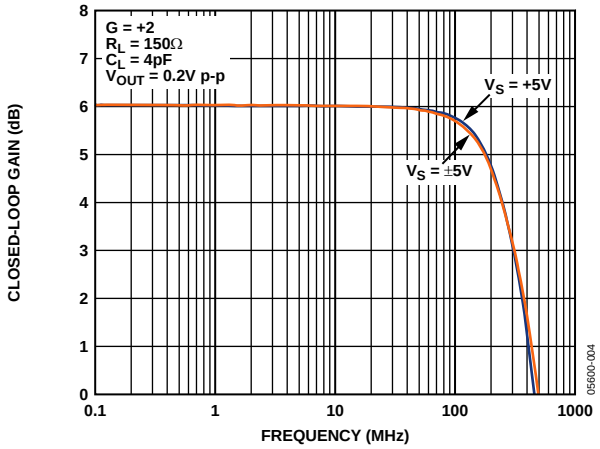


Figure 4. Small Signal Frequency Response for Various Supplies

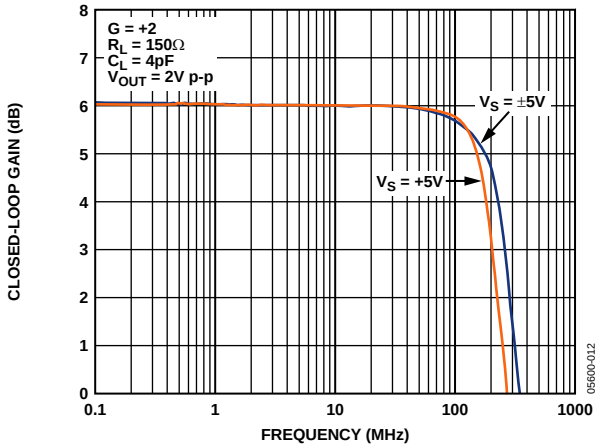


Figure 5. Large Signal Frequency Response for Various Supplies

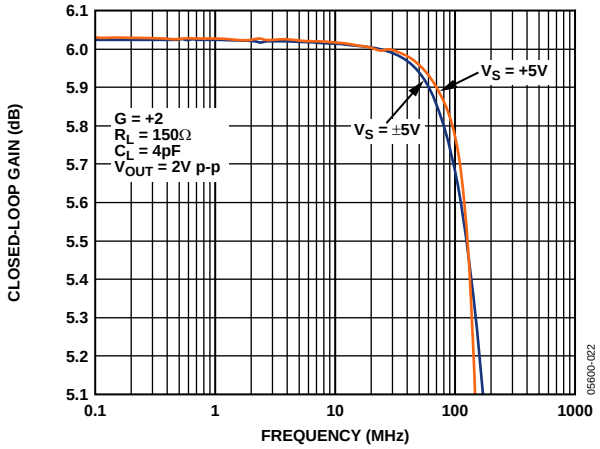


Figure 6. Large Signal 0.1 dB Bandwidth for Various Supplies

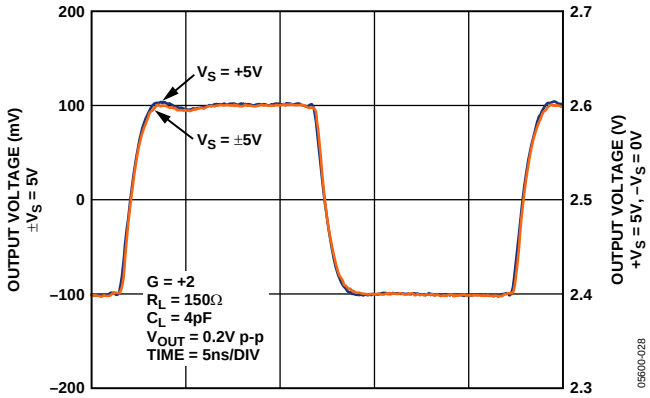


Figure 7. Small Signal Transient Response for Various Supplies

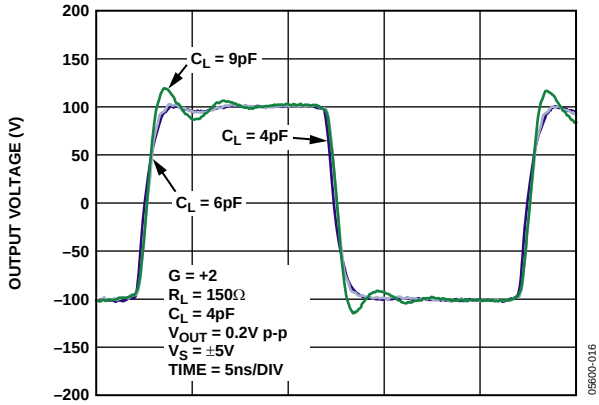


Figure 8. Small Signal Transient Response for Various Capacitor Loads

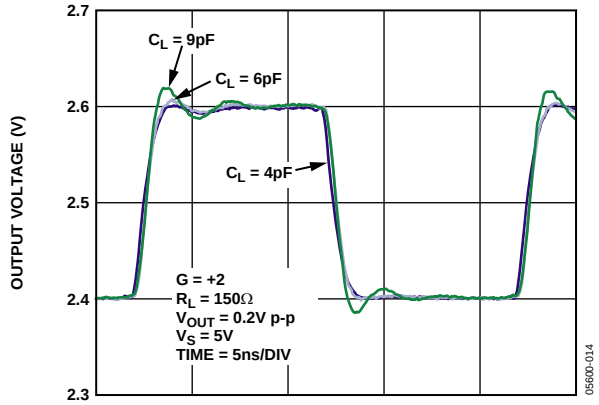


Figure 9. Small Signal Transient Response for Various Capacitor Loads

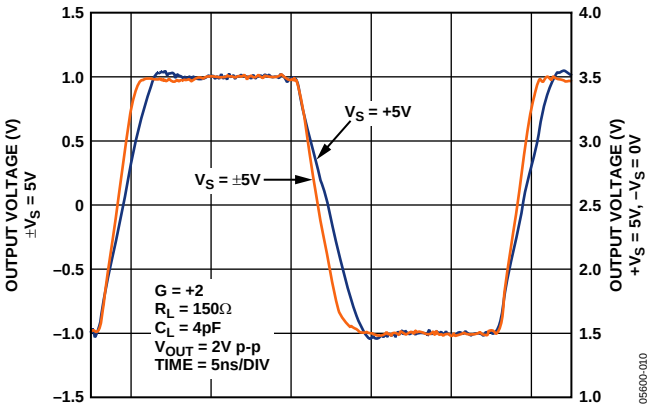


Figure 10. Large Signal Transient Response for Various Supplies

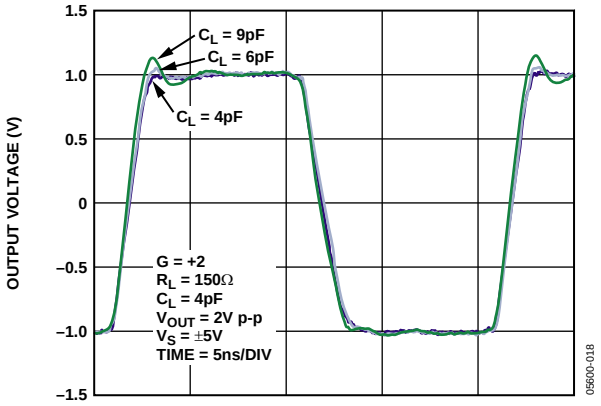


Figure 11. Large Signal Transient Response for Various Capacitor Loads

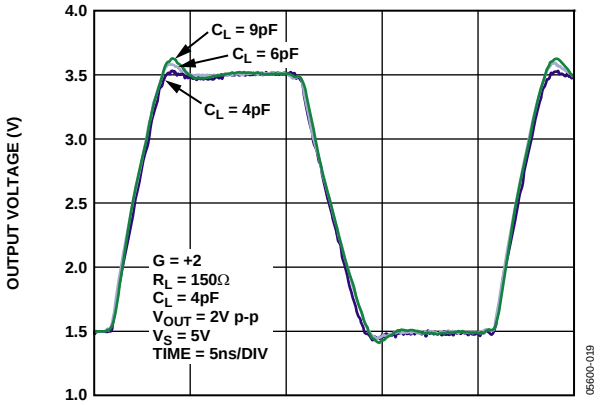


Figure 12. Large Signal Transient Response for Various Capacitor Loads

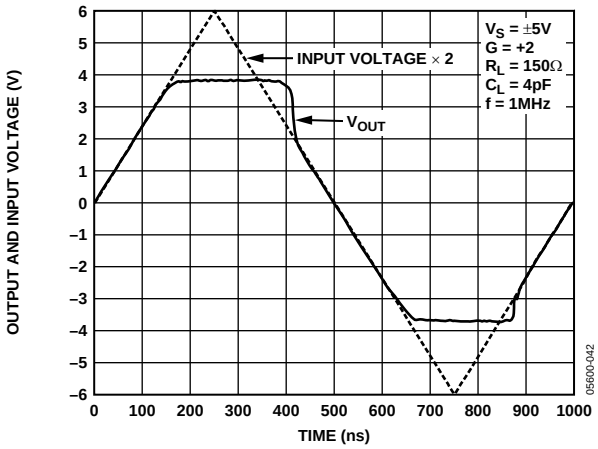


Figure 13. Input Overdrive Recovery

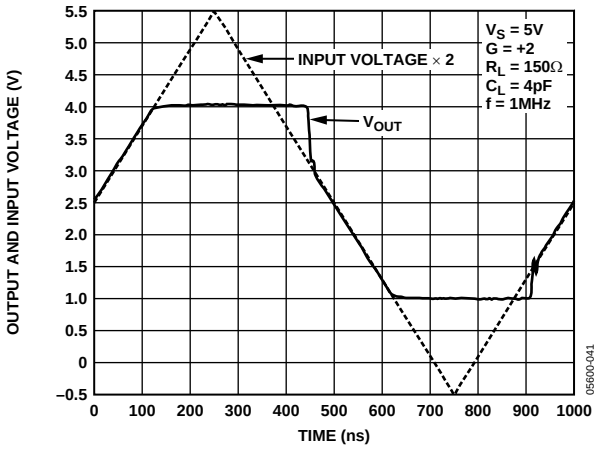


Figure 14. Output Overdrive Recovery

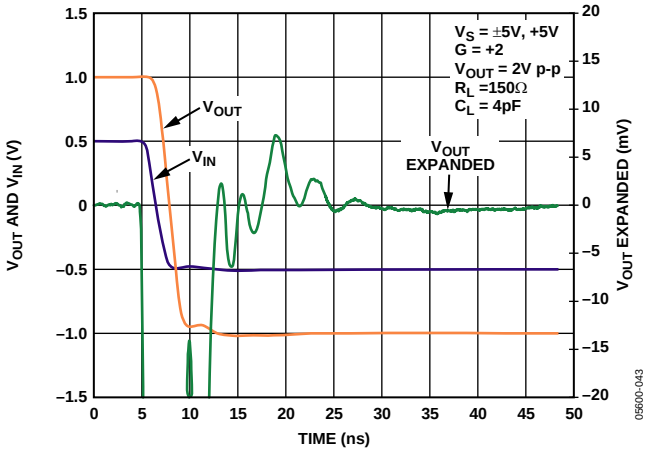


Figure 15. Settling Time Falling Edge

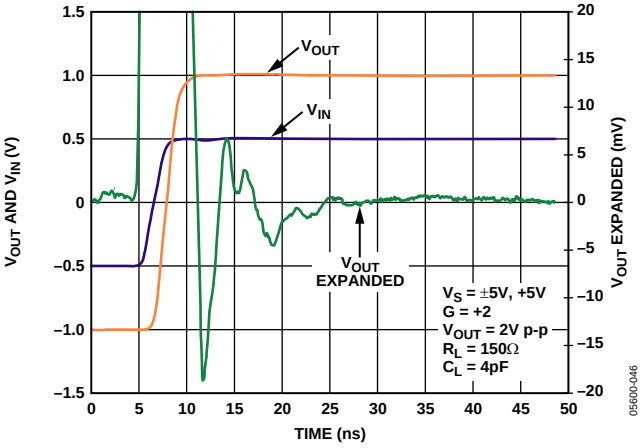


Figure 18. Settling Time Rising Edge

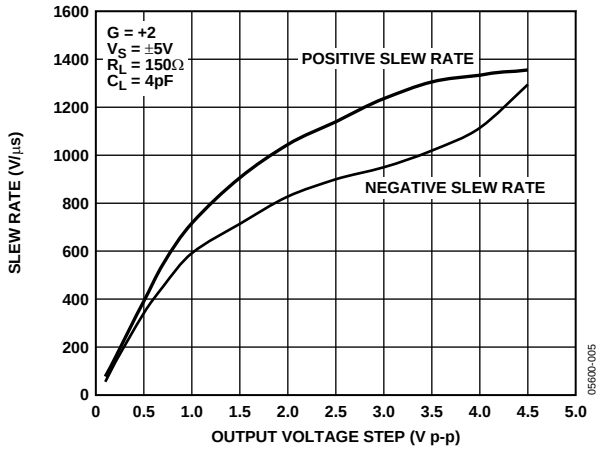


Figure 16. Slew Rate vs. Output Voltage

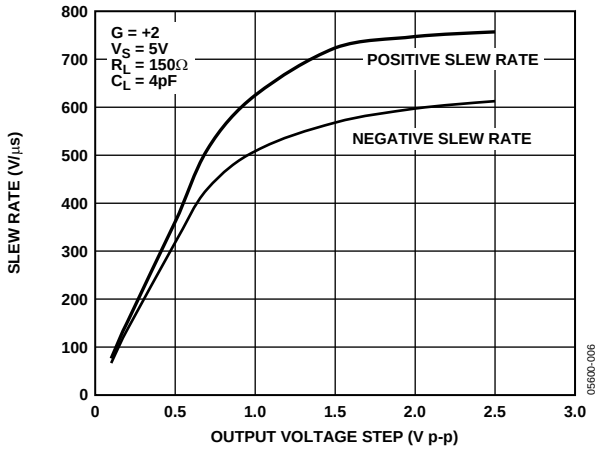


Figure 19. Slew Rate vs. Output Voltage

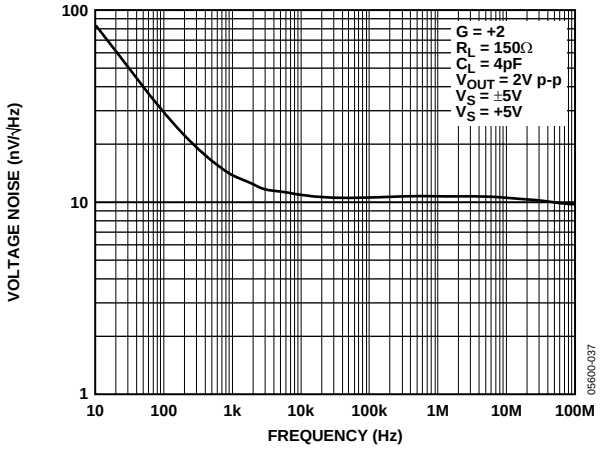


Figure 17. Voltage Noise vs. Frequency Referred to Output (RTO)

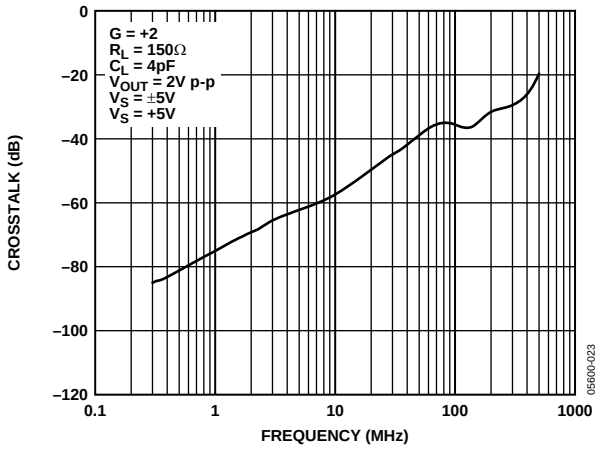


Figure 20. Large Signal Crosstalk

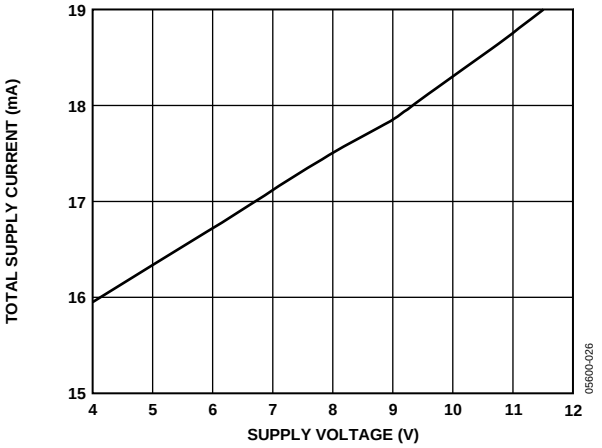


Figure 21. Total Supply Current vs. V_{SUPPLY}

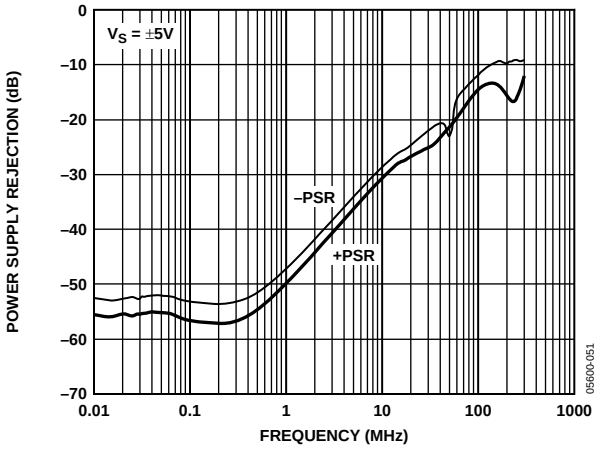


Figure 23. Power Supply Rejection vs. Frequency

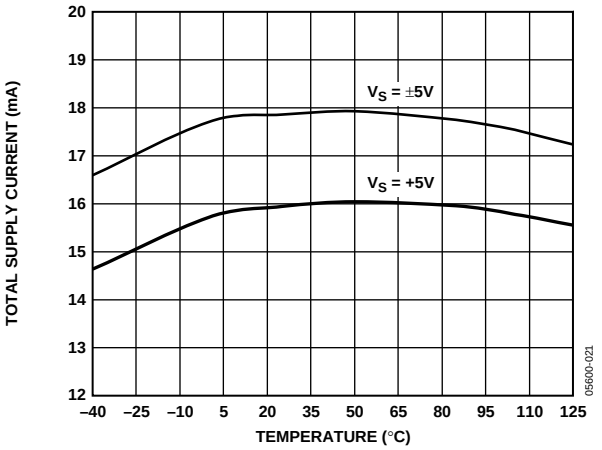


Figure 22. Total Supply Current at Various Supplies vs. Temperature

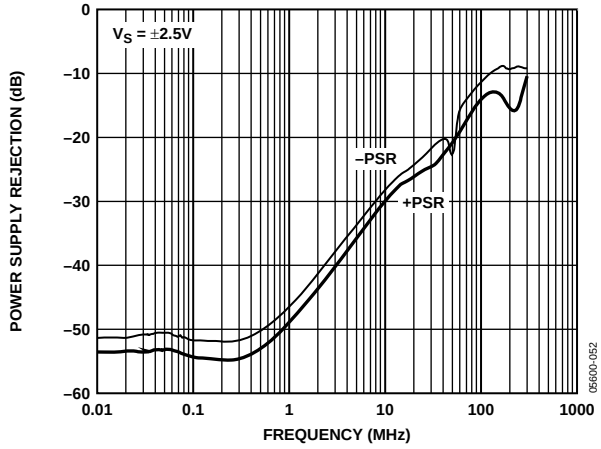


Figure 24. Power Supply Rejection vs. Frequency

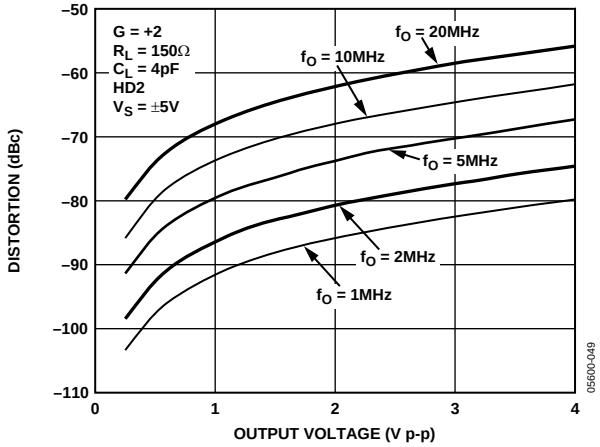


Figure 25. HD2 vs. Frequency vs. Output Voltage

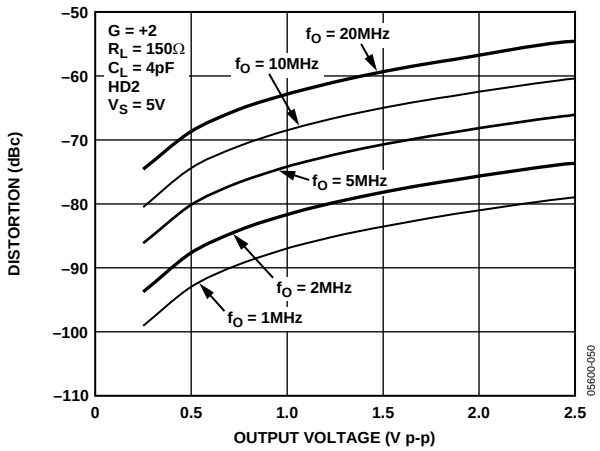


Figure 26. HD2 vs. Frequency vs. Output Voltage

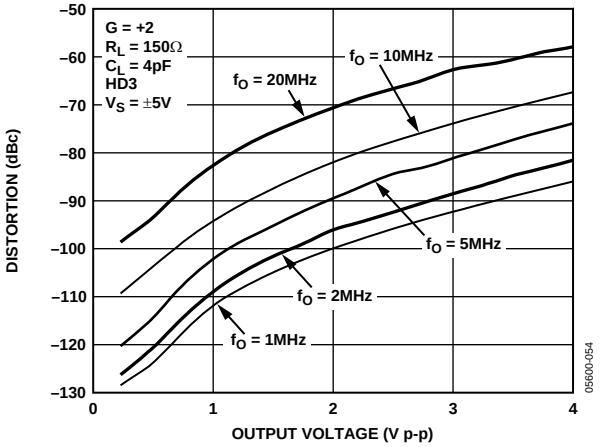


Figure 27. HD3 vs. Frequency vs. Output Voltage

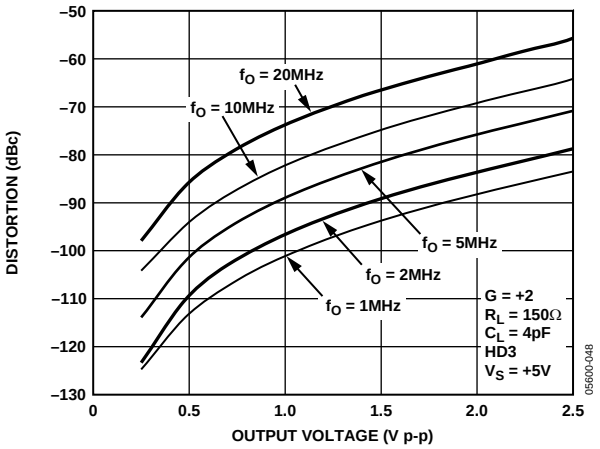


Figure 28. HD3 vs. Frequency vs. Output Voltage

APPLICATIONS

USING THE ADA4862-3 IN GAINS = +1, −1

The ADA4862-3 was designed to offer outstanding video performance, simplify applications, and minimize board area.

The ADA4862-3 is a triple amplifier with on-chip feedback and gain set resistors. The gain is fixed internally at G = +2. The inclusion of the on-chip resistors not only simplifies the design of the application but also eliminates six surface-mount resistors, saving valuable board space and lowers assembly costs. A typical schematic is shown in Figure 29.

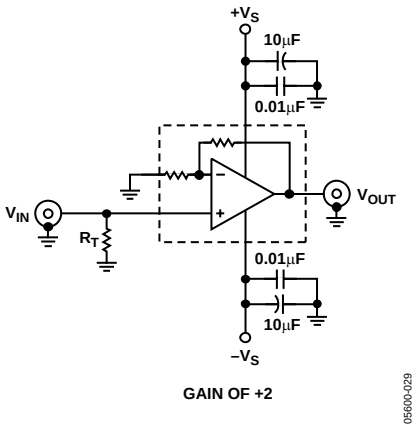


Figure 29. Noninverting Configuration (G = +2)

While the ADA4862-3 has a fixed gain of G = +2, it can be used in other gain configurations, such as G = −1 and G = +1, which are discussed next.

Unity-Gain Operation (Option 1)

There are two options for obtaining unity gain (G = +1). The first is shown in Figure 30. In this configuration, the –IN input pin is left floating (feedback is provided via the internal 550 Ω), and the input is applied to the noninverting input. The noise gain for this configuration is 1. Frequency performance and transient response are shown in Figure 31 through Figure 33.

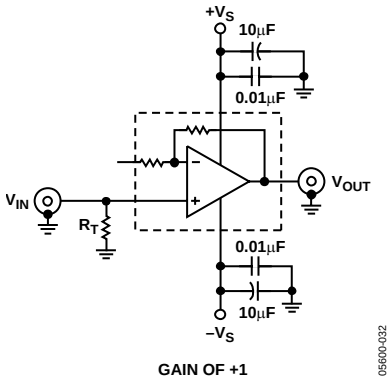


Figure 30. Unity Gain of Option 1

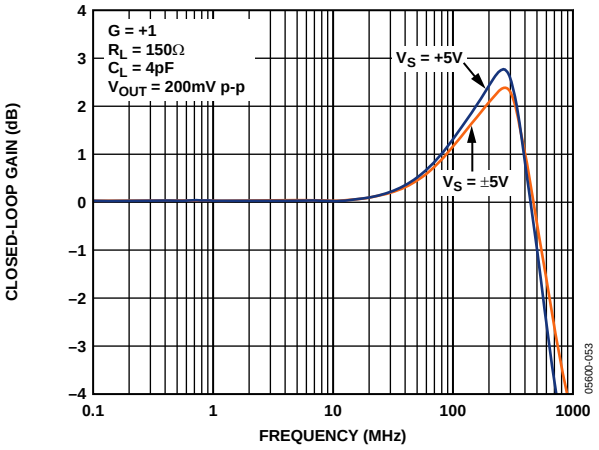


Figure 31. Small Signal Unity Gain

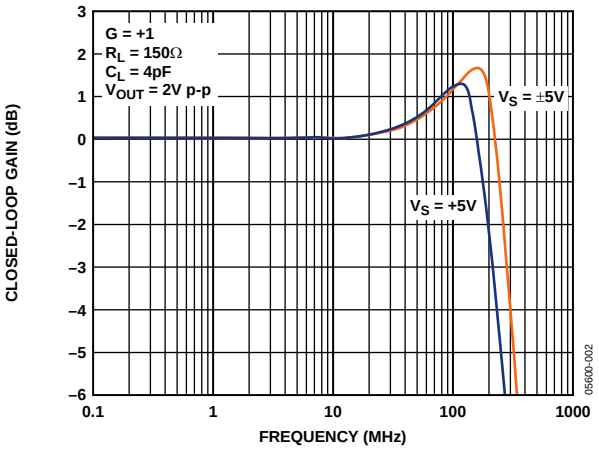


Figure 32. Large Signal Gain +1

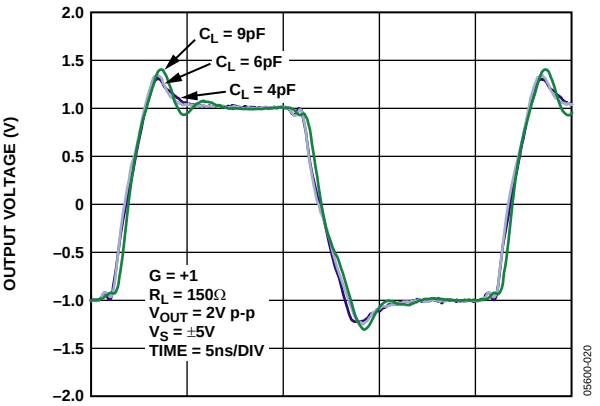


Figure 33. Large Signal Transient Response for Various Capacitor Loads

Option 2

Another option exists for running the ADA4862-3 as a unity-gain amplifier. In this configuration, the noise gain is 2, see Figure 34. The frequency response and transient response for this configuration closely match the gain of +2 plots because the noise gains are equal. This method does have twice the noise gain of Option 1; however, in applications that do not require low noise, Option 2 offers less peaking and ringing. By tying the inputs together, the net gain of the amplifier becomes 1. Equation 1 shows the transfer characteristic for the schematic shown in Figure 34. Frequency and transient response are shown in Figure 35 and Figure 36.

$$V_O = V_i\left(\frac{-R_F}{R_G}\right) + V_i\left(\frac{R_F + R_G}{R_G}\right) \quad (1)$$

which simplifies to $V_O = V_i$.

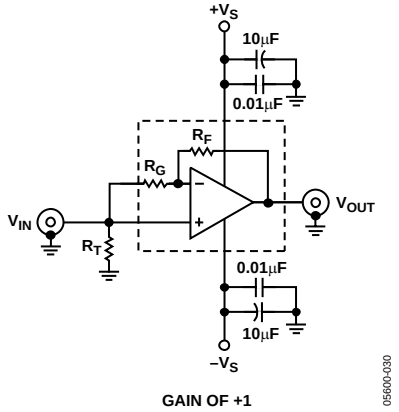


Figure 34. Unity Gain of Option 2

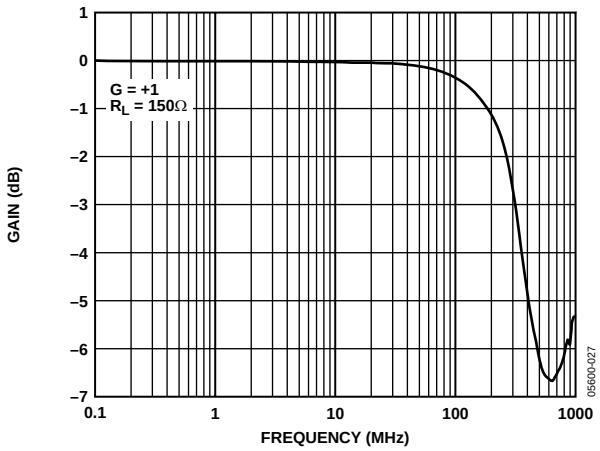


Figure 35. Frequency Response of Option 2

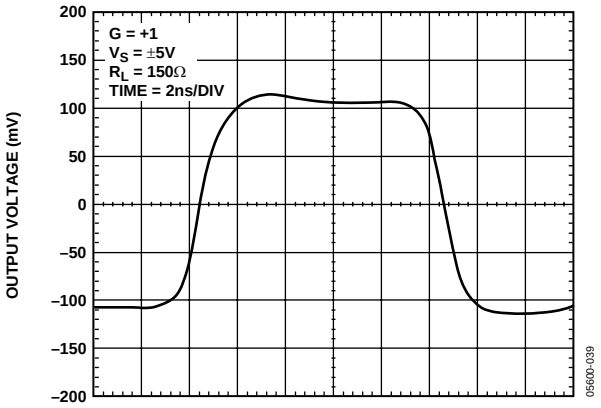


Figure 36. Small Signals Transient Response of Option 2

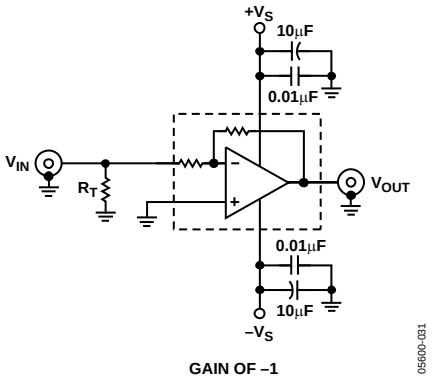


Figure 37. Inverting Configuration (G = –1)

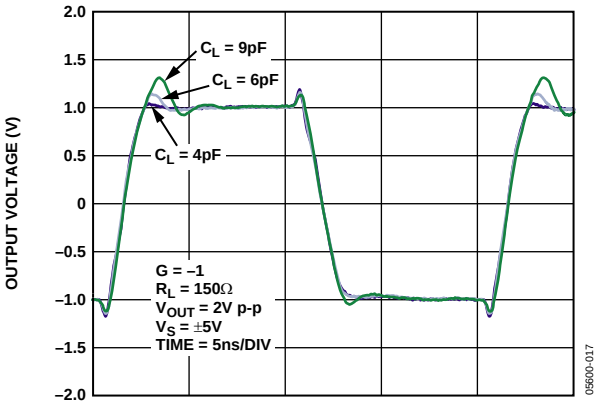


Figure 38. Large Signal Transient Response for Various Capacitor Loads

VIDEO LINE DRIVER

The ADA4862-3 was designed to excel in video driver applications. Figure 39 shows a typical schematic for a video driver operating on a bipolar supplies.

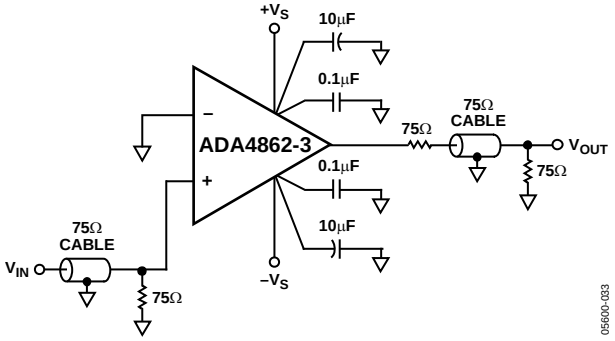


Figure 39. Video Driver Schematic

In applications that require two video loads be driven simultaneously, the ADA4862-3 can deliver. Figure 40 shows the ADA4862-3 configured with dual video loads. Figure 41 shows the dual video load performance.

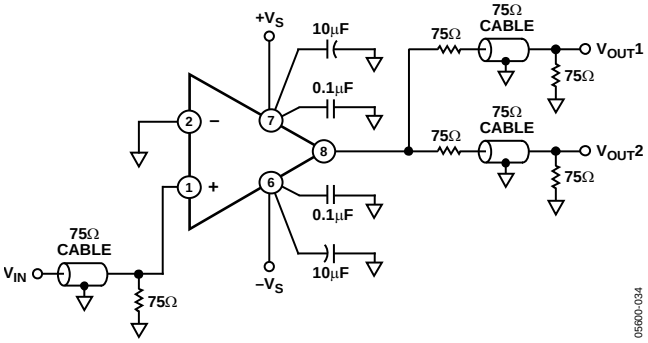


Figure 40. Video Driver Schematic for Two Video Loads

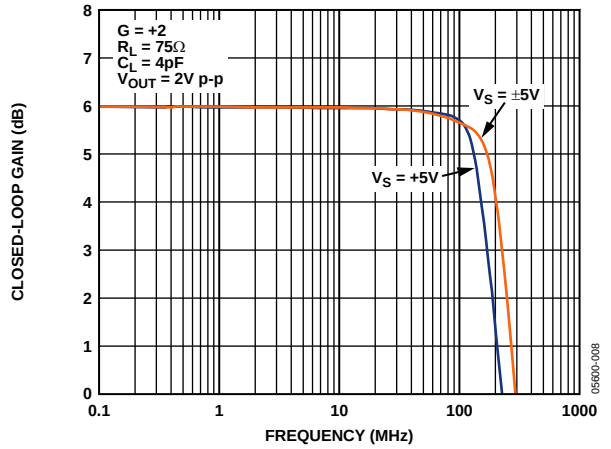


Figure 41. Large Signal Frequency Response for Various Supplies, R_L = 75 Ω

SINGLE-SUPPLY OPERATION

The ADA4862-3 can also operate in single-supply applications. Figure 42 shows the schematic for a single 5 V supply video driver. Resistors R2 and R4 establish the midsupply reference. Capacitor C2 is the bypass capacitor for the midsupply reference. Capacitor C1 is the input coupling capacitor, and C6 is the output coupling capacitor. Capacitor C5 prevents constant current from being drawn through the internal gain set resistor. Resistor R3 sets the circuits ac input impedance.

For more information on single-supply operation of op amps, see www.analog.com/library/analogDialogue/archives/35-02/avoiding/.

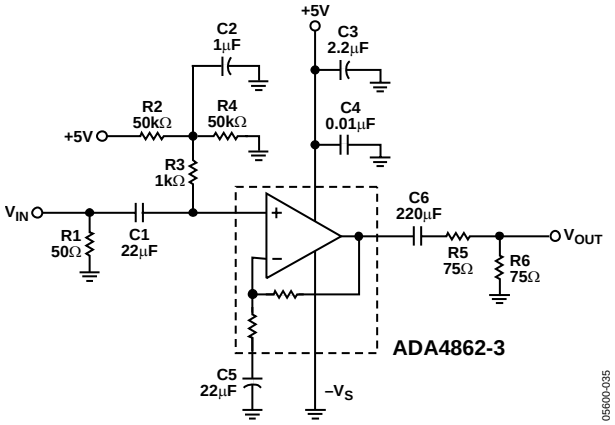


Figure 42. Single-Supply Video Driver Schematic

POWER DOWN

The ADA4862-3 is equipped with an independent Power Down pin for each amplifier allowing the user to reduce the supply current when an amplifier is inactive. The voltage applied to the $-V_S$ pin is the logic reference, making single-supply applications useful with conventional logic levels. In a typical 5 V single-supply application, the $-V_S$ pin is connected to analog ground. The amplifiers are powered down when applied logic levels are greater than $-V_S$ + 1 V. The amplifiers are enabled whenever the disable pins are left either floating (disconnected) or the applied logic levels are lower than 1 V above $-V_S$.

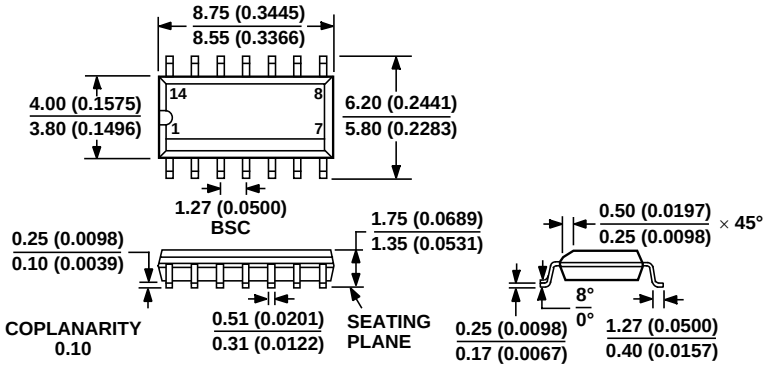
LAYOUT CONSIDERATIONS

As is the case with all high speed applications, careful attention to printed circuit board layout details prevents associated board parasitics from becoming problematic. Proper RF design technique is mandatory. The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance return path. Removing the ground plane on all layers from the area near the input and output pins reduces stray capacitance. Termination resistors and loads should be located as close as possible to their respective inputs and outputs. Input and output traces should be kept as far apart as possible to minimize coupling (crosstalk) though the board. Adherence to microstrip or stripline design techniques for long signal traces (greater than about 1 inch) is recommended.

POWER SUPPLY BYPASSING

Careful attention must be paid to bypassing the power supply pins of the ADA4862-3. High quality capacitors with low equivalent series resistance (ESR), such as multilayer ceramic capacitors (MLCCs), should be used to minimize supply voltage ripple and power dissipation. A large, usually tantalum, 10 µF to 47 µF capacitor located in proximity to the ADA4862-3 is required to provide good decoupling for lower frequency signals. In addition, 0.1 µF MLCC decoupling capacitors should be located as close to each of the power supply pins as is physically possible, no more than 1/8 inch away. The ground returns should terminate immediately into the ground plane. Locating the bypass capacitor return close to the load return minimizes ground loops and improves performance.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 43. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Ordering Quantity	Package Option
ADA4862-3YRZ[1]	–40°C to +105°C	14-Lead SOIC_N	1	R-14
ADA4862-3YRZ-RL[1]	–40°C to +105°C	14-Lead SOIC_N	2,500	R-14
ADA4862-3YRZ-RL7[1]	–40°C to +105°C	14-Lead SOIC_N	1,000	R-14

[1] Z = Pb-free part.

NOTES

D05600–0–8/05(A)