TABLE OF CONTENTS

Features ... 1
Applications ... 1
Pin Configuration ... 1
General Description ... 1
Revision History ... 2
Specifications ... 3
Electrical Characteristics ... 3
Absolute Maximum Ratings ... 6
Thermal Resistance ... 6
ESD Caution ... 6
Typical Performance Characteristics ... 7
Theory of Operation ... 12
Power Consumption vs. Bandwidth ... 12
Driving Capacitive Loads ... 13
Full Power Bandwidth ... 13
A Micropower Reference Voltage Generator ... 14
A 100 kHz Single-Supply Second-Order Band-Pass Filter ... 14
Wien Bridge Oscillator ... 15
Outline Dimensions ... 16
Ordering Guide ... 16

REVISION HISTORY

1/2017—Rev. D to Rev. E

Changes to Ordering Guide ... 16

7/2007—Rev. C to Rev. D

Changes to Ordering Guide ... 16
Updated Package Designator Throughout ... 1
Changes to Table 1, Supply Current/Amplifier ... 3

7/2007—Rev. C to Rev. D

Updated Format ... Universal
Updated Package Designator Throughout ... 1
Changes to Table 1, Supply Current/Amplifier ... 3
Changes to Table 2, Supply Current/Amplifier ... 4
Changes to Table 3, Large Signal Voltage Gain, Power Supply Rejection Ratio, and Supply Current/Amplifier ... 5
Changes to Figure 10 ... 8
Changes to Figure 35 ... 14
Updated Outline Dimensions ... 16
Changes to Ordering Guide ... 16

3/2005—Rev. B to Rev. C

Changes to Specifications ... 2
Changes to Ordering Guide ... 5

4/2003—Rev. A to Rev. B

Change to Figure 5 ... 12

2/2003—Rev. 0 to Rev. A

Added new SC70 Package ... Universal
Changes to Features ... 1
Changes to General Description ... 1
Changes to Pin Configuration ... 1
Changes to Specifications ... 2
Changes to Absolute Maximum Ratings ... 5
Changes to Ordering Guide ... 5
Changes to TPC 3 ... 6
Changes to TPC 10 ... 7
Changes to TPC 13 ... 8
Changes to TPC 27 ... 10
Changes to TPC 28 ... 10
Added new TPC 29 ... 10
Changes to Functional Description ... 11
Updated to Outline Dimensions ... 14

8/2002—Revision. 0: Initial Version

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_S = 1.8 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = V_S/2$		1	6	mV
		−40°C < T_A < +125°C			8	mV
Input Bias Current	I_B	V_S = 1.8 V		2	30	pA
		−40°C < T_A < +85°C			600	pA
		−40°C < T_A < +125°C			8	nA
Input Offset Current	I_{OS}			1	10	pA
		−40°C < T_A < +125°C			500	pA
Input Voltage Range			0		1.8	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 1.8 V	50			dB
		−40°C < T_A < +125°C	47			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, 0.3 V ≤ V_{OUT} ≤ 1.5 V	110	400		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 100 µA, −40°C < T_A < +125°C	1.79			V
		I_L = 750 µA, −40°C < T_A < +125°C	1.77			V
Output Voltage Low	V_{OL}	I_L = 100 µA, −40°C < T_A < +125°C			10	mV
		I_L = 750 µA, −40°C < T_A < +125°C			30	mV
Short-Circuit Limit	I_{SC}			20		mA
POWER SUPPLY						
Supply Current/Amplifier	I_{SY}	$V_{OUT} = V_S/2$		325	450	µA
		−40°C < T_A < +125°C			500	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		2.7		V/µs
Gain Bandwidth Product	GBP			5		MHz
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		22		nV/√Hz
		f = 10 kHz		20		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05		pA/√Hz

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V_S = 3.0 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = V_S/2$		1	6	mV
		−40°C < T_A < +125°C			8	mV
Input Bias Current	I_B	V_S = 3.0 V		2	30	pA
		−40°C < T_A < +85°C			600	pA
		−40°C < T_A < +125°C			8	nA
Input Offset Current	I_{OS}			1	10	pA
		−40°C < T_A < +125°C			500	pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 3.0 V	54			dB
		−40°C < T_A < +125°C	50			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, 0.3 V ≤ V_{OUT} ≤ 2.7 V	250	1000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 100 µA, −40°C < T_A < +125°C	2.99			V
		I_L = 750 µA, −40°C < T_A < +125°C	2.98			V
Output Voltage Low	V_{OL}	I_L = 100 µA, −40°C < T_A < +125°C			10	mV
		I_L = 750 µA, −40°C < T_A < +125°C			20	mV
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 1.8 V to 5.0 V	65	85		dB
		−40°C < T_A < +125°C	57	80		dB
Supply Current/Amplifier	I_{SY}	$V_{OUT} = V_S/2$		350	450	µA
		−40°C < T_A < +125°C			500	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		2.7		V/µs
Gain Bandwidth Product	GBP			5		MHz
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		22		nV/√Hz
		f = 10 kHz		20		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05		pA/√Hz

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V_S = 5.0 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = V_S/2$		1	6	mV
		−40°C < T_A < +125°C			8	mV
Input Bias Current	I_B	V_S = 5.0 V		5	30	pA
		−40°C < T_A < +85°C			600	pA
		−40°C < T_A < +125°C			8	nA
Input Offset Current	I_{OS}			1	10	pA
		−40°C < T_A < +125°C			500	pA
Input Voltage Range			0		5.0	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 5.0 V	60	75		dB
		−40°C < T_A < +125°C	54			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, 0.3 V ≤ V_{OUT} ≤ 4.7 V	450	2000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
OUTPUT CHARACTERISTICS			4.99			
Output Voltage High	V_{OH}	I_L = 100 µA, −40°C < T_A < +125°C	4.98			V
		I_L = 750 µA, −40°C < T_A < +125°C				V
Output Voltage Low	V_{OL}	I_L = 100 µA, −40°C < T_A < +125°C			10	mV
		I_L = 750 µA, −40°C < T_A < +125°C			20	mV
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 1.8 V to 5.0 V	65	85		dB
		−40°C < T_A < +125°C	57	80		dB
Supply Current/Amplifier	I_{SY}	$V_{OUT} = V_S/2$		410	550	µA
		−40°C < T_A < +125°C			600	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		2.7		V/µs
Gain Bandwidth Product	GBP			5		MHz
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		22		nV/√Hz
		f = 10 kHz		20		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05		pA/√Hz

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to V_S
Differential Input Voltage	±6 V or ±V_S
Output Short-Circuit Duration to GND	Observe derating curves
Storage Temperature Range	
KS and RJ Packages	−65°C to +150°C
Operating Temperature Range	
AD8515	−40°C to +125°C
Junction Temperature Range	
KS and RJ Packages	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
5-Lead SOT-23 (RJ)	230	146	°C/W
5-Lead SC70 (KS)	376	126	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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TYPICAL PERFORMANCE CHARACTERISTICS

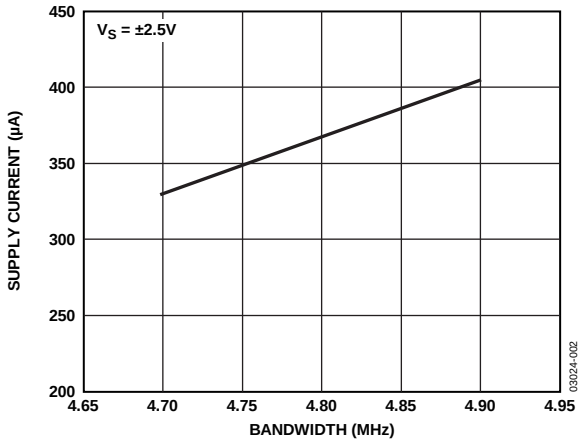

Figure 2. Supply Current vs. Bandwidth

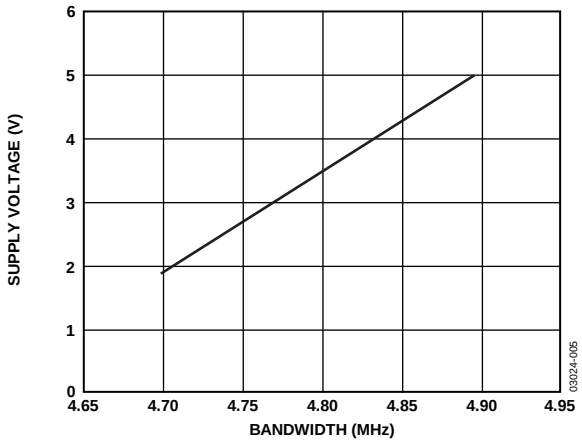

Figure 5. Supply Voltage vs. Bandwidth

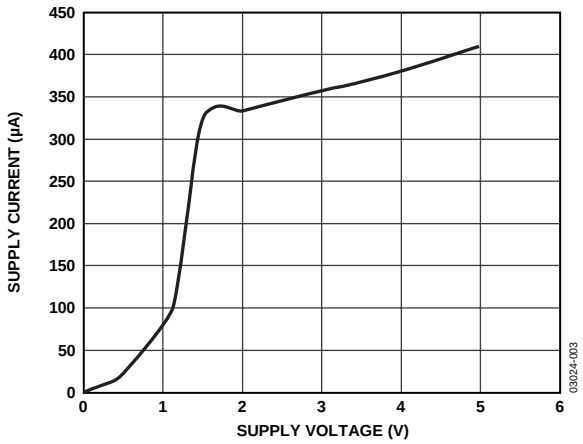

Figure 3. Supply Current vs. Supply Voltage

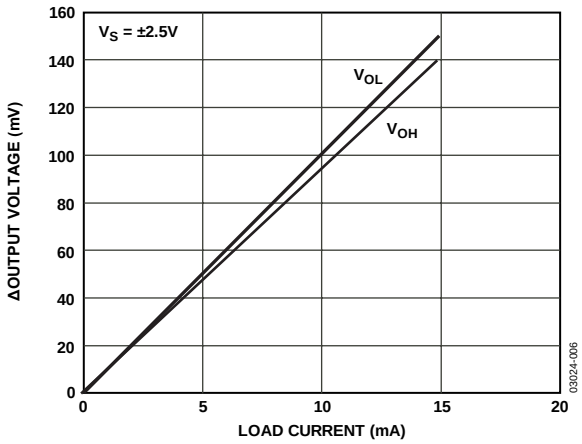

Figure 6. Output Voltage to Supply Rail vs. Load Current

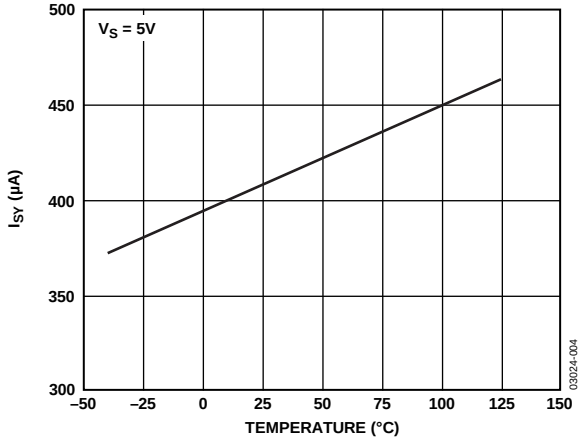

Figure 4. I_{SY} vs. Temperature

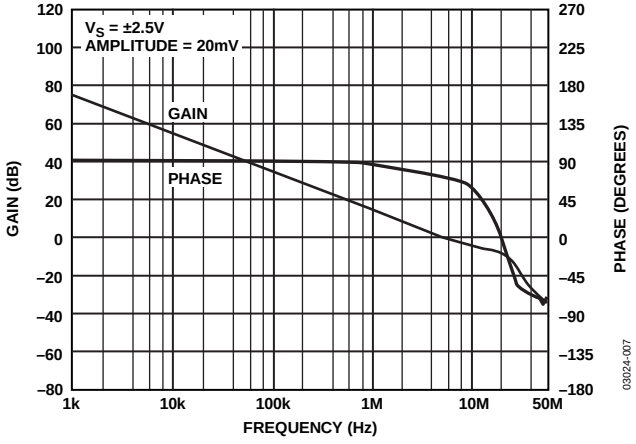

Figure 7. Gain and Phase vs. Frequency

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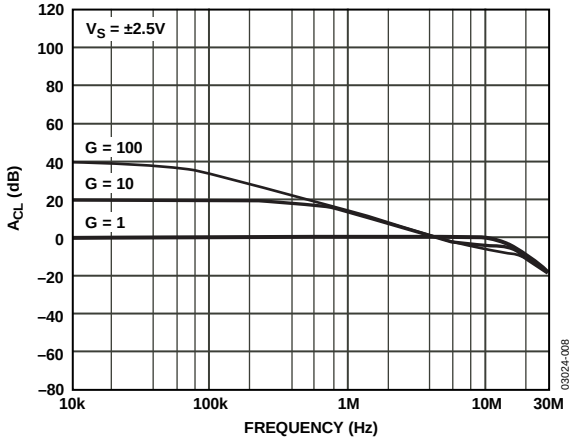

Figure 8. A_{CL} vs. Frequency

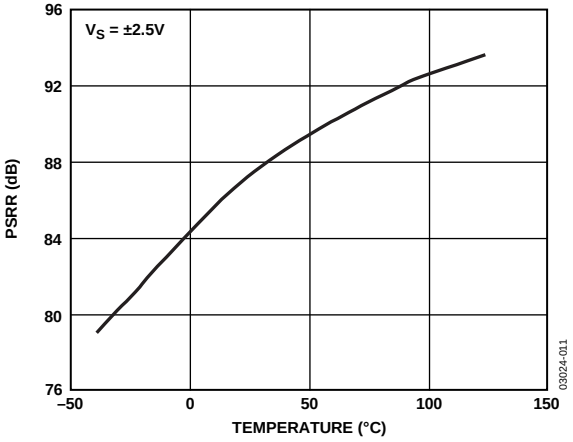

Figure 11. PSRR vs. Temperature

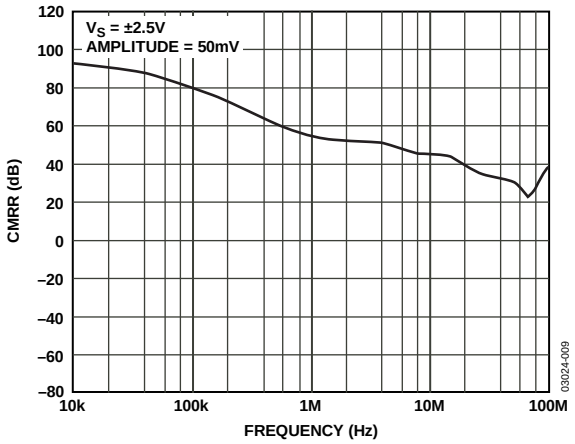

Figure 9. CMRR vs. Frequency

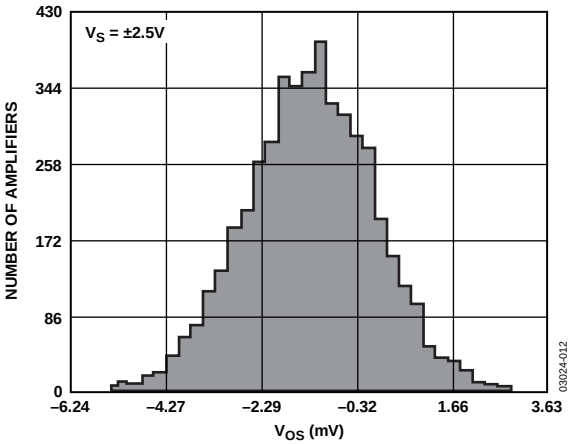

Figure 12. V_{OS} Distribution

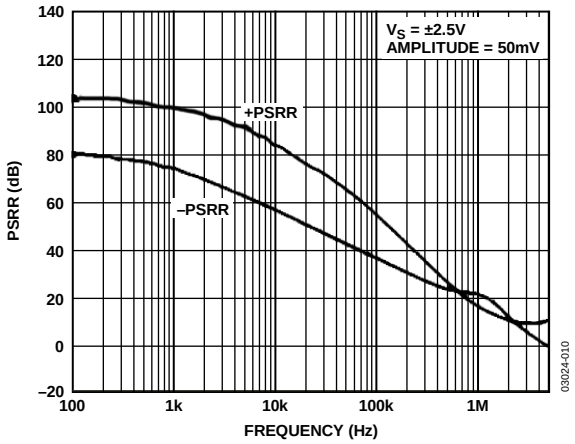

Figure 10. PSRR vs. Frequency

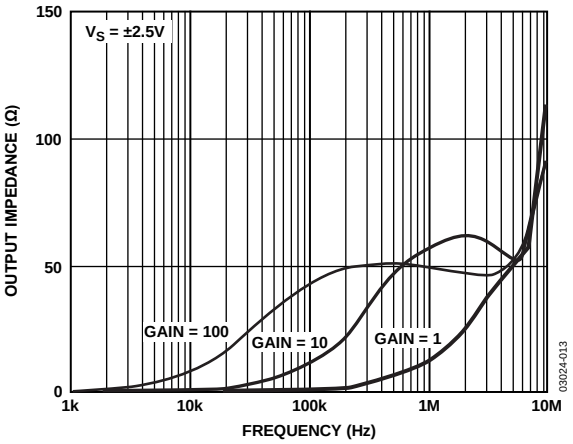

Figure 13. Output Impedance vs. Frequency

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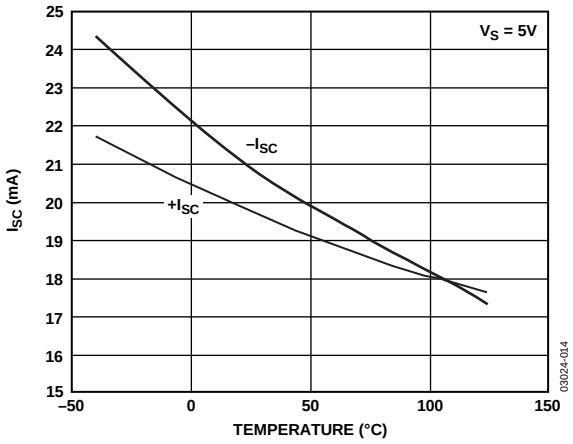

Figure 14. I_{SC} vs. Temperature

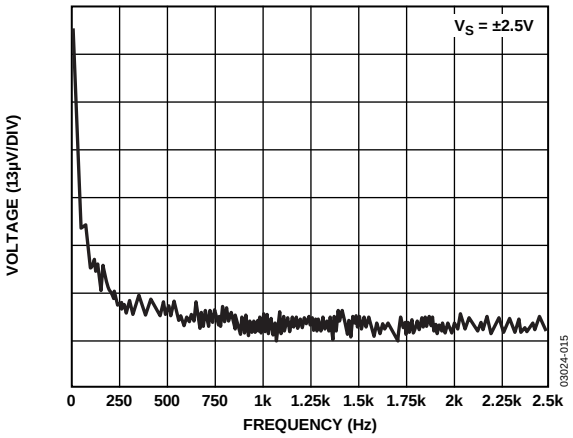

Figure 15. Voltage Noise Density

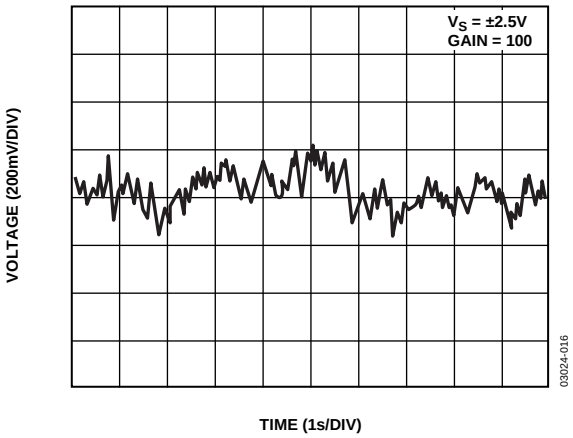

Figure 16. Input Voltage Noise

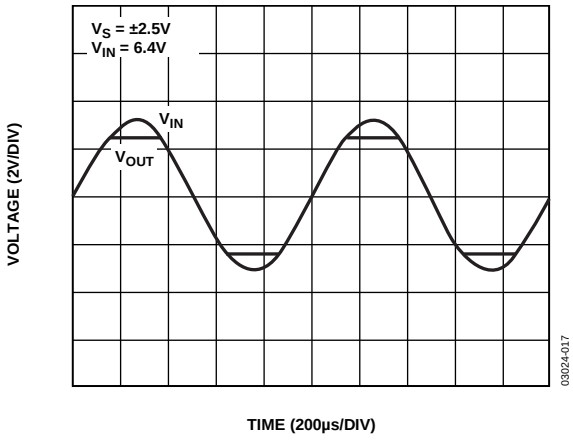

Figure 17. No Phase Reversal

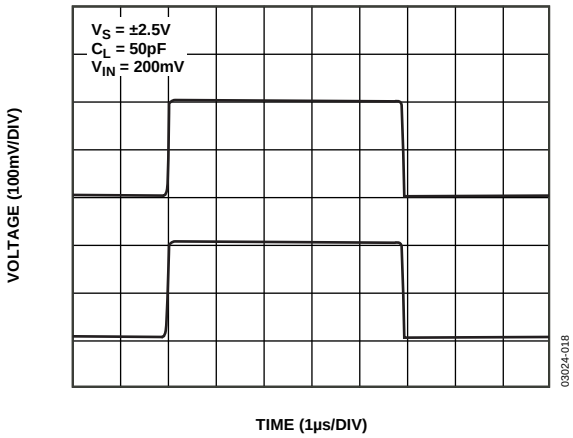

Figure 18. Small Signal Transient Response

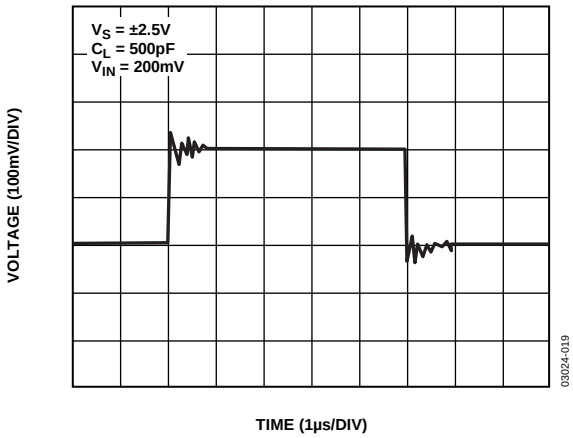

Figure 19. Small Signal Transient Response

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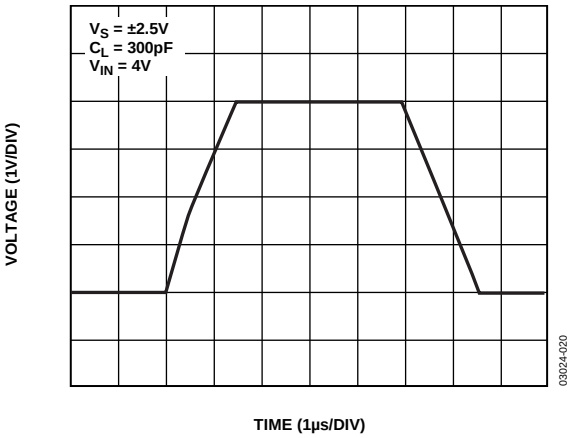

Figure 20. Large Signal Transient Response

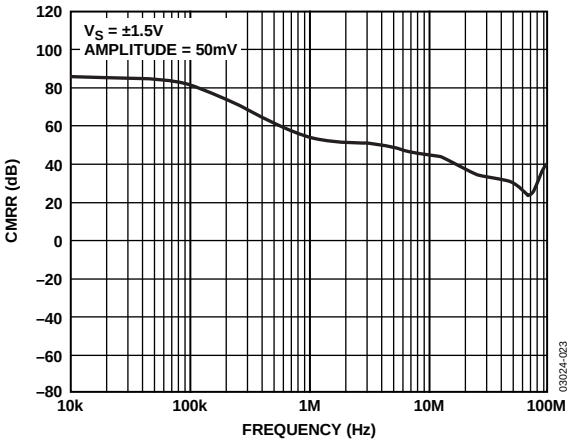

Figure 23. CMRR vs. Frequency

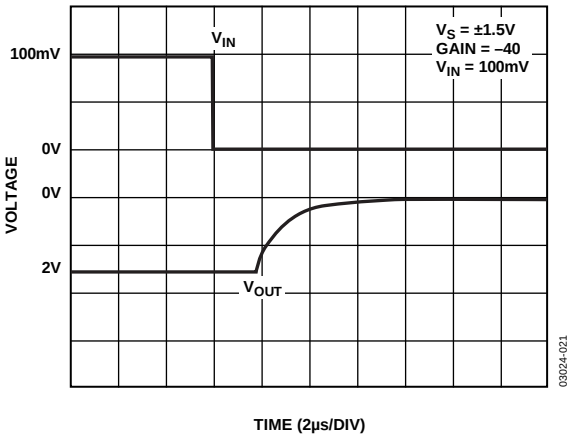

Figure 21. Saturation Recovery

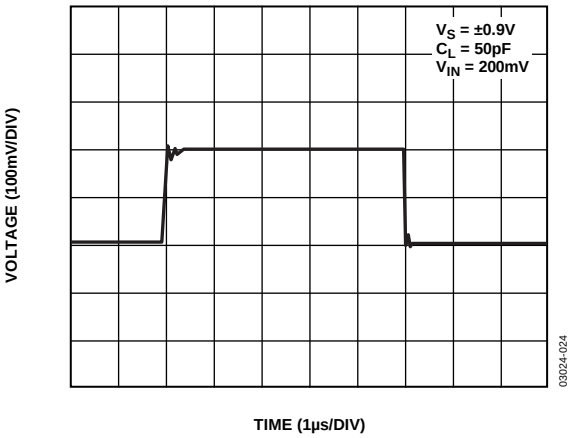

Figure 24. Small Signal Transient Response

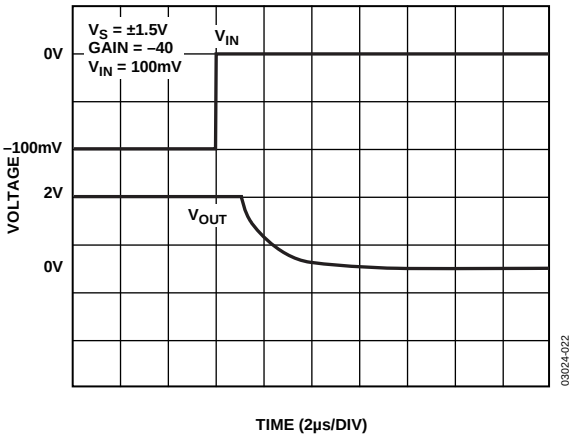

Figure 22. Saturation Recovery

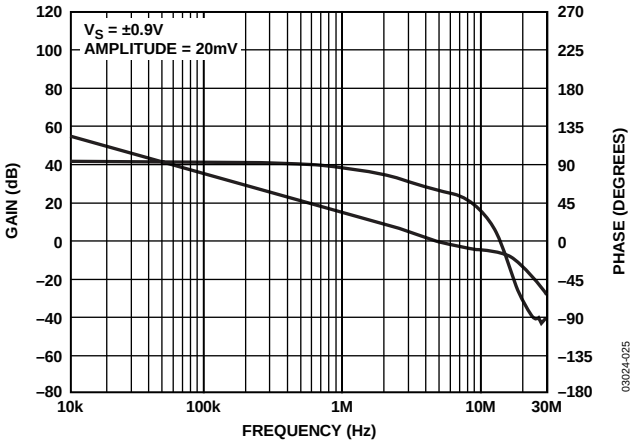

Figure 25. Gain and Phase vs. Frequency

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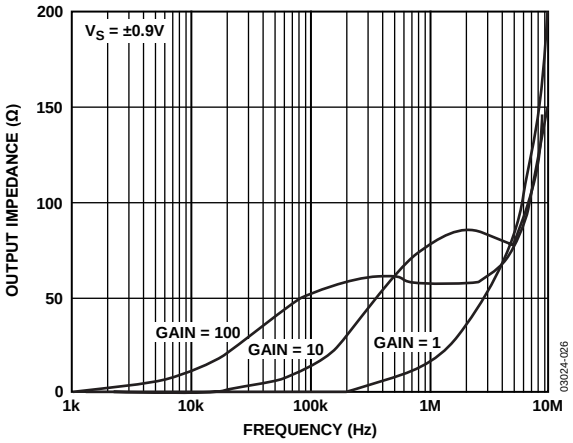

Figure 26. Output Impedance vs. Frequency

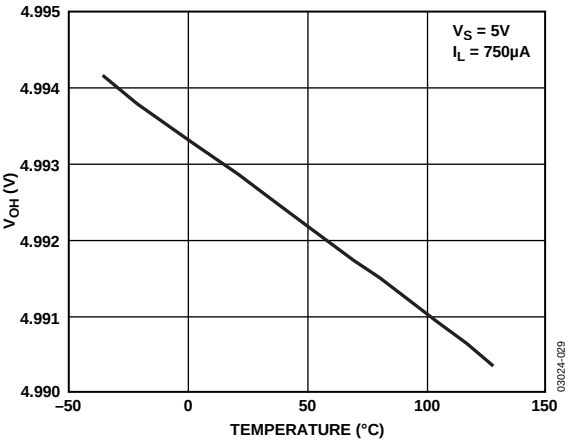

Figure 29. V_{OH} vs. Temperature

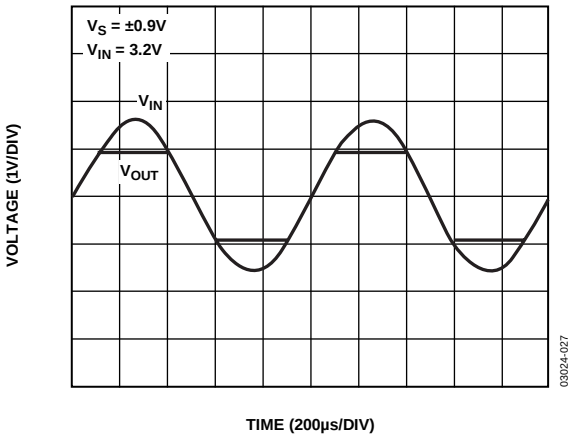

Figure 27. No Phase Reversal

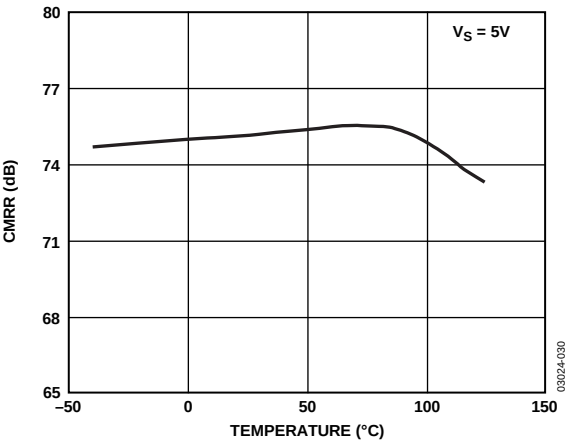

Figure 30. CMRR vs. Temperature

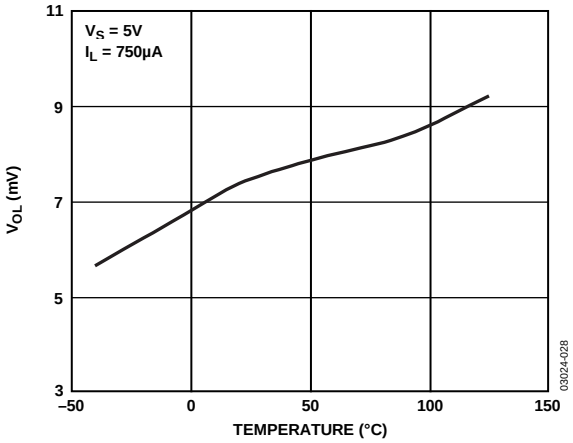

Figure 28. V_{OL} vs. Temperature

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THEORY OF OPERATION

The AD8515, offered in space-saving SOT-23 and SC70 packages, is a rail-to-rail input and output operational amplifier that can operate at supply voltages as low as 1.8 V. This product is fabricated using 0.6 micron CMOS to achieve one of the best power consumption-to-speed ratios (that is, bandwidth) in the industry. With a small amount of supply current (less than 400 μA), a wide unity gain bandwidth of 4.5 MHz is available for signal processing.

The input stage consists of two parallel, complementary, differential pairs of PMOS and NMOS. The AD8515 exhibits no phase reversal because the input signal exceeds the supply by more than 0.6 V. Currents into the input pin must be limited to 5 mA or less by the use of external series resistance(s). The AD8515 has a very robust ESD design and can stand ESD voltages of up to 4000 V.

POWER CONSUMPTION vs. BANDWIDTH

One of the strongest features of the AD8515 is the bandwidth stability over the specified temperature range while consuming small amounts of current. This effect is shown in Figure 2 through Figure 4.

This product solves the speed/power requirements for many applications. The wide bandwidth is also stable even when operated with low supply voltages. Figure 5 shows the relationship between the supply voltage vs. the bandwidth for the AD8515.

The AD8515 is ideal for battery-powered instrumentation and handheld devices because it can operate at the end of discharge voltage of most popular batteries. Table 6 lists the nominal and end of discharge voltages of several typical batteries.

Table 6. Typical Battery Life Voltage Range

Battery	Nominal Voltage (V)	End of Discharge Voltage (V)
Lead-Acid	2	1.8
Lithium	2.6 to 3.6	1.7 to 2.4
NiMH	1.2	1
NiCd	1.2	1
Carbon-Zinc	1.5	1.1

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DRIVING CAPACITIVE LOADS

Most amplifiers have difficulty driving large capacitive loads. Additionally, higher capacitance at the output can increase the amount of overshoot and ringing in the amplifier's step response and can even affect the stability of the device. This is due to the degradation of phase margin caused by additional phase lag from the capacitive load. The value of capacitive load that an amplifier can drive before oscillation varies with gain, supply voltage, input signal, temperature, and other parameters. Unity gain is the most challenging configuration for driving capacitive loads. The AD8515 is capable of driving large capacitive loads without any external compensation. The graphs in Figure 31 and Figure 32 show the amplifier's capacitive load driving capability when configured in unity gain of +1.

The AD8515 is even capable of driving higher capacitive loads in inverting gain of −1, as shown in Figure 33.

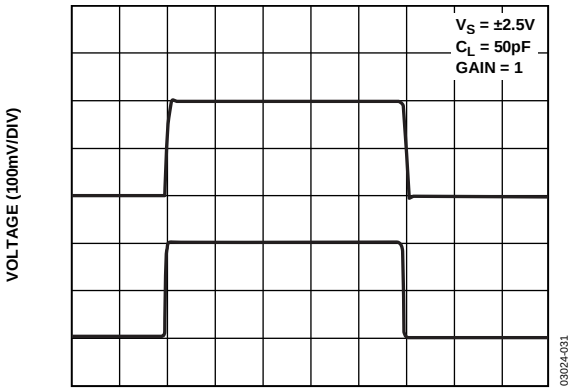

Figure 31. Capacitive Load Driving @ C_L = 50 pF

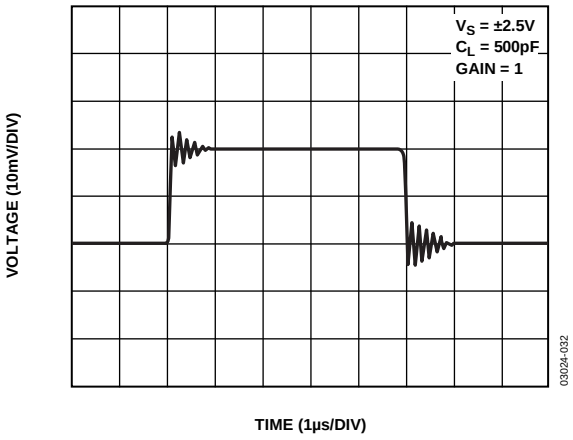

Figure 32. Capacitive Load Driving @ C_L = 500 pF

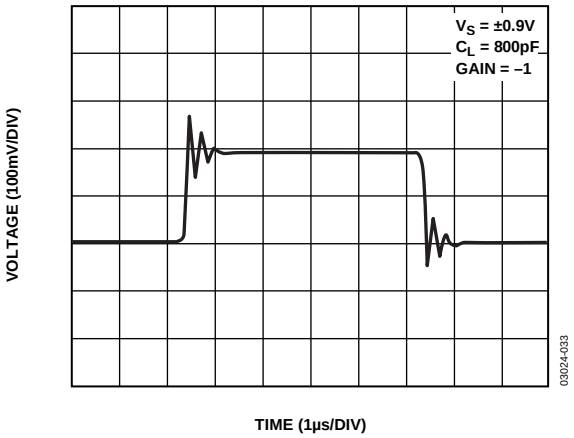

Figure 33. Capacitive Load Driving @ C_L = 800 pF

FULL POWER BANDWIDTH

The slew rate of an amplifier determines the maximum frequency at which it can respond to a large input signal. This frequency (known as full power bandwidth, FPBW) can be calculated from the equation

$$FPBW = \frac{SR}{2\pi \times V_{PEAK}}$$

for a given distortion. The FPBW of the AD8515 is shown in Figure 34 to be close to 200 kHz.

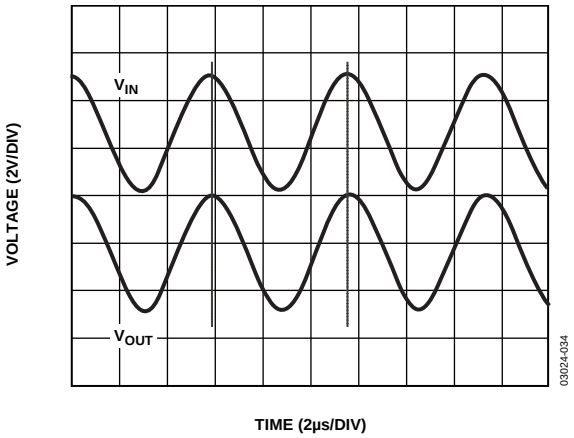

Figure 34. Full Power Bandwidth

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A MICROPOWER REFERENCE VOLTAGE GENERATOR

Many single-supply circuits are configured with the circuit biased to one-half of the supply voltage. In these cases, a false ground reference can be created by using a voltage divider buffered by an amplifier. Figure 35 shows the schematic for such a circuit. The two 1 MΩ resistors generate the reference voltages while drawing only 0.9 µA of current from a 1.8 V supply. A capacitor connected from the inverting terminal to the output of the op amp provides compensation to allow for a bypass capacitor to be connected at the reference output. This bypass capacitor helps establish an ac ground for the reference output.

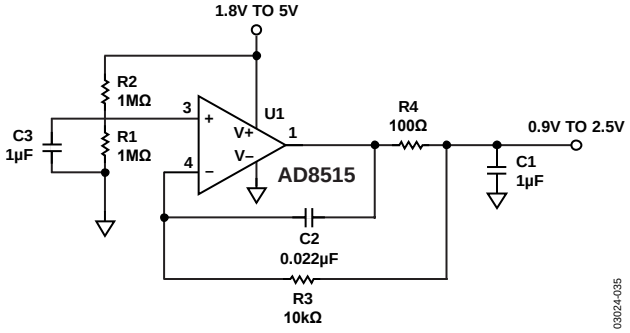

Figure 35. Micropower Voltage Reference Generator

A 100 kHz SINGLE-SUPPLY SECOND-ORDER BAND-PASS FILTER

The circuit in Figure 36 is commonly used in portable applications where low power consumption and wide bandwidth are required. This figure shows a circuit for a single-supply band-pass filter with a center frequency of 100 kHz. It is essential that the op amp have a loop gain at 100 kHz to maintain an accurate center frequency. This loop gain requirement necessitates the choice of an op amp with a high unity gain crossover frequency, such as the AD8515. The 4.5 MHz bandwidth of the AD8515 is sufficient to accurately produce the 100 kHz center frequency, as the response in Figure 37 shows. When the op amp bandwidth is close to the center frequency of the filter, the amplifier internal phase shift causes excess phase shift at 100 kHz, altering the filter response. In fact, if the chosen op amp has a bandwidth close to 100 kHz, the phase shift of the op amps causes the loop to oscillate.

A common-mode bias level is easily created by connecting the noninverting input to a resistor divider consisting of two resistors connected between VCC and ground. This bias point is also decoupled to ground with a 1 µF capacitor.

$$f_L = \frac{1}{2\pi \times R1 \times C1}$$

$$f_H = \frac{1}{2\pi \times R1 \times C1}$$

$$H_0 = 1 + \frac{R1}{R2}$$

$$VCC = 1.8\ \text{V} - 5\ \text{V}$$

where:
f_L is the low −3 dB frequency.
f_H is the high −3 dB frequency.
H_0 is the midfrequency gain.

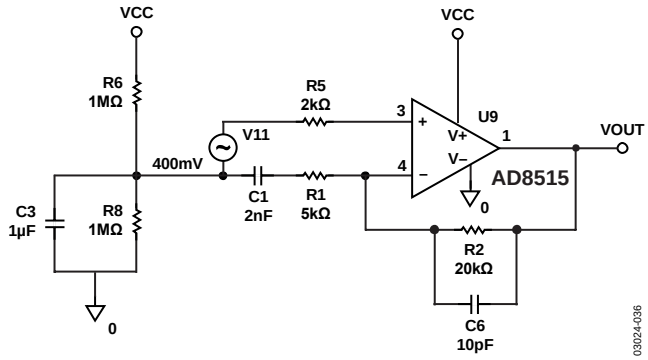

Figure 36. Second-Order Band-Pass Filter

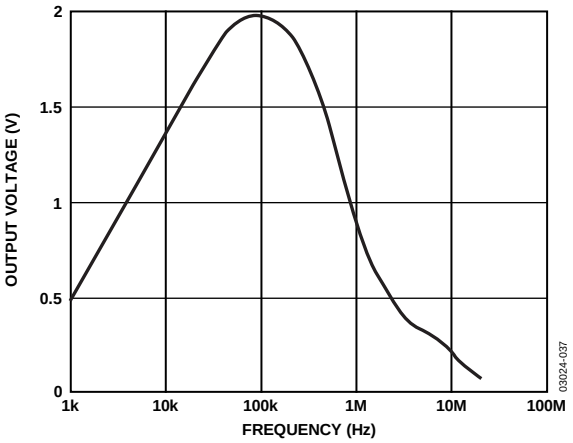

Figure 37. Frequency Response of the Band-Pass Filter

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WIEN BRIDGE OSCILLATOR

The circuit in Figure 38 can be used to generate a sine wave, one of the most fundamental waveforms. Known as a Wien Bridge oscillator, it has the advantage of requiring only one low power amplifier. This is an important consideration, especially for battery-operated applications where power consumption is a critical issue. To keep the equations simple, the resistor and capacitor values used are kept equal. For the oscillation to happen, two conditions have to be met. First, there should be a zero phase shift from the input to the output, which happens at the oscillation frequency of

$$f_{OSC} = \frac{1}{2\pi R10 \times C10}$$

Second, at this frequency, the ratio of VOUT to the voltage at the positive input (+IN, Pin 3) has to be 3, which means that the ratio of R11:R12 should be greater than 2.

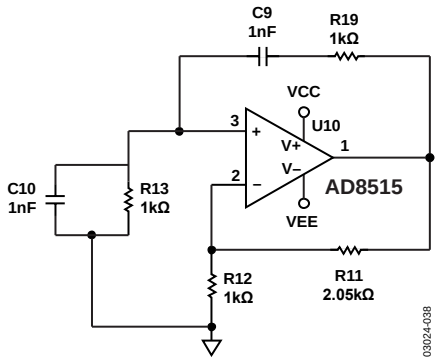

Figure 38. Low Power Wien Bridge Oscillator

High frequency oscillators can be built with the AD8515, due to its wide bandwidth. Using the values shown, an oscillation frequency of 130 kHz is created and is shown in Figure 39. If R11 is too low, the oscillation might converge; if too large, the oscillation diverges until the output clips (V_S = ±2.5 V, f_{OSC} = 130 kHz).

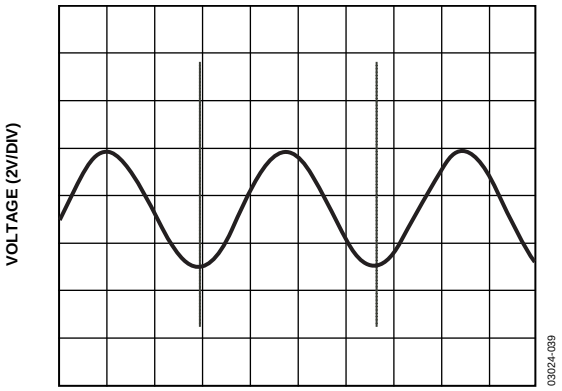

Figure 39. Output of Wien Bridge Oscillator

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OUTLINE DIMENSIONS

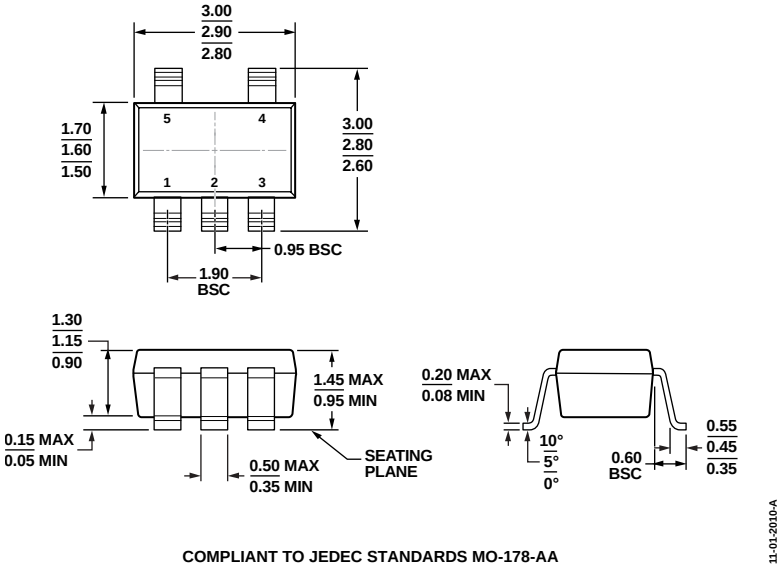

Figure 40. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters

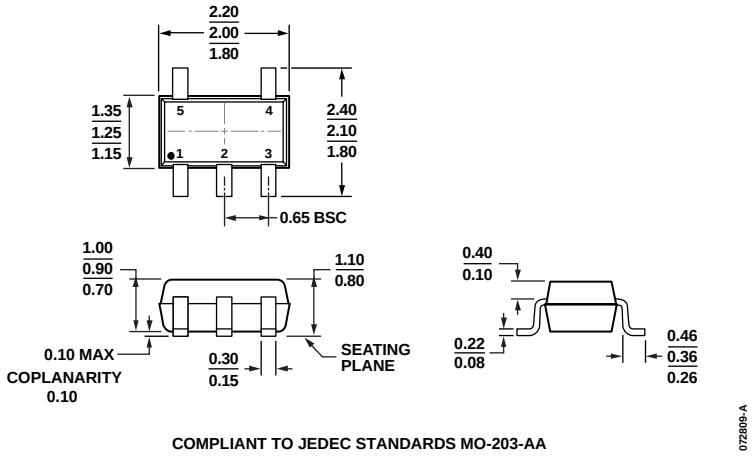

Figure 41. 5-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8515ARTZ-R2[1]	−40°C to +125°C	5-Lead SOT-23	RJ-5
AD8515ARTZ-REEL[1]	−40°C to +125°C	5-Lead SOT-23	RJ-5
AD8515ARTZ-REEL7[1]	−40°C to +125°C	5-Lead SOT-23	RJ-5
AD8515AKSZ-R2[1]	−40°C to +125°C	5-Lead SC70	KS-5
AD8515AKSZ-REEL[1]	−40°C to +125°C	5-Lead SC70	KS-5
AD8515AKSZ-REEL7[1]	−40°C to +125°C	5-Lead SC70	KS-5

[1] Z = RoHS Compliant Part.

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