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5/09—Rev. D to Rev E

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SPECIFICATIONS

T_A = 25°C and $\pm V_S$ = ±5 V, unless otherwise noted; dBm assumes 50 Ω load. Specifications in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Table 1.

Parameters	Conditions	Min	Typ	Max	Unit
MULTIPLIER PERFORMANCE					
Transfer Function			$W = \frac{XY}{(1\text{ V})^2} \times 4\text{ mA}$		
Total Error[1]	−1 V ≤ X, Y < +1 V		±0.5	**±2**	% FS
vs. Temperature (AD834A/AD834S Only)	T_{MIN} to T_{MAX}		±1.5	**±3**	% FS
vs. Supplies (All Models)[2]	±4 V to ±6 V		0.1	**0.3**	% FS/V
Linearity[3]			±0.5	**±1**	% FS
Bandwidth[4]		500			MHz
Feedthrough, X	X = ±1 V, Y = nulled		0.2	**0.3**	% FS
Feedthrough, Y	X = nulled, Y = ±1 V		0.1	**0.2**	% FS
AC Feedthrough, X[5]	X = 0 dBm, Y = nulled				
	f = 10 MHz		−65		dB
	f = 100 MHz		−50		dB
AC Feedthrough, Y[5]	X = nulled, Y = 0 dBm				
	f = 10 MHz		−70		dB
	f = 100 MHz		−50		dB
INPUTS (X1, X2, Y1, Y2)					
Full-Scale Range	Differential		±1		V
Clipping Level	Differential	**±1.1**	±1.3		V
Input Resistance	Differential		25		kΩ
Offset Voltage			0.5	**3**	mV
vs. Temperature	T_{MIN} to T_{MAX}		10		µV/°C
				4	mV
vs. Supplies[2]	±4 V to ±6 V		100	**300**	µV/V
Bias Current			45		µA
Common-Mode Rejection	f ≤ 100 kHz; 1 V p-p		70		dB
Nonlinearity, X	Y = 1 V; X = ±1 V		0.2	**0.5**	% FS
Nonlinearity, Y	X = 1 V; Y = ±1 V		0.1	**0.3**	% FS
Distortion, X	X = 0 dBm, Y = 1 V				
	f = 10 MHz		−60		dB
	f = 100 MHz		−44		dB
Distortion, Y	X = 1 V, Y = 0 dBm				
	f = 10 MHz		−65		dB
	f = 100 MHz		−50		dB
OUTPUTS (W1, W2)					
Zero Signal Current	Each output		8.5		mA
Differential Offset	X = 0, Y = 0		±20	**±60**	µA
vs. Temperature					nA°C
All Models	T_{MIN} to T_{MAX}		40		
AD834A/AD834S Only				**±60**	µA
Scaling Current	Differential	3.96	4	4.04	mA
Output Compliance		4.75		9	V
Noise Spectral Density	f = 10 Hz to 1 MHz		16		nV/√Hz
	Outputs into 50 Ω Load				

Parameters	Conditions	Min	Typ	Max	Unit
POWER SUPPLIES					
Operating Range		±4		±9	V
Quiescent Current[6]	T_{MIN} to T_{MAX}				
$+V_S$			11	**14**	mA
$-V_S$			28	**35**	mA

[1] Error is defined as the maximum deviation from the ideal output, and expressed as a percentage of the full-scale output. See Figure 16.
[2] Both supplies taken simultaneously; sinusoidal input at f ≤10 kHz.
[3] Linearity is defined as residual error after compensating for input offset voltage, output offset current, and scaling current errors.
[4] Bandwidth is guaranteed when configured in squarer mode. See Figure 12.
[5] Sine input; relative to full-scale output; zero input port nulled; represents feedthrough of the fundamental.
[6] Negative supply current is equal to the sum of positive supply current, the signal currents into each output, W1 and W2, and the input bias currents.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Ratings
Supply Voltage ($+V_S$ to $-V_S$)	18 V
Internal Power Dissipation	500 mW
Input Voltages (X1, X2, Y1, Y2)	$+V_S$
Operating Temperature Ranges	
Commercial, AD834J Only	0°C to 70°C
Industrial, AD834A Only	−40°C to +85°C
Military AD834S/883B Only	−55°C to +125°C
Storage Temperature Range (Q)	−65°C to +150°C
Storage Temperature Range (R, N)	−65°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C
ESD Rating	500 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Table 3.

Package	θ_{JA}	θ_{JA}	Unit
8-Lead CERDIP (Q)	110	110	°C/W
8-Lead SOIC (R)	165	165	°C/W
8-Lead PDIP (N)	99	99	°C/W

CHIP DIMENSIONS AND BONDING DIAGRAM

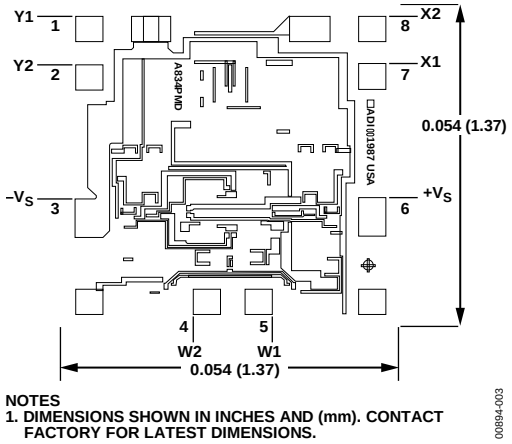


Figure 2. Metallization Photograph

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

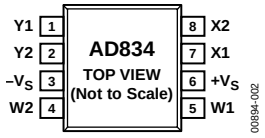


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	Y1	Positive Y Input
2	Y2	Negative Y Input
3	$-V_S$	Negative Power Supply
4	W2	Open-Collector Output
5	W1	Open-Collector Output
6	$+V_S$	Positive Power Supply.
7	X1	Positive X Input
8	X2	Negative X Input

TYPICAL PERFORMANCE CHARACTERISTICS

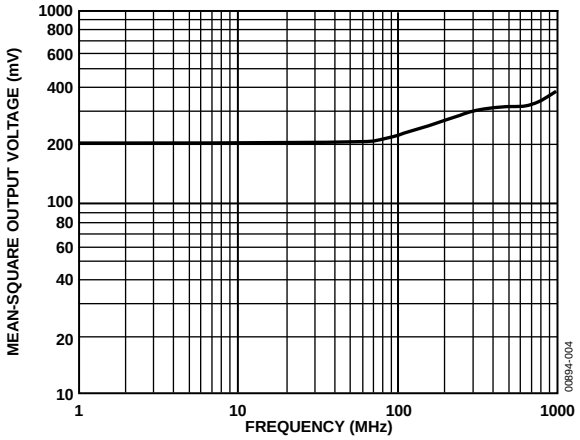


Figure 4. Mean-Square Output vs. Frequency

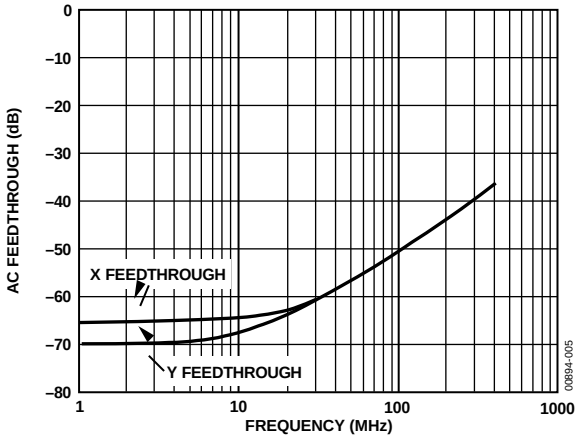


Figure 5. AC Feedthrough vs. Frequency

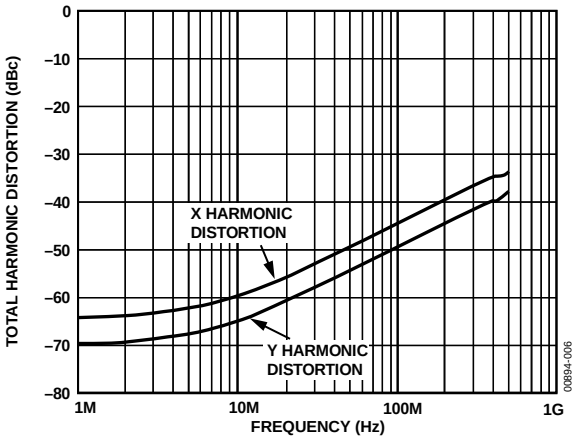


Figure 6. Total Harmonic Distortion vs. Frequency

TEST CIRCUITS

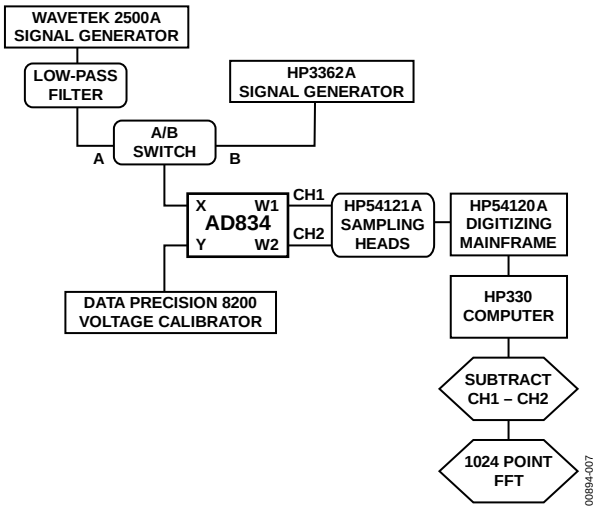


Figure 7. Test Configuration for Measuring AC Feedthrough and Total Harmonic Distortion

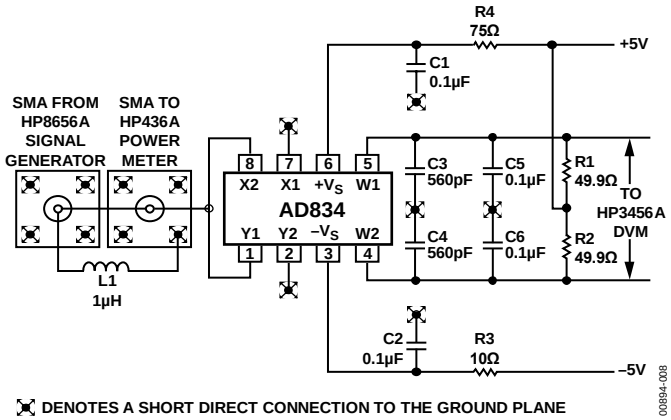
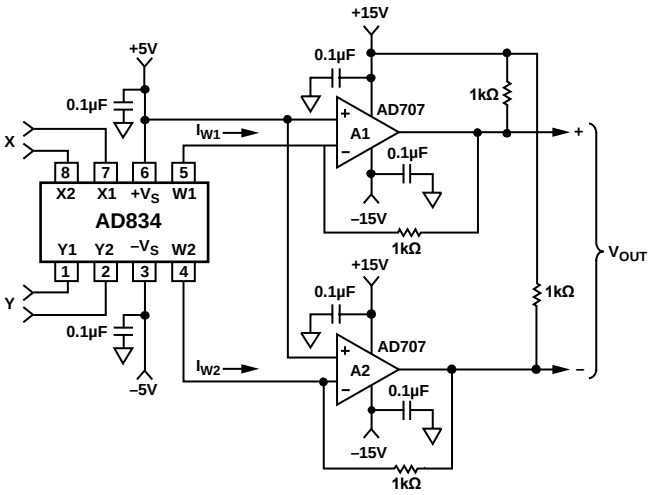


Figure 8. Bandwidth Test Circuit



NOTES
1. R1, R2 SHOULD BE PRECISION TYPE RESISTOR (±0.1%).
2. ABSOLUTE VALUE ERRORS OF R1, R2 CAUSE A SMALL FACTOR ERROR.
3. R1, R2 MISMATCHES ARE EXPRESSED AS LINEARITY ERRORS.
4. $V_{OUT} = I_{W1}$ R1 − U_{W2} R2
(IF R1 = R2, $V_{OUT} = >I_W$ R1).

Figure 9. Low Frequency Test Circuit

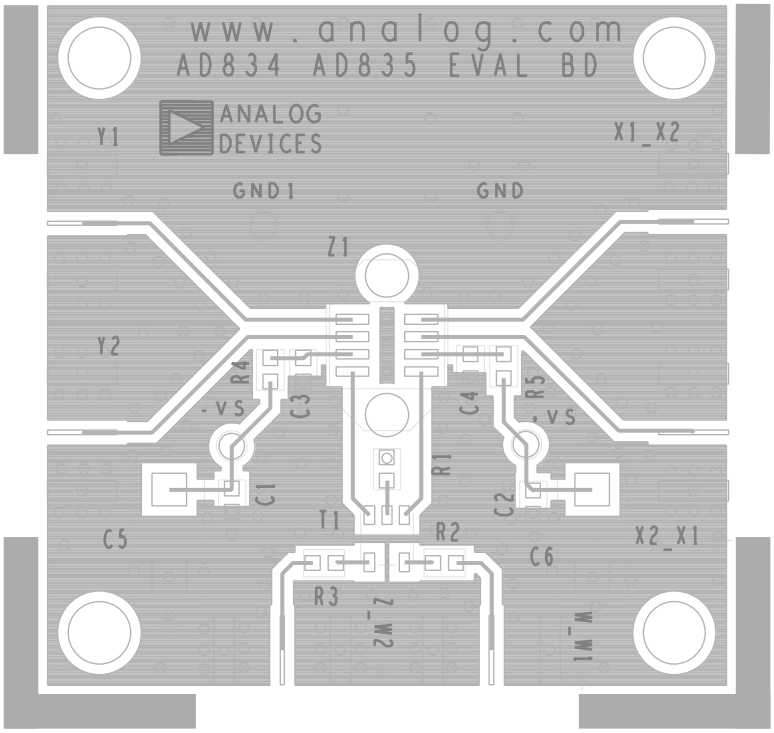


Figure 10. Example Layout for SOIC

EXPLANATION OF TYPICAL PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

Figure 4 is a plot of the mean-square output vs. frequency for the test circuit of Figure 8. Note that the rising response is due to package resonances.

For frequencies above 1 MHz, ac feedthrough is dominated by static nonlinearities in the transfer function and the finite offset voltages. The offset voltages cause a small fraction of the fundamental to appear at the output, and can be nulled out (see Figure 5).

THD data represented in Figure 6 is dominated by the second harmonic, and is generated with 0 dBm input on the ac input and 1 V on the dc input. For a given amplitude on the ac input, THD is relatively insensitive to changes in the dc input amplitude. Varying the ac input amplitude while maintaining a constant dc input amplitude affects THD performance.

The squarer configuration shown in Figure 8 is used to determine wideband performance because it eliminates the need for (and the response uncertainties of) a wideband measurement device at the output. The wideband output of a squarer configuration is a fluctuating current at twice the input frequency with a mean value proportional to the square of the input amplitude.

By placing the capacitors, C3/C5 and C4/C6, across the load resistors, R1 and R2, a simple low-pass filter is formed, and the mean-square value is extracted. The mean-square response can be measured using a DVM connected across R1 and R2.

Care should be taken when laying out the board. When using the DIP package, mount the IC socket on a ground plane with a clear area in the rectangle formed by the pins. This is important because significant transformer action can arise if the pins pass through individual holes in the board; improperly constructed test jigs have caused oscillation at 1.3 GHz.

THEORY OF OPERATION

Figure 11 is a functional equivalent of the AD834. There are three differential signal interfaces: the two voltage inputs (X = X1 − X2 and Y = Y1 − Y2), and the current output (W) which flows in the direction shown in Figure 11 when X and Y are positive. The outputs (W1 and W2) each have a standing current of typically 8.5 mA.

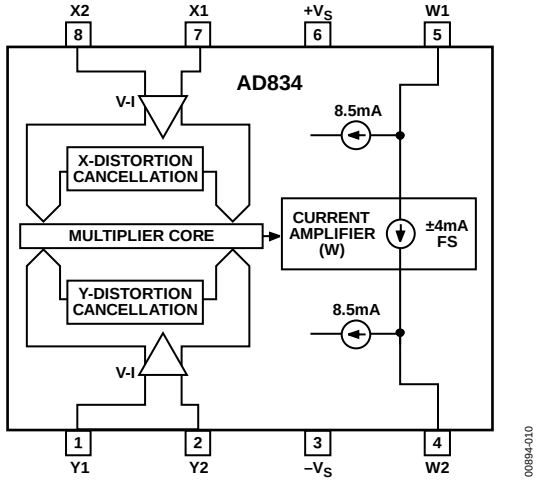


Figure 11. Functional Block Diagram

The input voltages are first converted to differential currents that drive the translinear core. The equivalent resistance of the voltage-to-current (V-I) converters is about 285 Ω, which results in low input related noise and drift. However, the low full-scale input voltage results in relatively high nonlinearity in the V-I converters. This is significantly reduced by the use of distortion cancellation circuits, which operate by Kelvin sensing the voltages generated in the core—an important feature of the AD834.

The current mode output of the core is amplified by a special cascode stage that provides a current gain of nominally × 1.6, trimmed during manufacturing to set up the full-scale output current of ±4 mA. This output appears at a pair of open collectors that must be supplied with a voltage slightly above the voltage on Pin 6. As shown in Figure 12, this can be arranged by inserting a resistor in series with the supply to Pin 6 and taking the load resistors to the full supply. With R3 = 60 Ω, the voltage drop across it is about 600 mV. Using two 50Ω load resistors, the full-scale differential output voltage is ±400 mV. For best performance, the voltage on the output open-collectors (Pin 4 and Pin 5) must be higher than the voltage on Pin 6 by about 200 mV, as shown in Figure 12.

The full bandwidth potential of the AD834 can be realized only when very careful attention is paid to grounding and decoupling. The device must be mounted close to a high quality ground plane and all lead lengths must be extremely short, in keeping with UHF circuit layout practice. In fact, the AD834 shows useful response to well beyond 1 GHz, and the actual upper frequency in a typical application is usually determined by the care with which the layout is affected. Note that R4 (in series with the $-V_S$ supply) carries about 30 mA and thus introduces a voltage drop of about 150 mV. It is made large enough to reduce the Q of the resonant circuit formed by the supply lead and the decoupling capacitor. Slightly larger values can be used, particularly when using higher supply voltages. Alternatively, lossy RF chokes or ferrite beads on the supply leads may be used.

For best performance, use termination resistors at the inputs, as shown in Figure 12. Note that although the resistive component of the input impedance is quite high (about 25 kΩ), the input bias current of typically 45 µA can generate significant offset voltages if not compensated. For example, with a source and termination resistance of 50 Ω (net source of 25 Ω) the offset is 25 Ω × 45 µA = 1.125 mV. The offset can be almost fully cancelled by including (in this example) another 25 Ω resistor in series with the unused input. (In Figure 12, a 25 Ω resistor would be added from X1 to GND and Y2 to GND.) To minimize crosstalk, ground the input pins closest to the output (X1 and Y2); the effect is merely to reverse the phase of the X input and thus alter the polarity of the output.

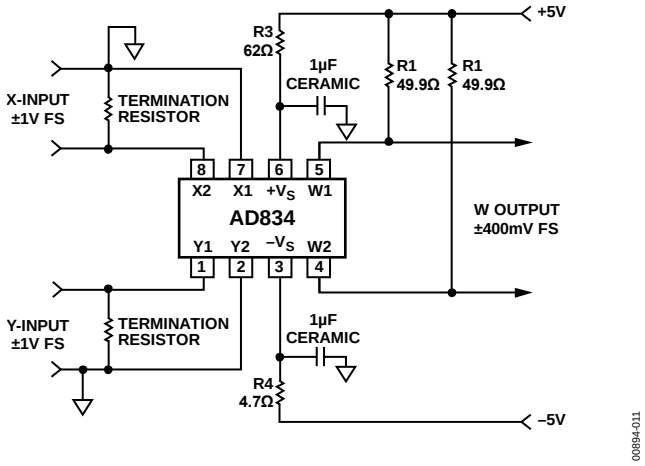


Figure 12. Basic Connections for Wideband Operation

TRANSFER FUNCTION

The Output Current W is the linear product of input voltages (X and Y) divided by $(1\ V)^2$ and multiplied by the scaling current of 4 mA:

$$W = \frac{XY}{(1\ V)^2} 4\ mA$$

With the understanding that the inputs are specified in volts, the following simplified expression can be used:

$$W = (XY)4\ mA$$

Alternatively, the full transfer function can be written as

$$W = \frac{XY}{1\ V} \times \frac{1}{250\ \Omega}$$

When both inputs are driven to their clipping level of about 1.3 V, the peak output current is roughly doubled to ±8 mA, but distortion levels become very high.

BIASING THE OUTPUT

The AD834 has two open collector outputs as shown in Figure 13. The $+V_S$ pin, Pin 6, is tied to the base of the output NPN transistors. The following general guidelines maximize performance of the AD834.

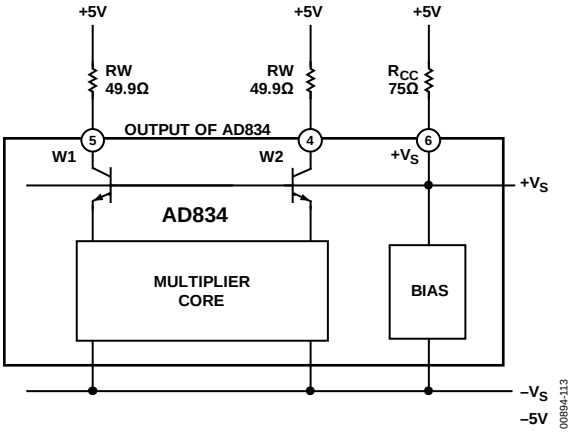


Figure 13. Output Stage Block Diagram

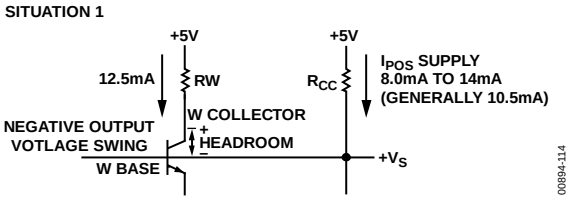


Figure 14. Negative Swing

Figure 14 shows the currents at the input when the AD834 swings negative. Generally, $+V_S$ should be biased at +4 V or higher. For best performance, use resistor values that do not saturate the output transistors. Allowing for adequate transistor headroom reduces distortion.

$$Headroom = Voltage\ at\ W_{COLLECTOR} - Voltage\ at\ W_{BASE}$$

When either output swings negative, the maximum current flows through the RW resistors. It is in this situation that headroom is at a minimum.

$$Headroom_{NEGATIVE\ SWING} = (I_{POS}\ SUPPLY \times R_{CC}) - (12.5\ mA \times RW)$$

Try to keep headroom at or above 200 mV to maintain adequate range. *Headroom ≥ 200 mV.*

This recommendation addresses the positive swing of the output as shown in Figure 15. It is sometimes difficult to meet this for negative output swing.

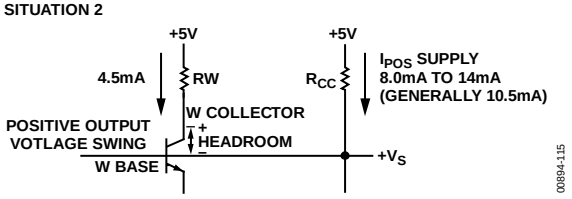


Figure 15. Positive Output Swing

The current through RW is smaller for positive output swings.

$$Headroom_{POSITIVE\ SWING} = (I_{POS}\ SUPPLY \times R_{CC}) - (4.5\ mA \times RW)$$

For dc applications or applications where distortion is not a concern, the headroom may be zero or as low as −200 mV. However, for most cases, size the resistors to give the output adequate headroom.

TRANSFORMER COUPLING

In many high frequency applications where baseband operation is not required at either inputs or the output, transformer coupling can be used. Figure 16 shows the use of a center-tapped output transformer, which provides the necessary dc load condition at the outputs, W1 and W2, and is designed to match into the desired load impedance by appropriate choice of turns ratio. The specific choice of the transformer design depends entirely on the application. Transformers can also be used at the inputs. Center-tapped transformers can reduce high frequency distortion and lower HF feedthrough by driving the inputs with balanced signals.

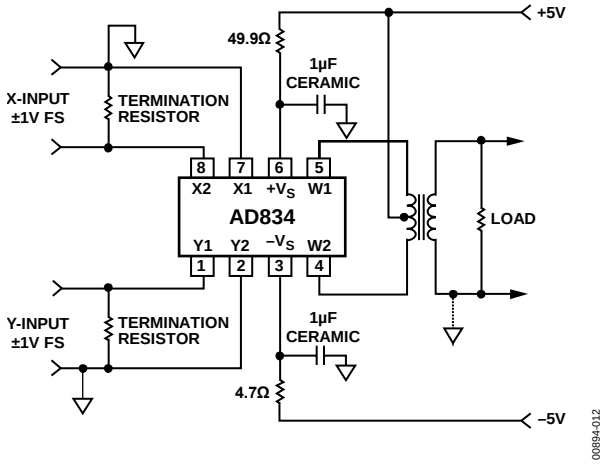


Figure 16. Transformer-Coupled Output

A particularly effective type of transformer is the balun[1], which is a short length of transmission line wound onto a toroidal ferrite core. Figure 17 shows this arrangement used to convert the bal(anced) output to an un(balanced) one (therefore, the use of the term). Although the symbol used is identical to that for a transformer, the mode of operation is quite different. First, the load should now be equal to the characteristic impedance of the line (although this is usually not critical for short line lengths). The collector load resistors, R_W, can also be chosen to reverse-terminate the line, but again this is only necessary when an electrically long line is used. In most cases, R_W is made as large as the dc conditions allow to minimize power loss to the load. The line can be a miniature coaxial cable or a twisted pair.

[1] For a good treatment of baluns, see *Transmission Line Transformers* by Jerry Sevick; American Radio Relay League publication.

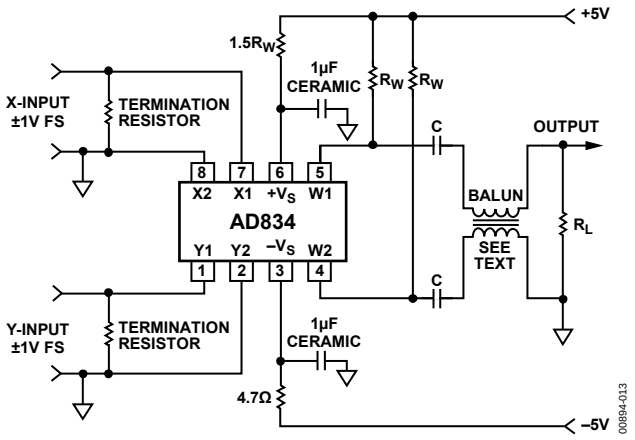


Figure 17. Using a Balun at the Output

Note that the upper bandwidth limit of the balun is determined only by the quality of the transmission line; therefore, the upper bandwidth of the balun usually exceeds that of the multiplier. This is unlike a conventional transformer where the signal is conveyed as a flux in a magnetic core and is limited by core losses and leakage inductance. The lower limit on bandwidth is determined by the series inductance of the line, taken as a whole, and the load resistance (if the blocking capacitors, C, are sufficiently large). In practice, a balun can provide excellent differential-to-single-sided conversion over much wider bandwidths than a transformer.

WIDEBAND MULTIPLIER CONNECTIONS

When operation down to dc and a ground based output are necessary, the configuration shown in Figure 18 can be used. The element values were chosen in this example to result in a full-scale output of ±1 V at the load, so the overall multiplier transfer function is

$$W = (X1 - X2)(Y1 - Y2)$$

where the *X1*, *X2*, *Y1*, *Y2* inputs and *W* output are in volts. The polarity of the output can be reversed simply by reversing either the X or Y input.

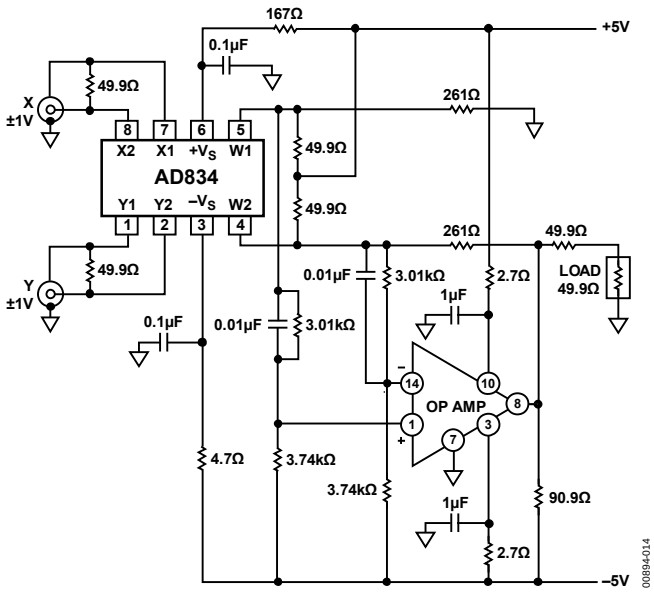


Figure 18. Sideband DC-Coupled Multiplier

Choose the op amp to support the desired output bandwidth. The op amp originally used in Figure 18 was the AD5539, providing an overall system bandwidth of 100 MHz. The AD8009 should provide similar performance. Many other choices are possible where lower post multiplication bandwidths are acceptable. The level shifting network places the input nodes of the op amp to within a few hundred millivolts of ground using the recommended balanced supplies. The output offset can be nulled by including a 100 Ω trim pot between each of the lower pair of resistors (3.74 kΩ) and the negative supply.

The pulse response for this circuit is shown in Figure 19; the X input is a pulse of 0 V to 1 V and the Y input is 1 V dc. The transition times at the output are about 4 ns.

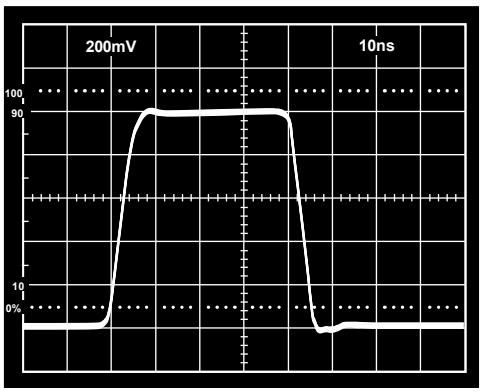


Figure 19. Pulse Response for the Circuit of Figure 18

POWER MEASUREMENT (MEAN-SQUARE AND RMS)

The AD834 is well-suited to measurement of average power in high frequency applications, connected either as a multiplier for the determination of the V × I product, or as a squarer for use with a single input. In these applications, the multiplier is followed by a low-pass filter to extract the long-term average value. Where the bandwidth extends to several hundred megahertz, the first pole of this filter should be formed by grounded capacitors placed directly at the output pins, W1 and W2. This pole can be at a few kilohertz. The effective multiplication or squaring bandwidth is then limited solely by the AD834, because the active circuitry that follows the multiplier is required to process only low frequency signals. Using the device as a squarer, like the circuit shown in Figure 8, the wideband output in response to a sinusoidal stimulus is a raised cosine.

$$\sin^2 \omega t = (1 - \cos 2\,\omega t)/2$$

Recall that the full-scale output current (when full-scale input voltages of 1 V are applied to both X and Y) is 4 mA. In a 50 Ω system, a sinusoid power of +10 dBm has a peak value of 1 V. Thus, at this drive level, the peak output voltage across the differential 50 Ω load in the absence of the filter capacitors is 400 mV (that is, 4 mA × 50 Ω × 2), whereas the average value of the raised cosine is only 200 mV. The averaging configuration is useful in evaluating the bandwidth of the AD834, because a dc voltage is easier to measure than a wideband differential output. In fact, the squaring mode is an even more critical test than the direct measurement of the bandwidth of either channel taken independently (with a dc input on the nonsignal channel), because the phase relationship between the two channels also affects the average output. For example, a time delay difference of only 250 ps between the X and Y channels results in zero output when the input frequency is 1 GHz, at which frequency the phase angle is 90 degrees and the intrinsic product is now between a sine and cosine function, which has zero average value.

The physical construction of the circuitry around the IC is critical to realizing the bandwidth potential of the device. The input is supplied from an HP 8656A signal generator (100 kHz to 990 MHz) via an SMA connector and terminated by an HP 436A power meter using an HP 8482A sensor head connected via a second SMA connector. Because neither the generator nor the sensor provide a dc path to ground, a lossy 1 µH inductor, L1, formed by a 22-gauge wire passing through a ferrite bead (Fair-Rite Type 2743001112) is included. This provides adequate impedance down to about 30 MHz. The IC socket is mounted on a ground plane with a clear area in the rectangle formed by the pins. This is important because significant transformer action can arise if the pins pass through individual holes in the board; it can cause an oscillation at 1.3 GHz in improperly constructed test jigs. The filter capacitors must be connected directly to the same point on the ground plane via the shortest possible leads. Parallel combinations of large and small capacitors are used to minimize the impedance over the full frequency range. Refer to Figure 4 for mean-square response for the AD834 in a CERDIP package, using the configuration of Figure 8.

To provide a square root response and thus generate the rms value at the output, a second AD834, also connected as a squarer, can be used, as shown in Figure 20. Note that an attenuator is inserted both in the signal input and in the feedback path to the second AD834. This increases the maximum input capability to +15 dBm and improves the response flatness by damping some of the resonances. The overall gain is unity; that is, the output voltage is exactly equal to the rms value of the input signal. The offset potentiometer at the AD834 outputs extends the dynamic range and is adjusted for a dc output of 125.7 mV when a 1 MHz sinusoidal input at −5 dBm is applied.

Additional filtering is provided; the time constants were chosen to allow operation down to frequencies as low as 1 kHz and to provide a critically damped envelope response, which settles typically within 10 ms for a full-scale input (and proportionally slower for smaller inputs). The 5 µF and 0.1 µF capacitors can be scaled down to reduce response time if accurate rms operation at low frequencies is not required. The output op amp must be specified to accept a common-mode input near its supply. Note that the output polarity can be inverted by replacing the NPN transistor with a PNP type.

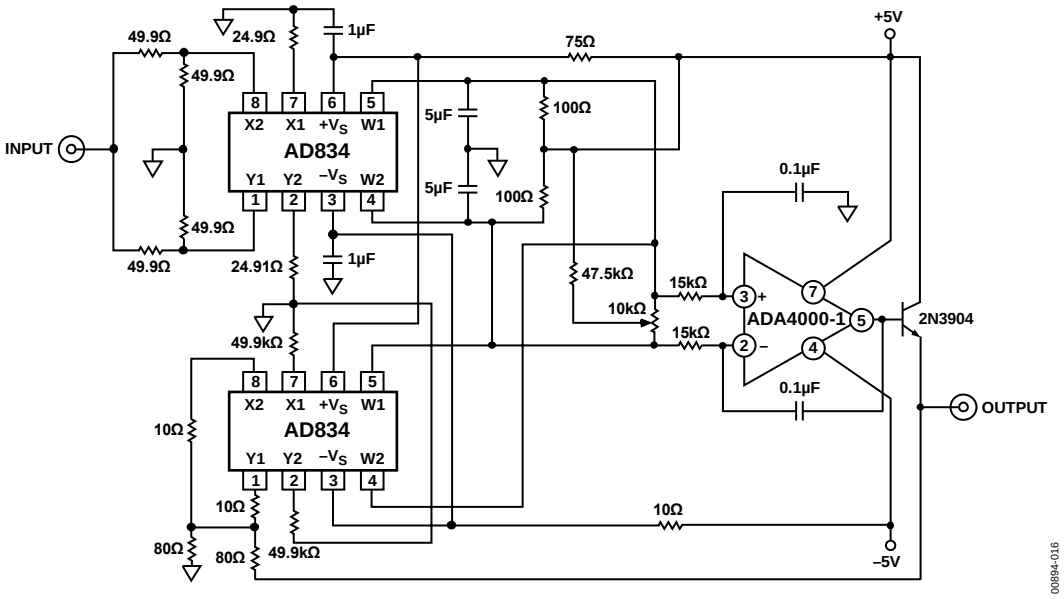


Figure 20. Connections for Wideband RMS Measurement

FREQUENCY DOUBLER

Figure 21 shows another squaring application. In this case, the output filter has been removed and the wideband differential output is converted to a single-sided signal using a balun, which consists of a length of 50 Ω coaxial cable fed through a ferrite core (Fair-Rite Type 2677006301). No attempt is made to reverse terminate the output. Higher load power can be achieved by replacing the 50 Ω load resistors with ferrite bead inductors. The same precautions should be observed with regard to printed circuit board (PCB) layout as recommended in the Power Measurement (Mean-Square and RMS) section. The output spectrum shown in Figure 22 is for an input power of +10 dBm at a frequency of 200 MHz. The second harmonic component at 400 MHz has an output power of −15 dBm. Some feedthrough of the fundamental occurs; it is 15 dB below the main output. A spurious output at 600 MHz is also present, but it is 30 dB below the main output. At an input frequency of 100 MHz, the measured power level at 200 MHz is −16 dBm, while the fundamental feedthrough is reduced to 25 dB below the main output; at an output of 600 MHz the power is −11 dBm and the third harmonic at 900 MHz is 32 dB below the main output.

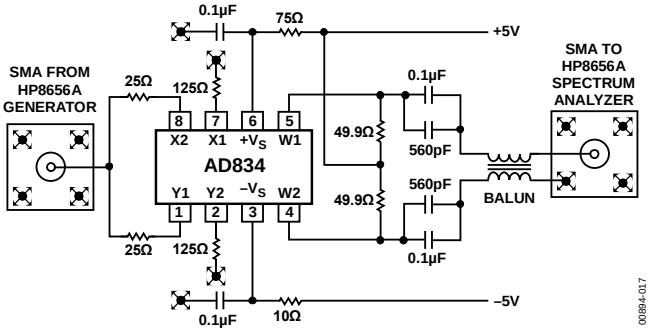


Figure 21. Frequency Doubler Connections

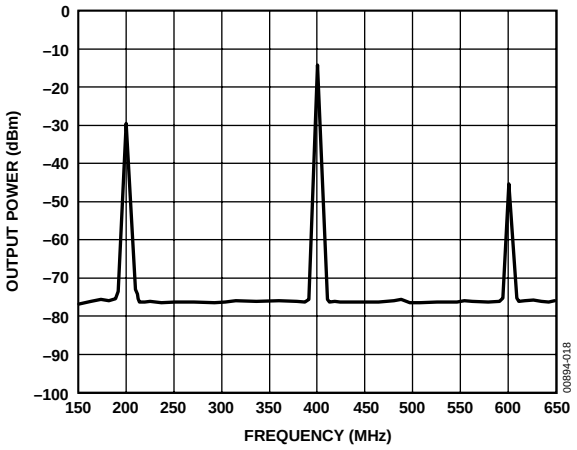


Figure 22. Output Spectrum for Configuration of Figure 21

WIDEBAND THREE-SIGNAL MULTIPLIER/DIVIDER

Two AD834 devices and a wideband op amp can be connected to make a versatile multiplier/divider having the transfer function

$$W = \frac{(X1 - X2)(Y1 - Y2)}{(U1 - U2)} + Z$$

with a denominator range of about 100:1. The denominator input U = U1 − U2 must be positive and in the range 100 mV to 10 V; X, Y, and Z inputs may have either polarity. Figure 23 shows a general configuration that may be simplified to suit a particular application. This circuit accepts full-scale input voltages of 10 V, and delivers a full-scale output voltage of 10 V. The optional offset trim at the output of the AD834 improves the accuracy for small denominator values. It is adjusted by nulling the output voltage when the X and Y inputs are zero and U = 100 mV.

The op amp is internally compensated to be stable without the use of any additional HF compensation. As Input U is reduced, the bandwidth falls because the feedback around the op amp is proportional to Input U. Note that, this circuit was originally characterized using the AD840 op amp; some alternative op amps include the AD818 and the AD8021.

This circuit can be modified in several ways. For example, if the differential input feature is not needed, the unused input can be connected to ground through a single resistor, equal to the parallel sum of the resistors in the attenuator section. The full-scale input levels on X, Y, and U can be adapted to any full-scale voltage down to ±1 V by altering the attenuator ratios. Note, however, that precautions must be taken if the attenuator ratio from the output of A3 back to the second AD834 (A2) is lowered. First, the HF compensation limit of the op amp may be exceeded if the negative feedback factor is too high. Second, if the attenuated output at the AD834 exceeds its clipping level of ±1.3 V, feedback control is lost and the output suddenly jumps to the supply rails. However, with these limitations understood, it is possible to adapt the circuit to smaller full-scale inputs and/or outputs, for use with lower supply voltages.

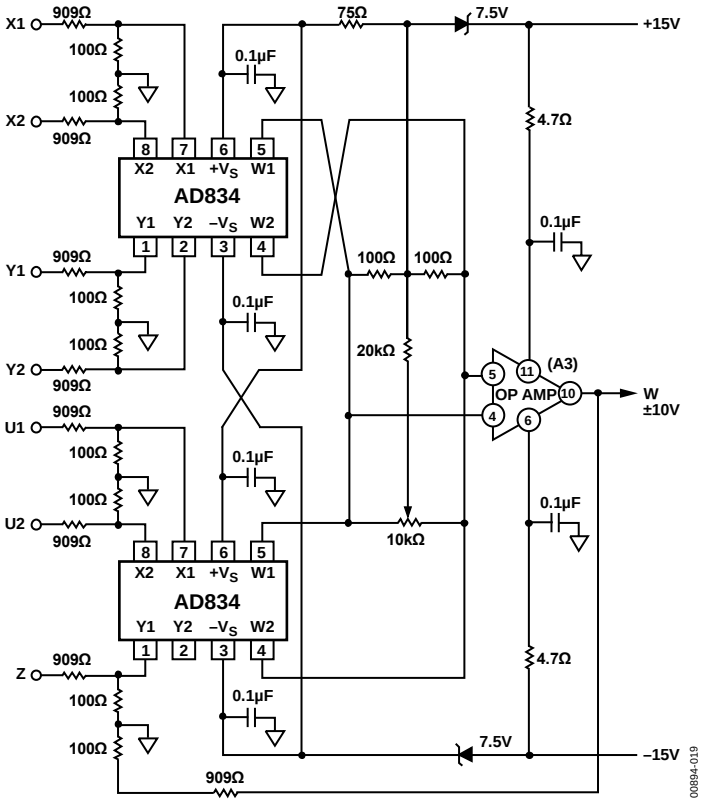
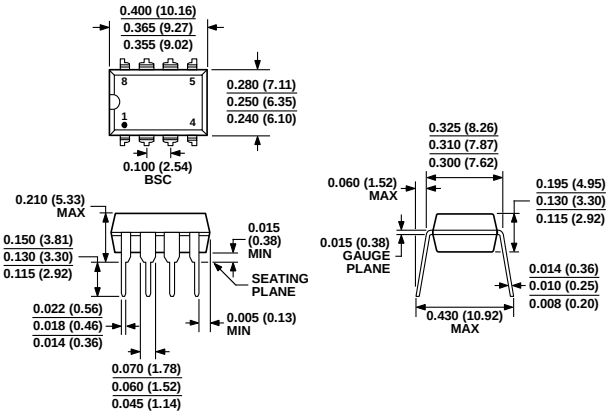


Figure 23. Wideband Three-Signal Multiplier/Divider

OUTLINE DIMENSIONS

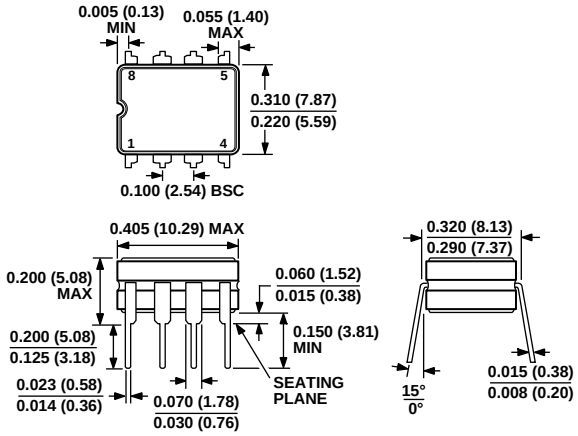


COMPLIANT TO JEDEC STANDARDS MS-001

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

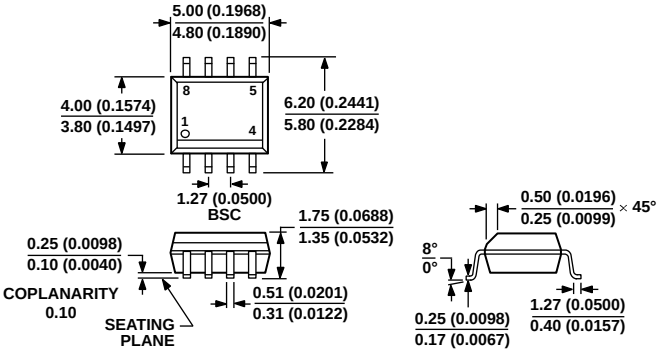
070606-A

Figure 24. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-8)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 25. 8-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-8)
Dimensions shown in inches and (millimeters)



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012407-A

Figure 26. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD834JNZ	0°C to 70°C	8-Lead PDIP	N-8
AD834JRZ	0°C to 70°C	8-Lead SOIC_N	R-8
AD834JRZ-RL	0°C to 70°C	8-Lead SOIC_N	R-8
AD834JRZ-R7	0°C to 70°C	8-Lead SOIC_N	R-8
AD834AR-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8
AD834AR-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8
AD834ARZ	−40°C to +85°C	8-Lead SOIC_N	R-8
AD834ARZ-RL	−40°C to +85°C	8-Lead SOIC_N	R-8
AD834ARZ-R7	−40°C to +85°C	8-Lead SOIC_N	R-8
AD834AQ	−40°C to +85°C	8-Lead CERDIP	Q-8
AD834SQ/883B	−55°C to +125°C	8-Lead CERDIP	Q-8

[1] Z = RoHS Compliant Part.

NOTES