AD827* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-402: Replacing Output Clamping Op Amps with Input Clamping Amps
- AN-417: Fast Rail-to-Rail Operational Amplifiers Ease Design Constraints in Low Voltage High Speed Systems
- AN-581: Biasing and Decoupling Op Amps in Single Supply Applications

Data Sheet

- AD827: High Speed, Low Power Dual Op Amp Data Sheet
- AD827: Military Data Sheet

TOOLS AND SIMULATIONS

- Analog Filter Wizard
- Analog Photodiode Wizard
- Power Dissipation vs Die Temp
- VRMS/dBm/dBu/dBV calculators
- AD827 SPICE Macro Model

REFERENCE MATERIALS

Product Selection Guide

- High Speed Amplifiers Selection Table

Tutorials

- MT-032: Ideal Voltage Feedback (VFB) Op Amp
- MT-047: Op Amp Noise
- MT-048: Op Amp Noise Relationships: 1/f Noise, RMS Noise, and Equivalent Noise Bandwidth
- MT-049: Op Amp Total Output Noise Calculations for Single-Pole System
- MT-050: Op Amp Total Output Noise Calculations for Second-Order System
- MT-052: Op Amp Noise Figure: Don't Be Misled
- MT-053: Op Amp Distortion: HD, THD, THD + N, IMD, SFDR, MTPR
- MT-056: High Speed Voltage Feedback Op Amps
- MT-058: Effects of Feedback Capacitance on VFB and CFB Op Amps
- MT-060: Choosing Between Voltage Feedback and Current Feedback Op Amps

DESIGN RESOURCES

- AD827 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD827 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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AD827—SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted.)

Model	Conditions	V_S	AD827J Min	AD827J Typ	AD827J Max	AD827A/S Min	AD827A/S Typ	AD827A/S Max	Unit
DC PERFORMANCE									
Input Offset Voltage[1]		±5 V		0.5	2		0.3	2	mV
	T_{MIN} to T_{MAX}				3.5			4	mV
		±15 V			4			4	mV
	T_{MIN} to T_{MAX}				6			6	mV
Offset Voltage Drift		±5 V to ±15 V		15			15		µV/°C
Input Bias Current		±5 V to ±15 V		3.3	7		3.3	7	µA
	T_{MIN} to T_{MAX}				8.2			9.5	µA
Input Offset Current		±5 V to ±15 V		50	300		50	300	nA
	T_{MIN} to T_{MAX}				400			400	nA
Offset Current Drift		±5 V to ±15 V		0.5			0.5		nA/°C
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	±5 V	78	95		80	95		dB
	V_{CM} = ±12 V	±15 V	78	95		80	95		dB
	T_{MIN} to T_{MAX}	±5 V to ±15 V	75			75			dB
Power Supply Rejection Ratio		±5 V to ±15 V	75	86		75	86		dB
	T_{MIN} to T_{MAX}		72			72			dB
Open-Loop Gain									
	V_O = ±2.5 V	±5 V							
	R_{LOAD} = 500 Ω		2	3.5		2	3.5		V/mV
	T_{MIN} to T_{MAX}		1			1			V/mV
	R_{LOAD} = 150 Ω			1.6			1.6		V/mV
	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		3	5.5		3	5.5		V/mV
	T_{MIN} to T_{MAX}		1.5			1.5			V/mV
MATCHING CHARACTERISTICS									
Input Offset Voltage		±5 V		0.4			0.2		mV
Crosstalk	f = 5 MHz	±5 V		85			85		dB
DYNAMIC PERFORMANCE									
Unity-Gain Bandwidth		±5 V		35			35		MHz
		±15 V		50			50		MHz
Full Power Bandwidth[2]	V_O = 5 V p-p,								
	R_{LOAD} = 500 Ω	±5 V		12.7			12.7		MHz
	V_O = 20 V p-p,								
	R_{LOAD} = 1 kΩ	±15 V		4.7			4.7		MHz
Slew Rate[3]	R_{LOAD} = 500 Ω	±5 V		200			200		V/µs
	R_{LOAD} = 1 kΩ	±15 V		300			300		V/µs
Settling Time to 0.1%	A_V = –1								
	–2.5 V to +2.5 V	±5 V		65			65		ns
	–5 V to +5 V	±15 V		120			120		ns
Phase Margin	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD} = 1 kΩ			50			50		Degrees
Differential Gain Error	f = 4.4 MHz	±15 V		0.04			0.04		%
Differential Phase Error	f = 4.4 MHz	±15 V		0.19			0.19		Degrees
Input Voltage Noise	f = 10 kHz	±15 V		15			15		$nV/\sqrt{Hz}$
Input Current Noise	f = 10 kHz	±15 V		1.5			1.5		$pA/\sqrt{Hz}$
Input Common-Mode									
Voltage Range		±5 V		+4.3			+4.3		V
				–3.4			–3.4		V
		±15 V		+14.3			+14.3		V
				–13.4			–13.4		V
Output Voltage Swing	R_{LOAD} = 500 Ω	±5 V	3.0	3.6		3.0	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	2.5	3.0		2.5	3.0		±V
	R_{LOAD} = 1 kΩ	±15 V	12	13.3		12	13.3		±V
	R_{LOAD} = 500 Ω	±15 V	10	12.2		10	12.2		±V
Short-Circuit Current Limit		±5 V to ±15 V		32			32		mA
INPUT CHARACTERISTICS									
Input Resistance				300			300		kΩ
Input Capacitance				1.5			1.5		pF

Model	Conditions	V_S	AD827J Min	AD827J Typ	AD827J Max	AD827A/S Min	AD827A/S Typ	AD827A/S Max	Unit
OUTPUT RESISTANCE	Open Loop			15				15	Ω
POWER SUPPLY									
Operating Range			±4.5		±18	±4.5		±18	V
Quiescent Current		±5 V		10	13		10	13	mA
	T_{MIN} to T_{MAX}				16			16.5/17.5	mA
		±15 V		10.5	13.5		10.5	13.5	mA
	T_{MIN} to T_{MAX}				16.5			17/18	mA
TRANSISTOR COUNT				92			92		

NOTES
[1] Offset voltage for the AD827 is guaranteed after power is applied and the device is fully warmed up. All other specifications are measured using high speed test equipment, approximately 1 second after power is applied.
[2] Full Power Bandwidth = Slew Rate/2 π V_{PEAK}.
[3] Gain = +1, rising edge.
All min and max specifications are guaranteed.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) Package (Derate at 10 mW/°C) . . . . . 1.5 W
Cerdip (Q) Package (Derate at 8.7 mW/°C) . . . . . 1.3 W
Small Outline (R) Package (Derate at 10 mW/°C) . . . 1.5 W
LCC (E) Package (Derate at 6.7 mW/°C) . . . . . 1.0 W
Input Common-Mode Voltage . . . . . ±V_S
Differential Input Voltage . . . . . 6 V
Output Short Circuit Duration[3] . . . . . Indefinite
Storage Temperature Range (N, R) . . . . . –65°C to +125°C
Storage Temperature Range (Q) . . . . . –65°C to +150°C
Operating Temperature Range
AD827J . . . . . 0°C to 70°C
AD827A . . . . . –40°C to +85°C
AD827S . . . . . –55°C to +125°C
Lead Temperature Range
(Soldering to 60 sec) . . . . . 300°C

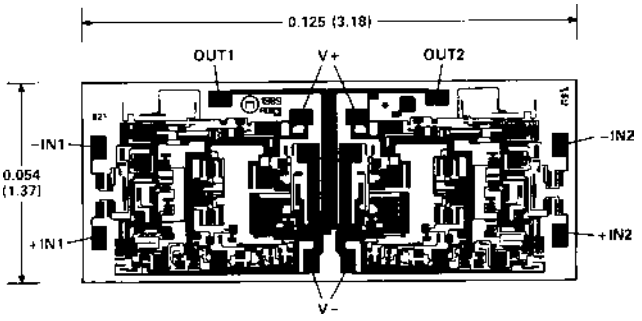
NOTES
[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.
[2] Maximum internal power dissipation is specified so that T_J does not exceed 175°C at an ambient temperature of 25°C.
Thermal Characteristics:
MiniDIP: θ_{JA} = 100°C/W; θ_{JC} = 33°C/ W
Cerdip: θ_{JA} = 110°C/W; θ_{JC} = 30°C/W
16-Lead Small Outline Package: θ_{JA} = 100°C/W
20-Lead LCC: θ_{JA} = 150°C/W; θ_{JC} = 35°C/W
[3] Indefinite short circuit duration is only permissible as long as the absolute maximum power rating is not exceeded.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD827JN	0°C to +70°C	8-Lead Plastic DIP	N-8
AD827JR	0°C to +70°C	16-Lead Plastic SO	R-16
AD827AQ	–40°C to +85°C	8-Lead Cerdip	Q-8
AD827SQ	–55°C to +125°C	8-Lead Cerdip	Q-8
AD827SQ/883B	–55°C to +125°C	8-Lead Cerdip	Q-8
5962-9211701MPA	–55°C to +125°C	8-Lead Cerdip	Q-8
AD827SE/883B	–55°C to +125°C	20-Lead LCC	E-20A
5962-9211701M2A	–55°C to +125°C	20-Lead LCC	E-20A
AD827JR-REEL	0°C to +70°C	Tape & Reel	
AD827JChips	0°C to +70°C	Die	
AD827SChips	–55°C to +125°C	Die	

METALLIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).
Substrate is connected to V+.



AD827–Typical Performance Characteristics (@ +25°C & ±15 V, unless otherwise noted)

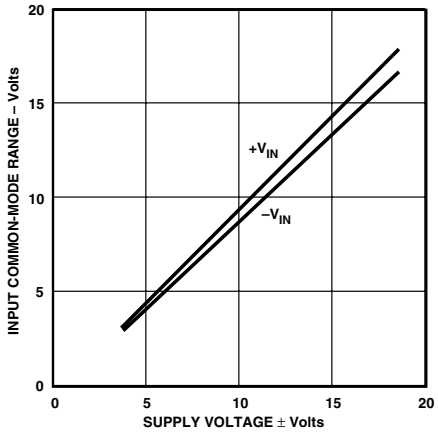


Figure1. InputCommon-Mode Range vs. Supply Voltage

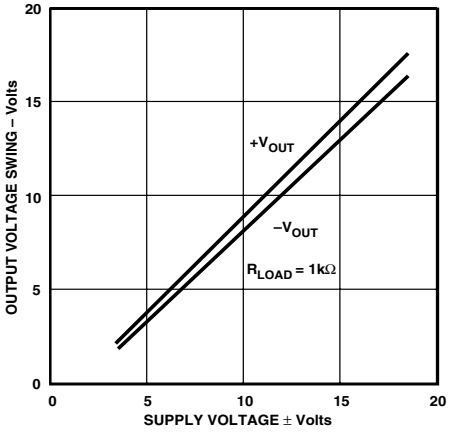


Figure 2. Output Voltage Swing vs. Supply Voltage

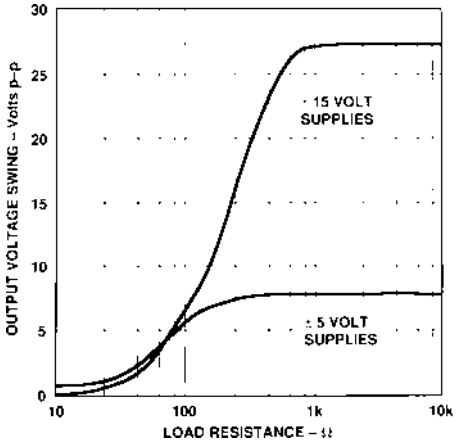


Figure 3. Output Voltage Swing vs. Load Resistance

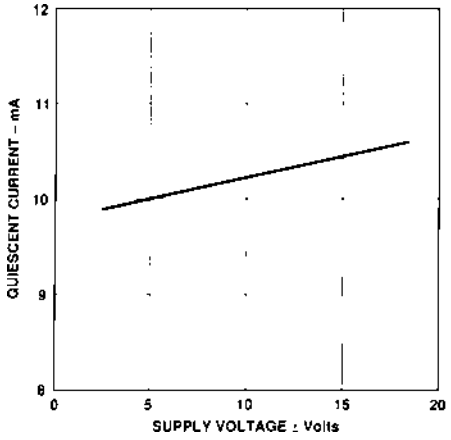


Figure 4. Quiescent Current vs. Supply Voltage

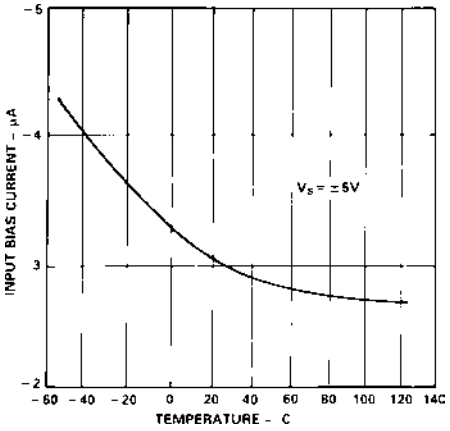


Figure 5. Input Bias Current vs. Temperature

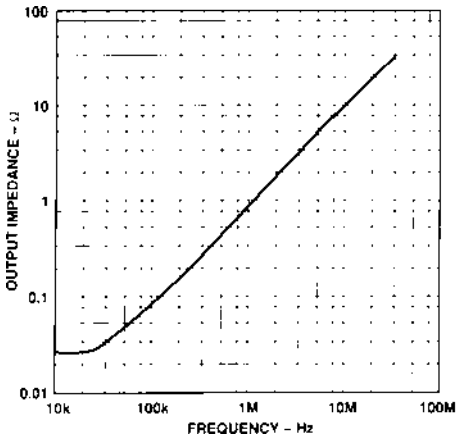


Figure 6. Closed-Loop Output Impedance vs. Frequency, Gain = +1

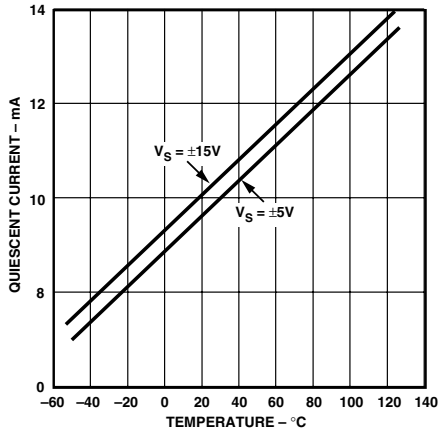


Figure 7. Quiescent Current vs. Temperature

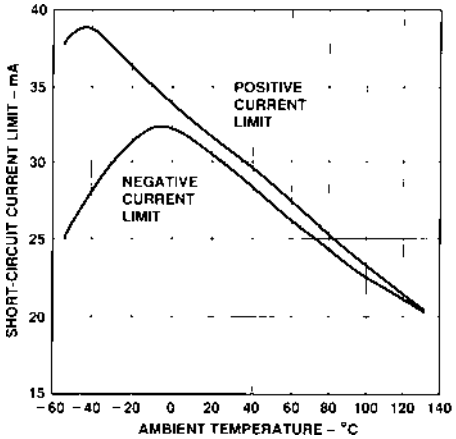


Figure 8. Short-Circuit Current Limit vs. Temperature

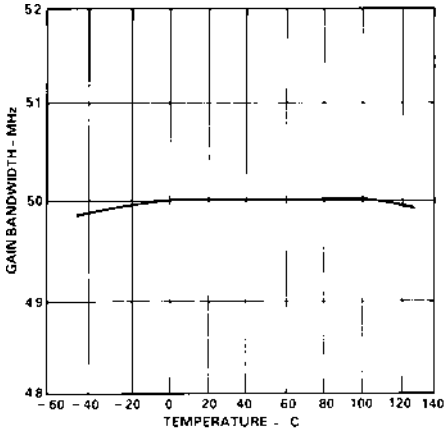


Figure 9. Gain Bandwidth vs. Temperature

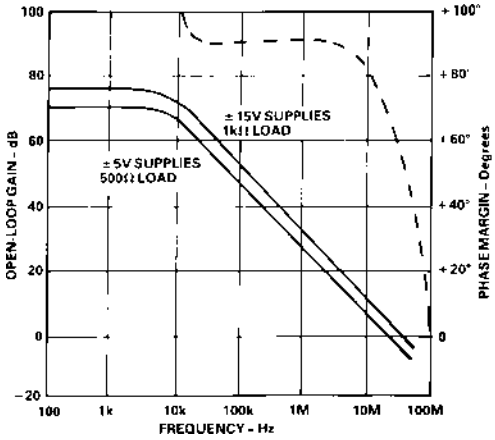


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

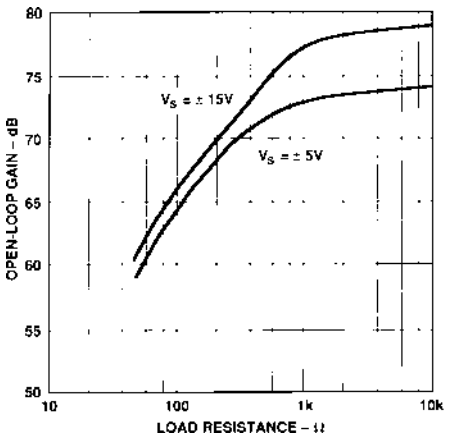


Figure 11. Open-Loop Gain vs. Load Resistance

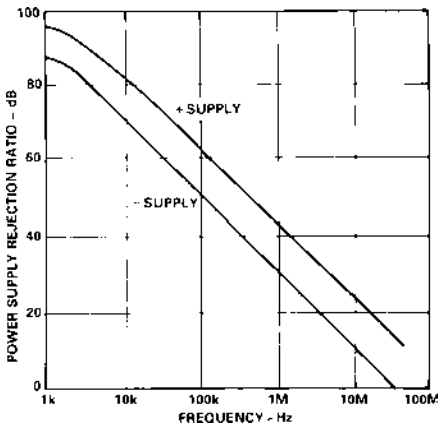


Figure 12. Power Supply Rejection Ratio vs. Frequency

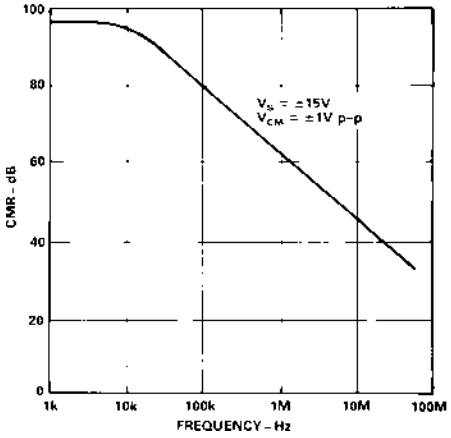


Figure 13. Common-Mode Rejection Ratio vs. Frequency

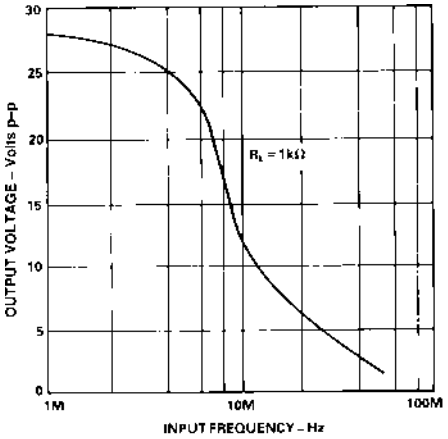


Figure 14. Large Signal Frequency Response

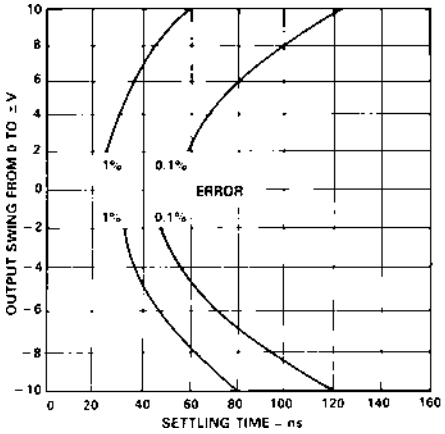


Figure 15. Output Swing and Error vs. Settling Time

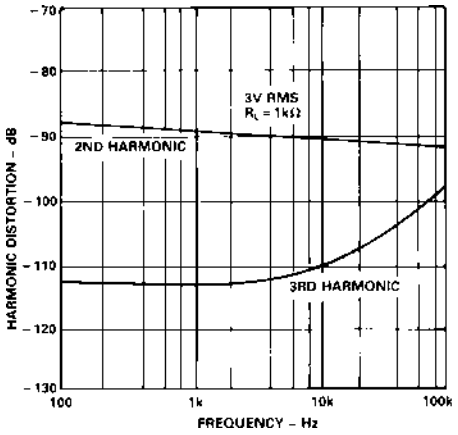


Figure 16. Harmonic Distortion vs. Frequency

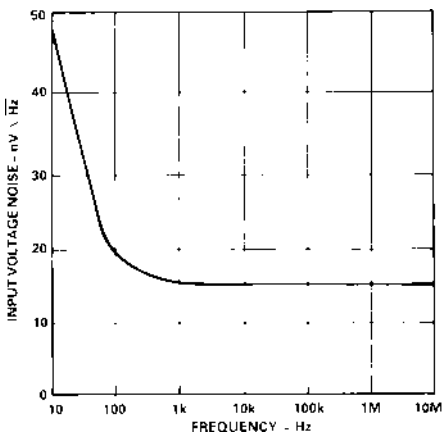


Figure 17. Input Voltage Noise Spectral Density

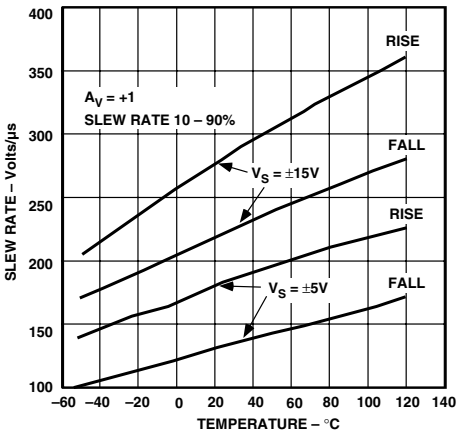


Figure 18. Slew Rate vs. Temperature

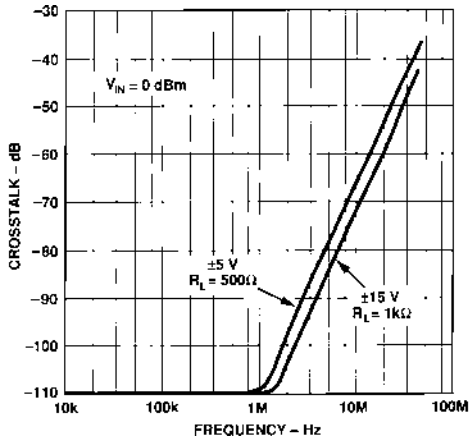


Figure 19. Crosstalk vs. Frequency

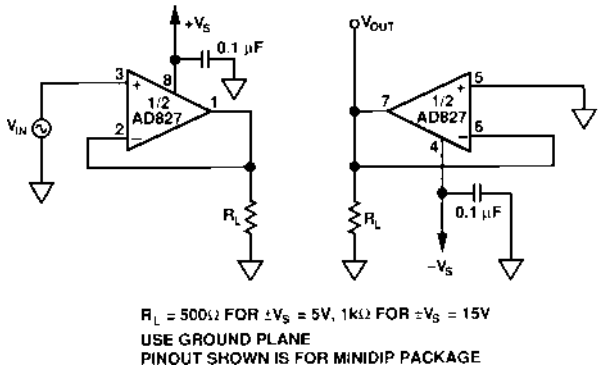


Figure 20. Crosstalk Test Circuit

INPUT PROTECTION PRECAUTIONS

An input resistor (resistor R_{IN} of Figure 21a) is recommended in circuits where the input common-mode voltage to the AD827 may exceed (on a transient basis) the positive supply voltage. This resistor provides protection for the input transistors by limiting the maximum current that can be forced into their bases.

For high performance circuits, it is recommended that a second resistor (R_B in Figures 21a and 22a) be used to reduce bias-current errors by matching the impedance at each input. This resistor reduces the error caused by offset voltages by more than an order of magnitude.

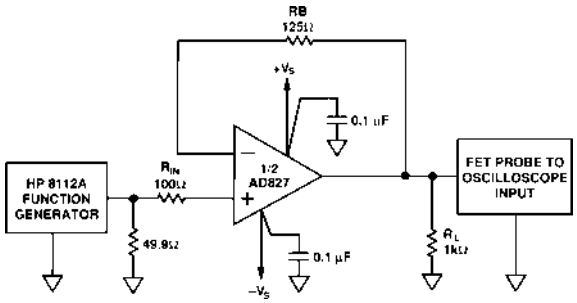


Figure 21a. Follower Connection

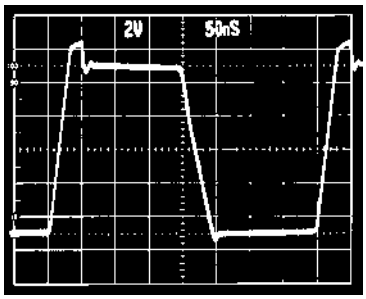


Figure 21b. Follower Large Signal Pulse Response

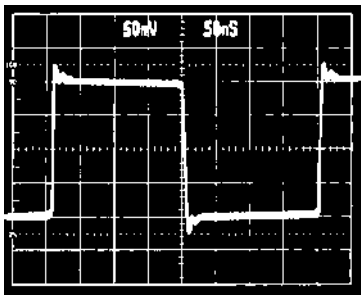


Figure 21c. Follower Small Signal Pulse Response

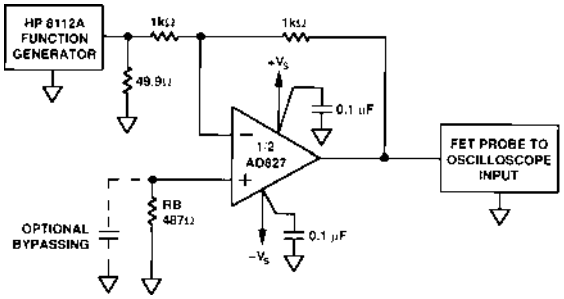


Figure 22a. Inverter Connection

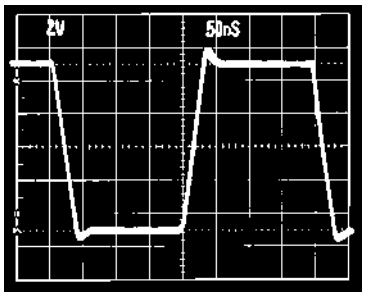


Figure 22b. Inverter Large Signal Pulse Response

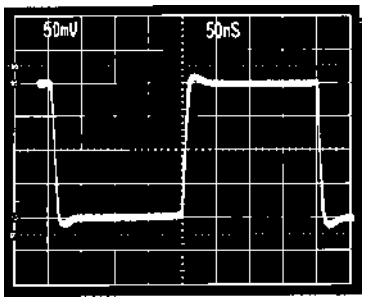


Figure 22c. Inverter Small Signal Pulse Response

VIDEO LINE DRIVER

The AD827 functions very well as a low cost, high speed line driver for either terminated or unterminated cables. Figure 23 shows the AD827 driving a doubly terminated cable in a follower configuration.

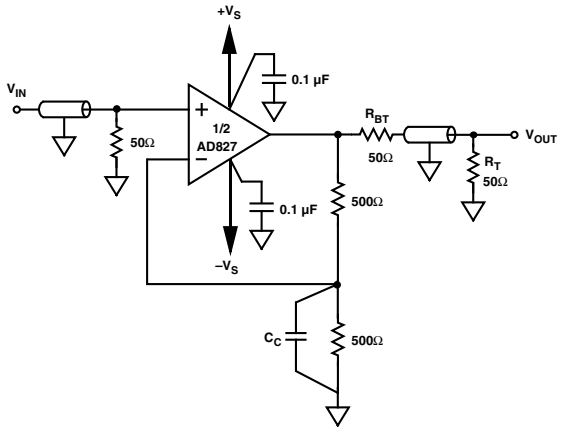


Figure 23. A Video Line Driver

The termination resistor, R_T, (when equal to the cable's characteristic impedance) minimizes reflections from the far end of the cable. While operating from ±5 V supplies, the AD827 maintains a typical slew rate of 200 V/µs, which means it can drive a ±1 V, 30 MHz signal into a terminated cable.

Table I. Video Line Driver Performance Summary

V_{IN}*	V_{SUPPLY}	C_C	–3 dB B_W	Over-shoot
0 dB or ±500 mV Step	±15	20 pF	23 MHz	4%
0 dB or ±500 mV Step	±15	15 pF	21 MHz	0%
0 dB or ±500 mV Step	±15	0 pF	13 MHz	0%
0 dB or ±500 mV Step	±5	20 pF	18 MHz	2%
0 dB or ±500 mV Step	±5	15 pF	16 MHz	0%
0 dB or ±500 mV Step	±5	0 pF	11 MHz	0%

*–3 dB bandwidth numbers are for the 0 dBm signal input. Overshoot numbers are the percent overshoot of the 1 V step input.

A back-termination resistor (R_{BT}, also equal to the characteristic impedance of the cable) may be placed between the AD827 output and the cable input, in order to damp any reflected signals caused by a mismatch between R_T and the cable's characteristic impedance. This will result in a flatter frequency response, although this requires that the op amp supply ±2 V to the output in order to achieve a ±1 V swing at resistor R_T.

A HIGH SPEED THREE OP AMP INSTRUMENTATION AMPLIFIER CIRCUIT

The instrumentation amplifier circuit shown in Figure 24 can provide a range of gains. Table II details performance.

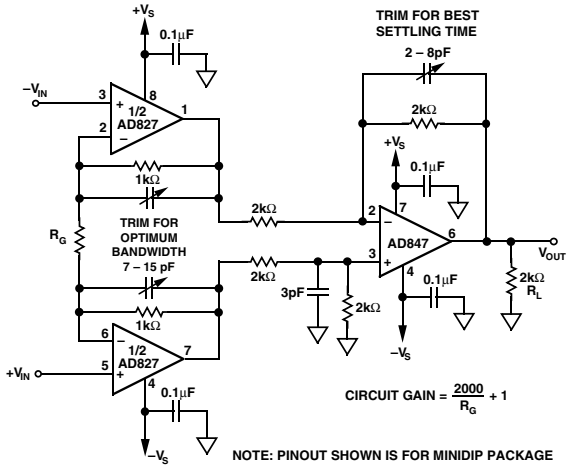


Figure 24. A High Bandwidth Three Op Amp Instrumentation Amplifier

Table II. Performance Specifications for the Three Op Amp Instrumentation Amplifier

Gain	R_G	Small Signal Bandwidth @ 1 V p-p Output
1	Open	16.1 MHz
2	2 k	14.7 MHz
10	226 Ω	4.9 MHz
100	20 Ω	660 kHz

A TWO-CHIP VOLTAGE-CONTROLLED AMPLIFIER (VCA) WITH EXPONENTIAL RESPONSE

Voltage-controlled amplifiers are often used as building blocks in automatic gain control systems. Figure 25 shows a two-chip VCA built using the AD827 and the AD539, a dual, current-output multiplier. As configured, the circuit has its two

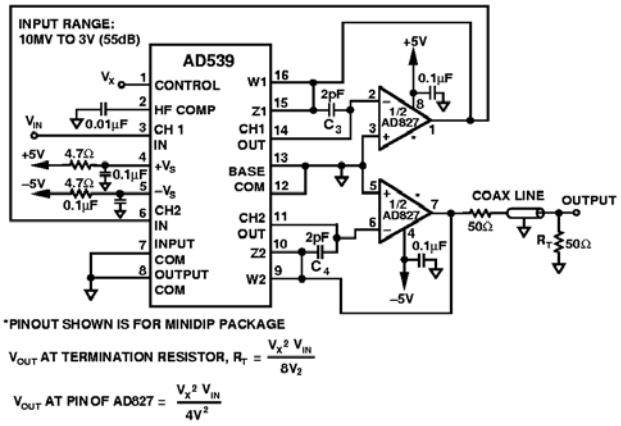


Figure 25. A Wide Range Voltage-Controlled Amplifier Circuit

multipliers connected in series. They could also be placed in parallel with an increase in bandwidth and a reduction in gain. The gain of the circuit is controlled by V_X, which can range from 0 to 3 V dc. Measurements show that this circuit easily supplies 2 V p-p into a 100 Ω load while operating from ±5 V supplies. The overall bandwidth of the circuit is approximately 7 MHz with 0.5 dB of peaking.

Each half of the AD827 serves as an I/V converter and converts the output current of one of the two multipliers in the AD539 into an output voltage. Each of the AD539's two multipliers contains two internal 6 kΩ feedback resistors; one is connected between the CH1 output and Z1, the other between the CH1 output and W1. Likewise, in the CH2 multiplier, one of the feedback resistors is connected between CH2 and Z2 and the other is connected between CH2 and Z2. In Figure 25, Z1 and W1 are tied together, as are Z2 and W2, providing a 3 kΩ feedback resistor for the op amp. The 2 pF capacitors connected between the AD539's W1 and CH1 and W2 and CH2 pins are in parallel with the feedback resistors and thus reduce peaking in the VCA's frequency response. Increasing the values of C3 and C4 can further reduce the peaking at the expense of reduced bandwidth. The 1.25 mA full-scale output current of the AD539 and the 3 kΩ feedback resistor set the full-scale output voltage of each multiplier at 3.25 V p-p.

Current limiting in the AD827 (typically 30 mA) limits the output voltage in this application to about 3 V p-p across a 100 Ω load. Driving a 50 Ω reverse-terminated load divides this value by two, limiting the maximum signal delivered to a 50 Ω load to about 1.5 V p-p, which suffices for video signal levels. The dynamic range of this circuit is approximately 55 dB and is primarily limited by feedthrough at low input levels and by the maximum output voltage at high levels.

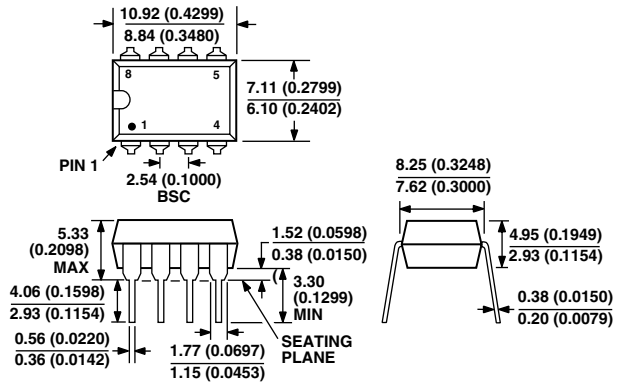
Guidelines for Grounding and Bypassing

When designing practical high frequency circuits using the AD827, some special precautions are in order. Both short interconnection leads and a large ground plane are needed whenever possible to provide low resistance, low inductance circuit paths. One should remember to minimize the effects of capacitive coupling between circuits. Furthermore, IC sockets should be avoided. Feedback resistors should be of a low enough value that the time constant formed with stray circuit capacitances at the amplifier summing junction will not limit circuit performance. As a rule of thumb, use feedback resistor values that are less than 5 kΩ. If a larger resistor value is necessary, a small (<10 pF) feedback capacitor in parallel with the feedback resistor may be used. The use of 0.1 µF ceramic disc capacitors is recommended for bypassing the op amp's power supply leads.

OUTLINE DIMENSIONS

8-Lead Plastic Dual-in-Line Package [PDIP]
(N-8)

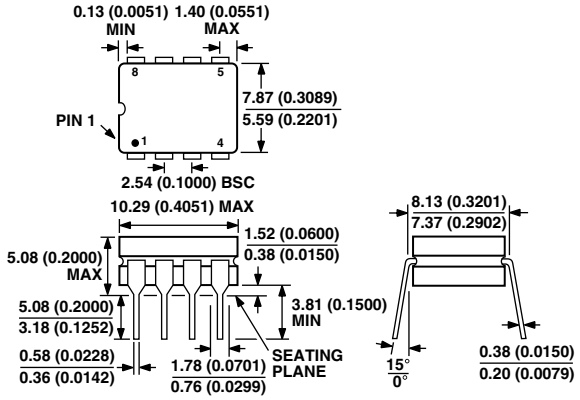
Dimensions shown in millimeters and (inches)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Ceramic DIP-Glass Hermetic Seal Package [CERDIP]
(Q-8)

Dimensions shown in millimeters and (inches)



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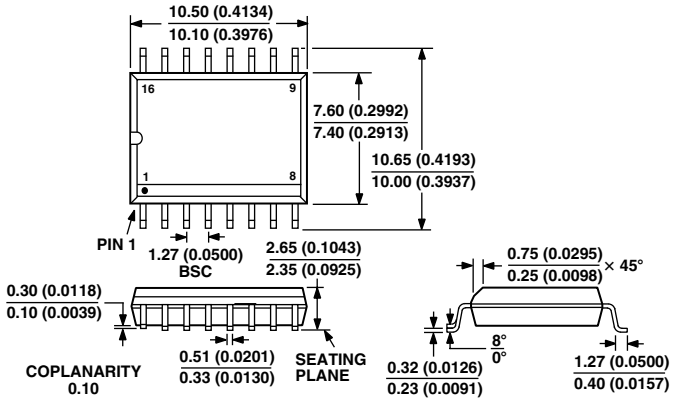
16-Lead Standard Small Outline Package [SOIC]
Wide Body
(R-16)

Dimensions shown in millimeters and (inches)



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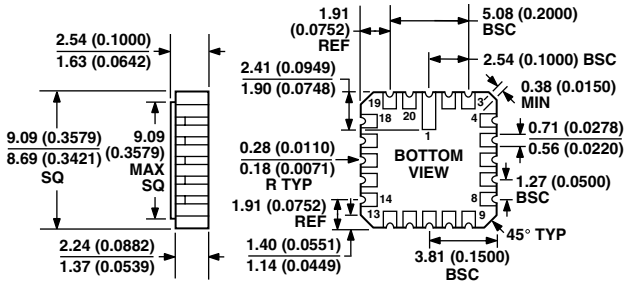
COMPLIANT TO JEDEC STANDARDS MS-013AA

20-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-20A)

Dimensions shown in millimeters and (inches)



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Revision History

Location	Page
8/02—Data Sheet changed from REV. B to REV. C.	
Updated Outline Dimensions	9

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