AD8022* Product Page Quick Links

Last Content Update: 11/01/2016

Comparable Parts

View a parametric search of comparable parts

Evaluation Kits

- ADSP-SC584 Evaluation Hardware for the ADSP-SC58x/ ADSP-2158x SHARC Family (349-ball CSPBGA)
- ADSP-SC589 Evaluation Hardware for the ADSP-SC58x/ ADSP-2158x SHARC Family (529-ball CSPBGA)
- Universal Evaluation Board for Dual High Speed Operational Amplifiers

Documentation

Application Notes

- AN-356: User's Guide to Applying and Measuring Operational Amplifier Specifications
- AN-402: Replacing Output Clamping Op Amps with Input Clamping Amps
- AN-417: Fast Rail-to-Rail Operational Amplifiers Ease Design Constraints in Low Voltage High Speed Systems
- AN-581: Biasing and Decoupling Op Amps in Single Supply Applications
- AN-649: Using the Analog Devices Active Filter Design Tool
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design

Data Sheet

- AD8022: Dual High Speed Low Noise Op Amp Data Sheet

User Guides

- UG-128: Universal Evaluation Board for Dual High Speed Op Amps in SOIC Packages
- UG-886: Universal Evaluation Board for Dual High Speed Op Amps Offered in 8-Lead MSOP

Tools and Simulations

- Analog Filter Wizard
- Analog Photodiode Wizard
- Power Dissipation vs Die Temp
- VRMS/dBm/dBu/dBV calculators
- AD8022 SPICE Macro-Model

Reference Designs

- CN0039
- CN0048

Reference Materials

Product Selection Guide

- High Speed Amplifiers Selection Table
- SAR ADC & Driver Quick-Match Guide

Technical Articles

- Maximize Performance When Driving Differential ADCs

Tutorials

- MT-032: Ideal Voltage Feedback (VFB) Op Amp
- MT-033: Voltage Feedback Op Amp Gain and Bandwidth
- MT-048: Op Amp Noise Relationships: 1/f Noise, RMS Noise, and Equivalent Noise Bandwidth
- MT-049: Op Amp Total Output Noise Calculations for Single-Pole System
- MT-050: Op Amp Total Output Noise Calculations for Second-Order System
- MT-052: Op Amp Noise Figure: Don't Be Misled
- MT-053: Op Amp Distortion: HD, THD, THD + N, IMD, SFDR, MTPR
- MT-056: High Speed Voltage Feedback Op Amps
- MT-058: Effects of Feedback Capacitance on VFB and CFB Op Amps
- MT-059: Compensating for the Effects of Input Capacitance on VFB and CFB Op Amps Used in Current-to-Voltage Converters
- MT-060: Choosing Between Voltage Feedback and Current Feedback Op Amps

Design Resources

- AD8022 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

View all AD8022 EngineerZone Discussions

Sample and Buy

Visit the product page to see pricing options

Technical Support

Submit a technical question or find your regional support number

* This page was dynamically generated by Analog Devices, Inc. and inserted into this data sheet. Note: Dynamic changes to the content on this page does not constitute a change to the revision number of the product data sheet. This content may be frequently modified.

TABLE OF CONTENTS

REVISION HISTORY

8/11—Rev. B to Rev. C

Changes to Figure 40 14
Updated Outline Dimensions 16
Changes to Ordering Guide 16

5/05—Rev. A to Rev. B

Changes to Format ..... Universal
Deleted Evaluation Boards Section 14
Deleted Generating DMT Section 14
Changes to Ordering Guide 16
Updated Outline Dimensions 16

9/02—Rev. 0 to Rev. A

Changes to Features 1
Changes to Applications 1
Changes to Product Description 1
Changes to Functional Block Diagram 1
Changes to Figure 1 1
Changes to Specifications Table 2
Edits to TPCs 1, 2, 3, 6 5
New TPCs 7, 8 6
Edits to TPCs 16, 17, 18 7
Edits to TPC 19 8
Edits to TPC 28 9
Edits to Figure 3 11
Edits to Figure 6 14
Updated Outline Dimensions 16

SPECIFICATIONS

At 25°C, V_S = ±12 V, R_L = 500 Ω, G = +1, T_{MIN} = −40°C, T_{MAX} = +85°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	V_{OUT} = 50 mV p-p	110	130		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 50 mV p-p		25		MHz
Large Signal Bandwidth[1]	V_{OUT} = 4 V p-p		4		MHz
Slew Rate	V_{OUT} = 2 V p-p, G = +2	40	50		V/µs
Rise and Fall Time	V_{OUT} = 2 V p-p, G = +2		30		ns
Settling Time 0.1%	V_{OUT} = 2 V p-p		62		ns
Overdrive Recovery Time	V_{OUT} = 150% of max output voltage, G = +2		200		ns
NOISE/DISTORTION PERFORMANCE					
Distortion	V_{OUT} = 2 V p-p				
Second Harmonic	f_C = 1 MHz		−95		dBc
Third Harmonic	f_C = 1 MHz		−100		dBc
Multitone Input Power Ratio[2]	G = +7 differential				
	26 kHz to 132 kHz		−67.2		dBc
	144 kHz to 1.1 MHz		−66		dBc
Voltage Noise (RTI)	f = 100 kHz		2.5		nV/√Hz
Input Current Noise	f = 100 kHz		1.2		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			−1.5	±6	mV
	T_{MIN} to T_{MAX}			±7.25	mV
Input Offset Current			±120		nA
Input Bias Current			2.5	5.0	µA
	T_{MIN} to T_{MAX}			±7.5	µA
Open-Loop Gain			72		dB
INPUT CHARACTERISTICS					
Input Resistance (Differential)			20		kΩ
Input Capacitance			0.7		pF
Input Common-Mode Voltage Range			−11.25 to +11.75		V
Common-Mode Rejection Ratio	V_{CM} = ±3 V		98		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 500 Ω		±10.1		V
	R_L = 2 kΩ		±10.6		V
Linear Output Current	G = +1, R_L = 150 Ω, dc error = 1%		±55		mA
Short-Circuit Output Current			100		mA
Capacitive Load Drive	R_S = 0 Ω, <3 dB of peaking		75		pF
POWER SUPPLY					
Operating Range		+4.5		±13.0	V
Quiescent Current			4.0	5.5	mA/Amp
	T_{MIN} to T_{MAX}			6.1	mA/Amp
Power Supply Rejection Ratio	V_S = ±5V to ±12 V		80		dB
OPERATING TEMPERATURE RANGE		−40		+85	°C

[1] FPBW = Slew Rate/(2π V_{PEAK}).
[2] Multitone testing performed with 800 mV rms across a 500 Ω load at Point A and Point B on the circuit of Figure 23.

At 25°C, V_S = ±2.5 V, R_L = 500 Ω, G = +1, T_{MIN} = −40°C, T_{MAX} = +85°C, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	V_{OUT} = 50 mV p-p	100	120		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 50 mV p-p		22		MHz
Large Signal Bandwidth[1]	V_{OUT} = 3 V p-p		4		MHz
Slew Rate	V_{OUT} = 2 V p-p, G = +2	30	42		V/µs
Rise and Fall Time	V_{OUT} = 2 V p-p, G = +2		40		ns
Settling Time 0.1%	V_{OUT} = 2 V p-p		75		ns
Overdrive Recovery Time	V_{OUT} = 150% of max output voltage, G = +2		225		ns
NOISE/DISTORTION PERFORMANCE					
Distortion	V_{OUT} = 2 V p-p				
Second Harmonic	f_C = 1 MHz		−77.5		dBc
Third Harmonic	f_C = 1 MHz		−94		dBc
Multitone Input Power Ratio[2]	G = +7 differential, V_S = ±6 V				
	26 kHz to 132 kHz		−69		dBc
	144 kHz to 1.1 MHz		−66.7		dBc
Voltage Noise (RTI)	f = 100 kHz		2.3		nV/√Hz
Input Current Noise	f = 100 kHz		1		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			−0.8	±5.0	mV
	T_{MIN} to T_{MAX}			±6.25	mV
Input Offset Current			±65		nA
Input Bias Current			2.0	5.0	µA
	T_{MIN} to T_{MAX}			7.5	µA
Open-Loop Gain			64		dB
INPUT CHARACTERISTICS					
Input Resistance (Differential)			20		kΩ
Input Capacitance			0.7		pF
Input Common-Mode Voltage Range			−1.83 to +2.0		V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V, V_S = ±5.0 V		98		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 500 Ω		−1.38 to +1.48		V
Linear Output Current	G = +1, R_L = 100 Ω, dc error = 1%		±32		mA
Short-Circuit Output Current			80		mA
Capacitive Load Drive	R_S = 0 Ω, <3 dB of peaking		75		pF
POWER SUPPLY					
Operating Range		+4.5		±13.0	V
Quiescent Current			3.5	4.25	mA/Amp
	T_{MIN} to T_{MAX}			4.4	mA/Amp
Power Supply Rejection Ratio	ΔV_S = ±1 V		86		dB
OPERATING TEMPERATURE RANGE		−40		+85	°C

[1] FPBW = Slew Rate/(2 π V_{PEAK}).
[2] Multitone testing performed with 800 mV rms across a 500 Ω load at Point A and Point B on the circuit of Figure 23.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage ($+V_S$ to $-V_S$)	26.4 V
Internal Power Dissipation[1]	
8-Lead SOIC (R)	1.6 W
8-Lead MSOP (RM)	1.2 W
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage	±0.8 V
Output Short-Circuit Duration	Observe Power Derating Curves
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range (A Grade)	−40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C

[1] Specification is for the device in free air:
8-Lead SOIC: θ_{JA} = 160°C/W.
8-Lead MSOP: θ_{JA} = 200°C/W.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8022 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8022 is internally short-circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

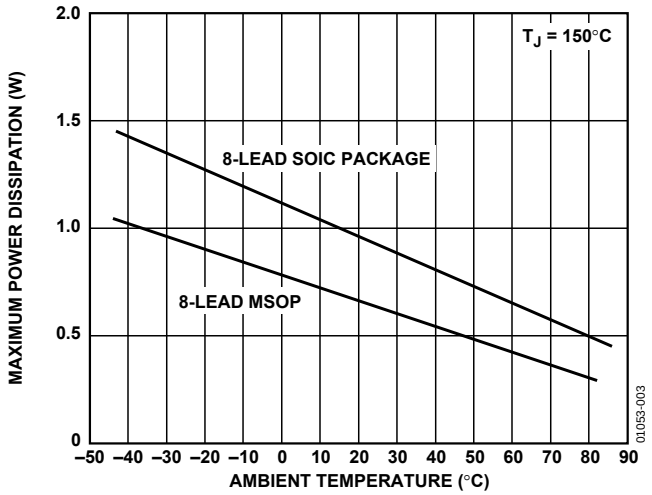

Figure 3. Maximum Power Dissipation vs. Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

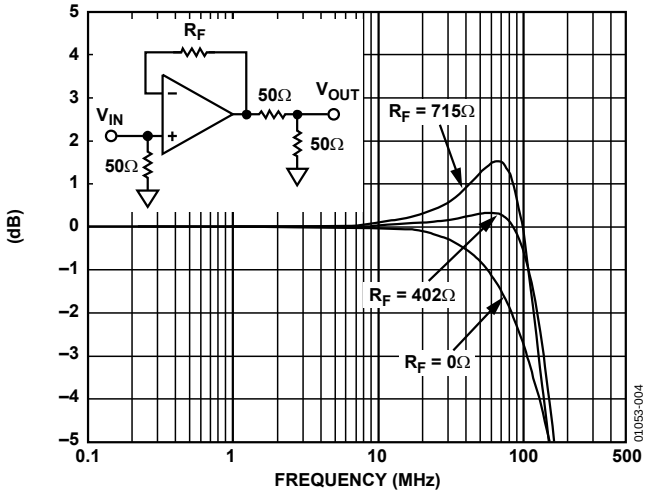

Figure 4. Frequency Response vs. R_F, G = +1, V_S = ±12 V, V_{IN} = 63 mV p-p

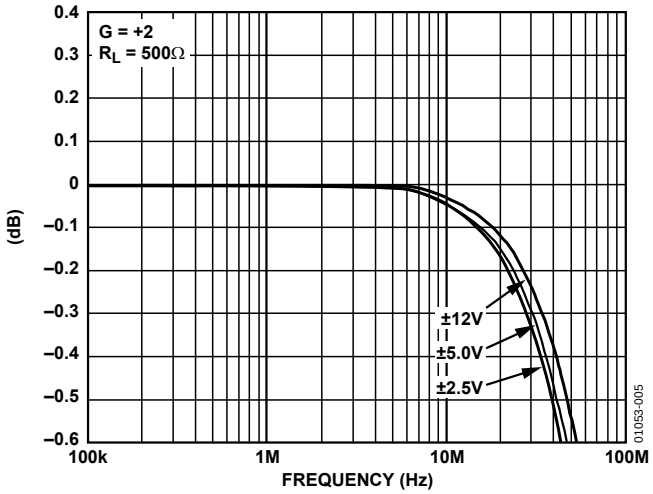

Figure 5. Fine-Scale Gain Flatness vs. Frequency, G = +2

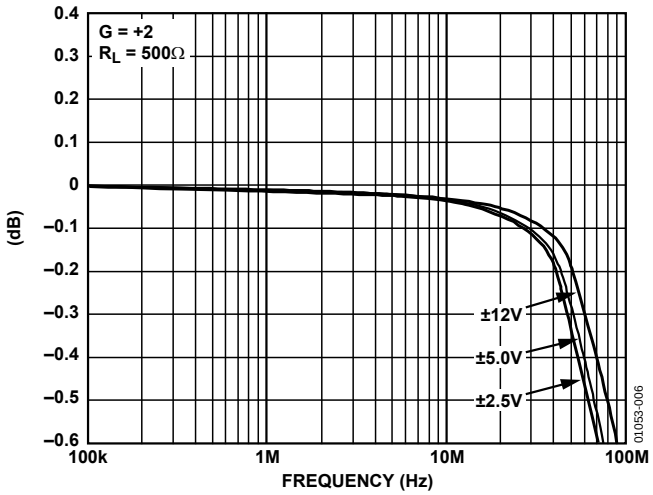

Figure 6. Fine-Scale Gain Flatness vs. Frequency, G = +1

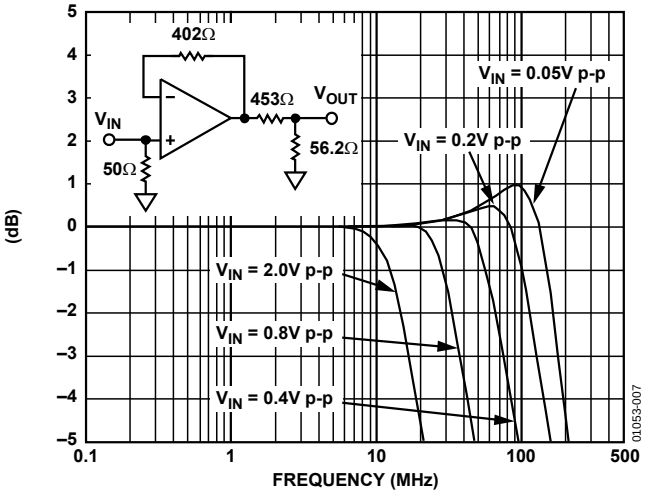

Figure 7. Frequency Response vs. Signal Level, V_S = ±12 V, G = +1

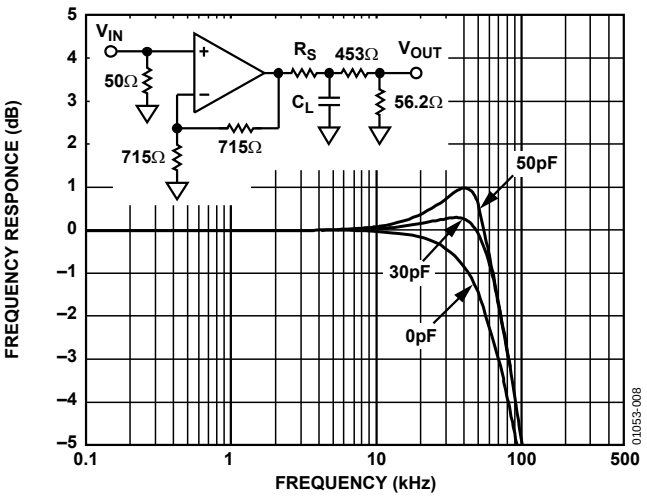

Figure 8. Frequency Response vs. Capacitive Load; C_L = 0 pF and 50 pF; R_S = 0 Ω

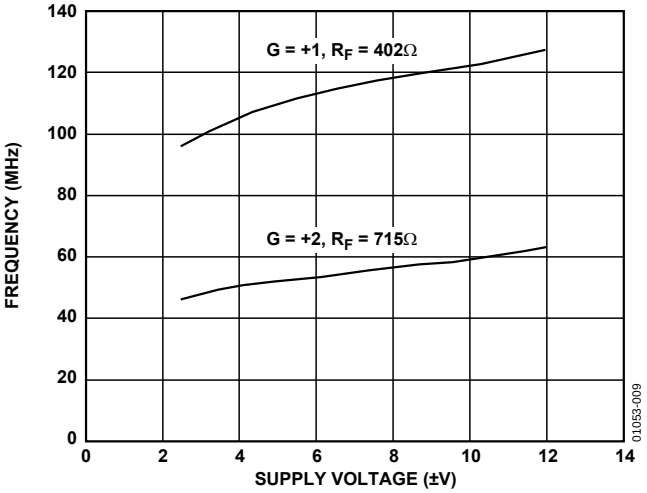

Figure 9. Bandwidth vs. Supply, R_L = 500 Ω, V_{IN} = 200 mV p-p

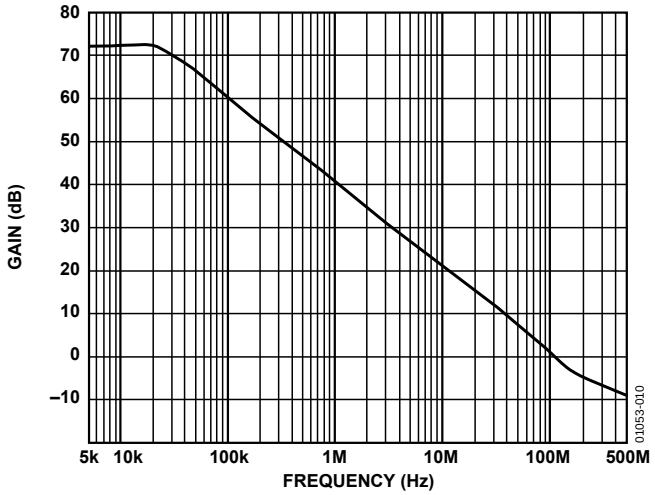

Figure 10. Open-Loop Gain vs. Frequency

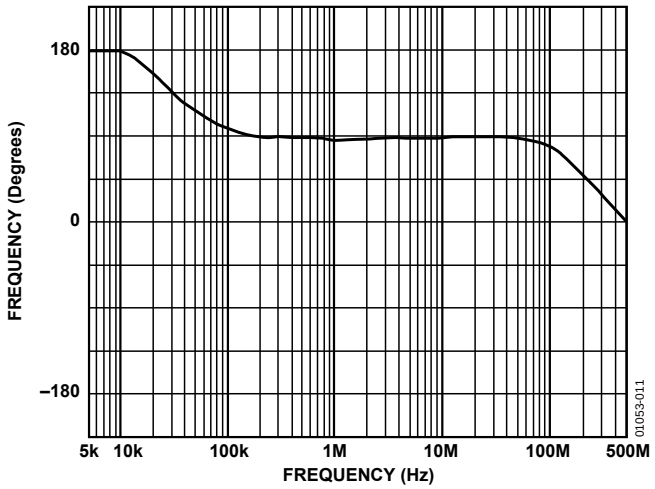

Figure 11. Open-Loop Phase vs. Frequency

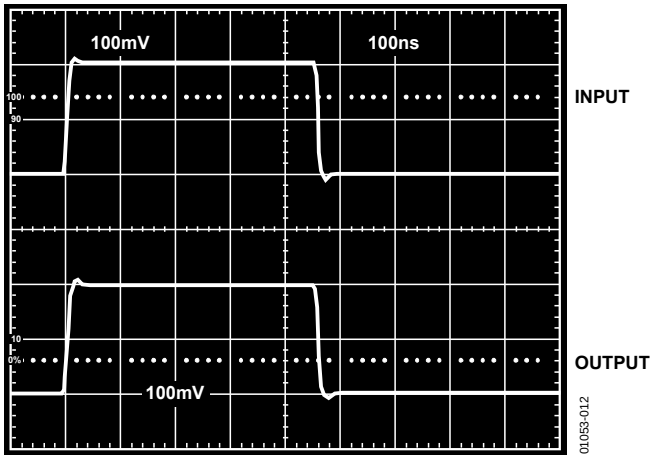

Figure 12. Noninverting Small Signal Pulse Response, $R_L = 500\ \Omega$, $V_S = \pm 12$ V, $G = +1$, $R_F = 0\ \Omega$

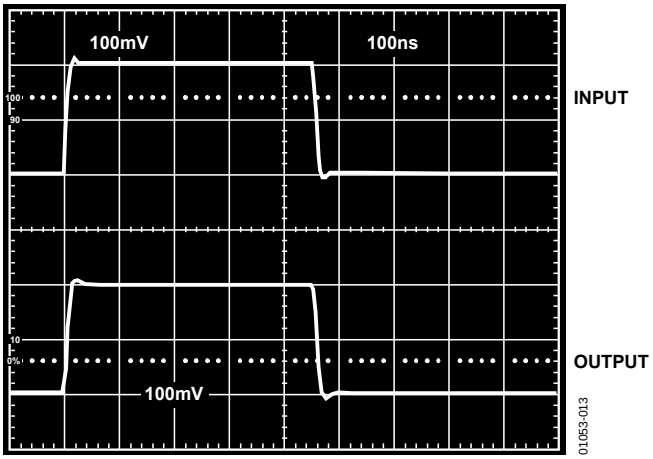

Figure 13. Noninverting Small Signal Pulse Response, $R_L = 500\ \Omega$, $V_S = \pm 2.5$ V, $G = +1$, $R_F = 0\ \Omega$

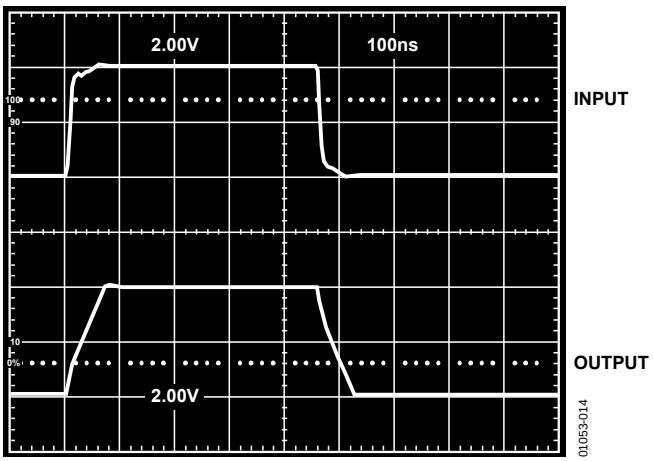

Figure 14. Noninverting Large Signal Pulse Response, $R_L = 500\ \Omega$, $V_S = \pm 12$ V, $G = +1$, $R_F = 0\ \Omega$

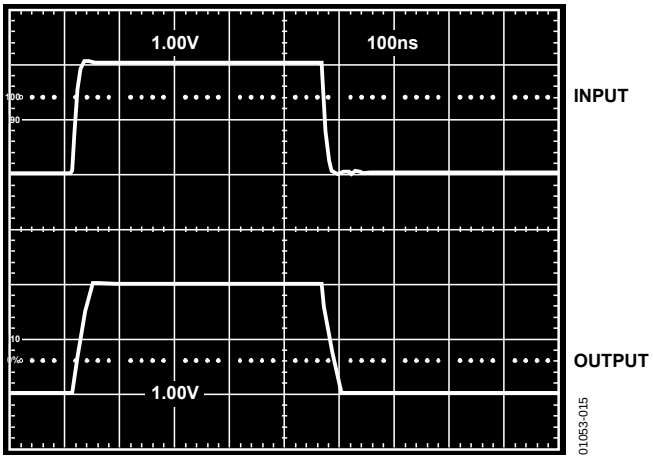

Figure 15. Noninverting Large Signal Pulse Response, $R_L = 500\ \Omega$, $V_S = \pm 2.5$ V, $G = +1$, $R_F = 0\ \Omega$

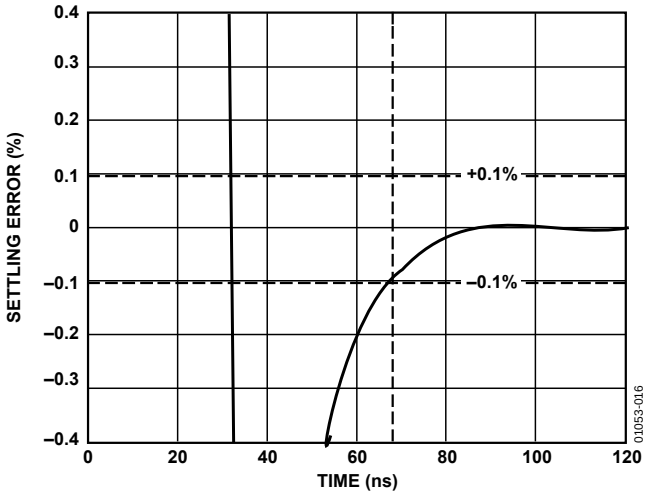

Figure 16. Settling Time to 0.1%, V_S = ±12 V, Step Size = 2 V p-p, G = +2, R_L = 500 Ω

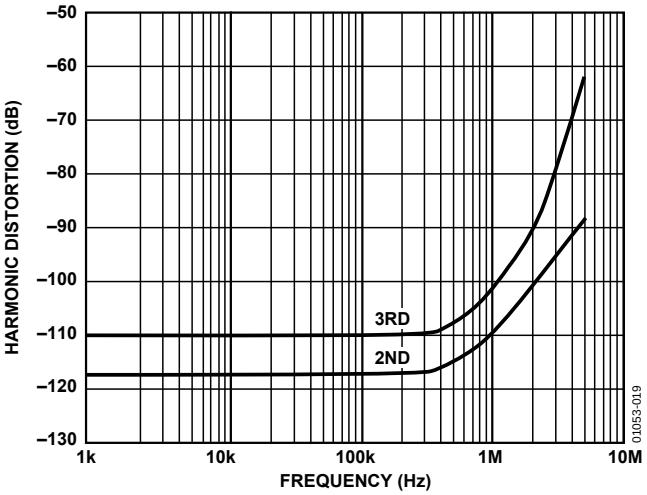

Figure 19. Distortion vs. Frequency, V_S = ±12 V, R_L = 500 Ω, R_F = 0 Ω, V_{OUT} = 2 V p-p, G = +1

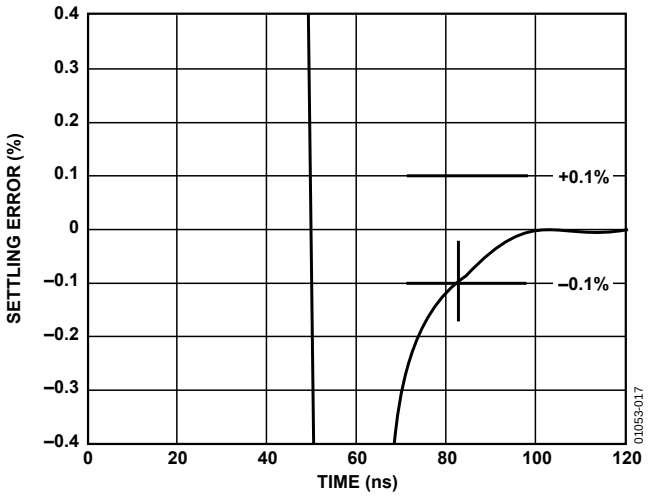

Figure 17. Settling Time to 0.1%, V_S = ±2.5 V, Step Size = 2 V p-p, G = +2, R_L = 500 Ω

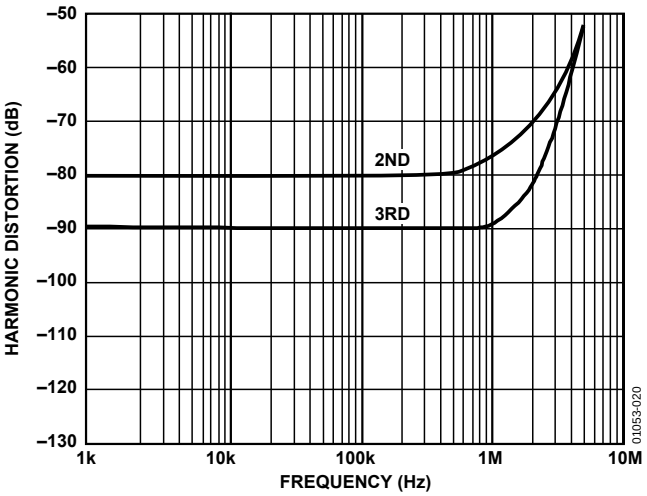

Figure 20. Distortion vs. Frequency, V_S = ±2.5 V, R_L = 500 Ω, R_F = 0 Ω, V_{OUT} = 2 V p-p, G = +1

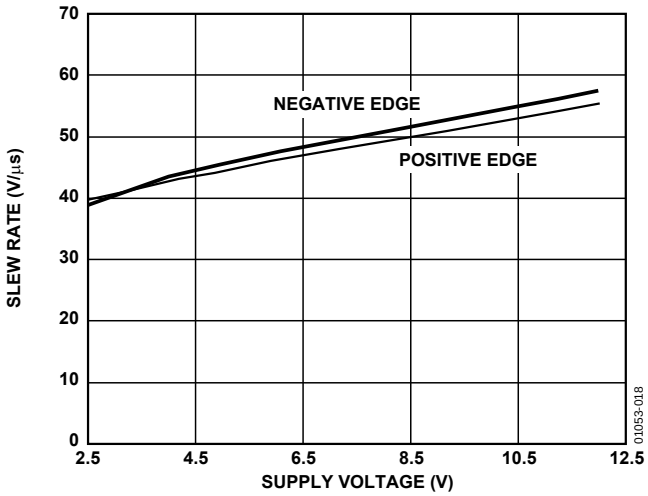

Figure 18. Slew Rate vs. Supply Voltage, G = +2

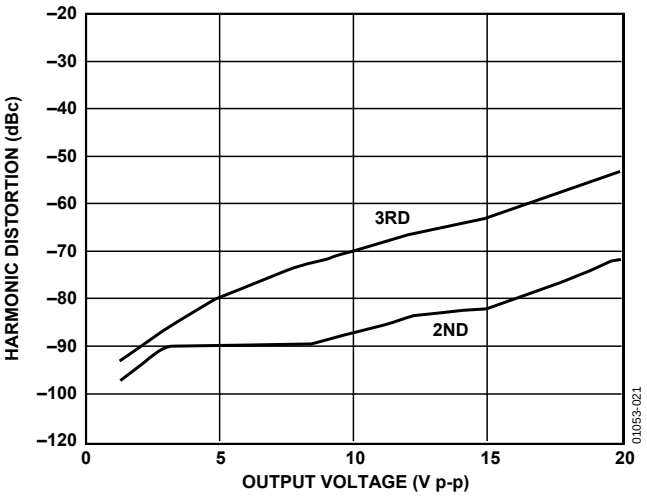

Figure 21. Distortion vs. Output Voltage, V_S = ±12 V, G = +2, f = 1 MHz, R_L = 500 Ω, R_F = 715 Ω

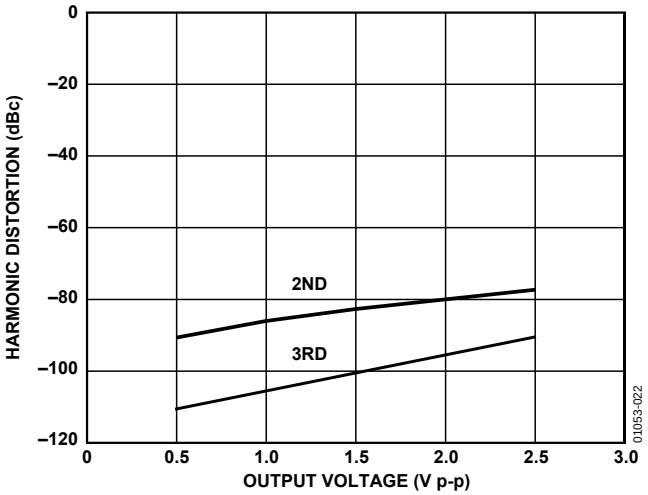

Figure 22. Distortion vs. Output Voltage, V_S = ±2.5 V, G = +1, f = 1 MHz, R_L = 500 Ω, R_F = 0 Ω

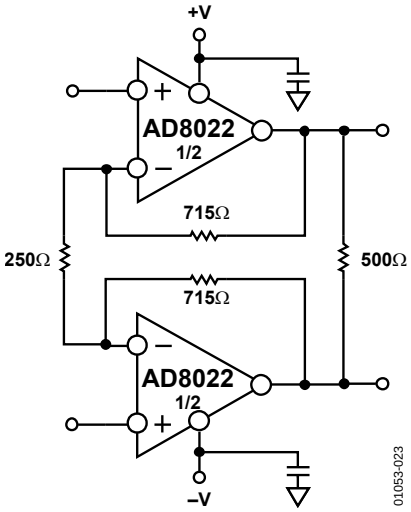

Figure 23. Multitone Power Ratio Test Circuit

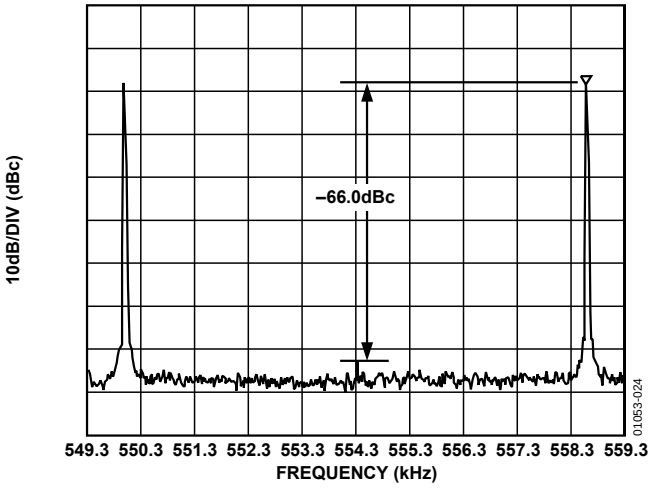

Figure 24. Multitone Power Ratio: V_S = ±12 V, R_L = 500 Ω, Full Rate ADSL (DMT), Downstream

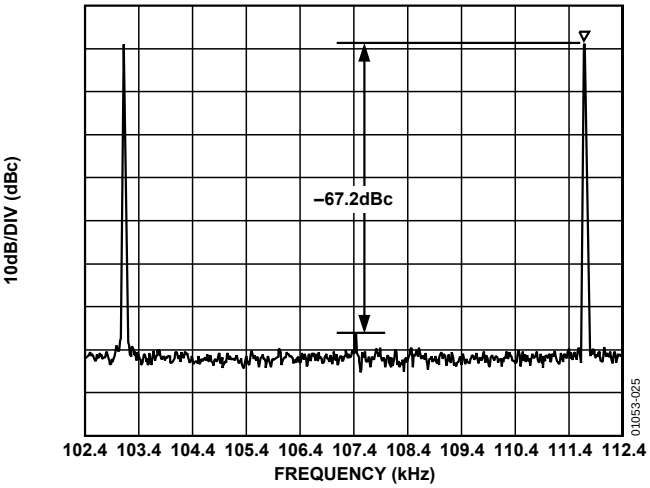

Figure 25. Multitone Power Ratio: V_S = ±12 V, R_L = 500 Ω, Full Rate ADSL (DMT), Upstream

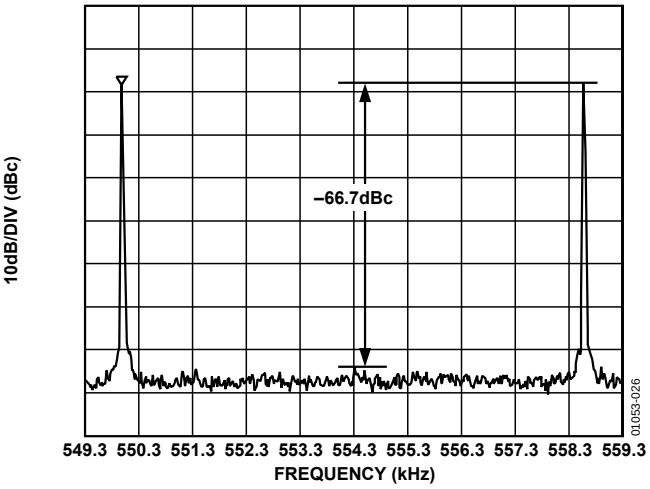

Figure 26. Multitone Power Ratio: V_S = ±6 V, R_L = 500 Ω, Full Rate ADSL (DMT), Downstream

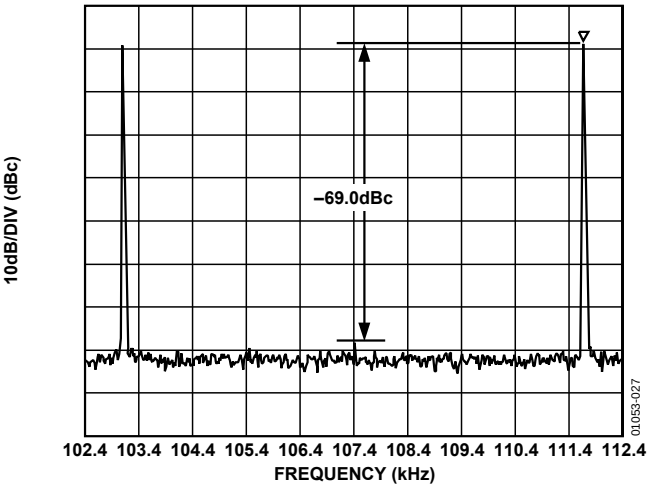

Figure 27. Multitone Power Ratio: V_S = ±6 V, R_L = 500 Ω, Full Rate ADSL (DMT), Upstream

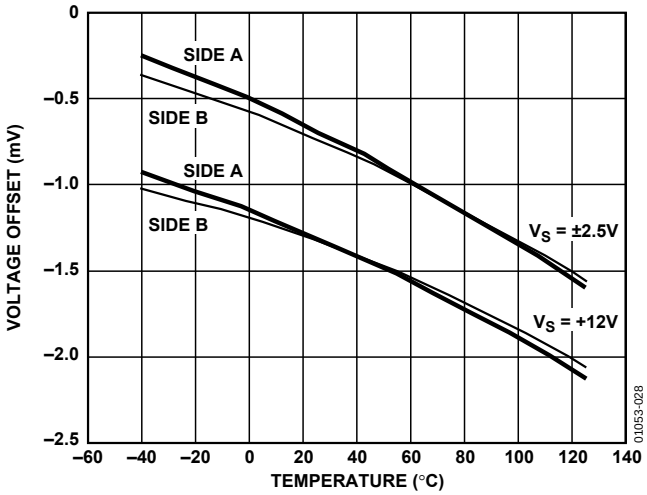

Figure 28. Voltage Offset vs. Temperature

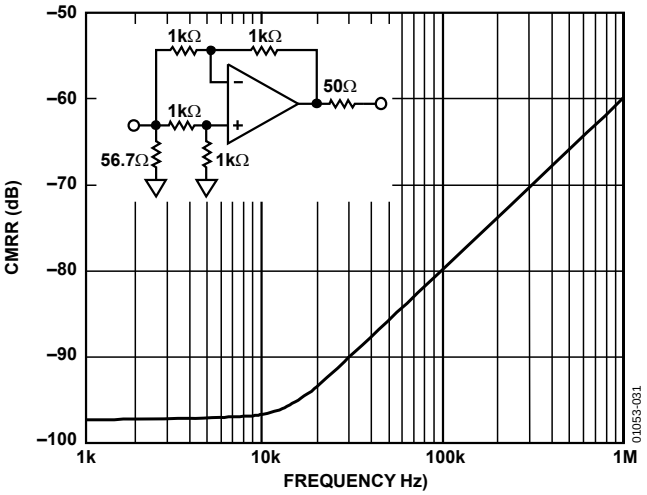

Figure 31. CMRR vs. Frequency

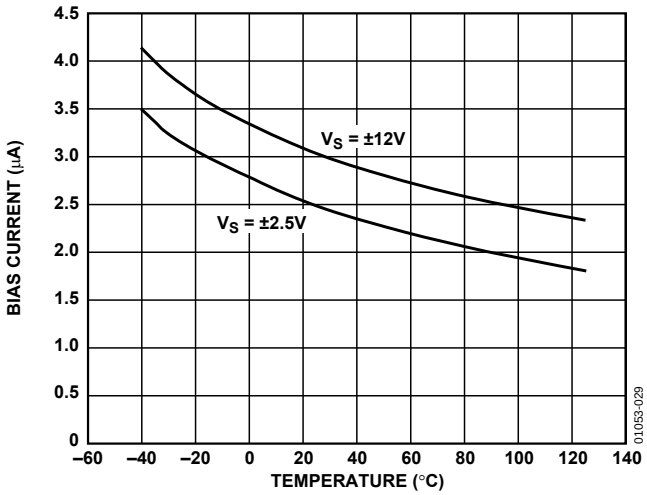

Figure 29. Bias Current vs. Temperature

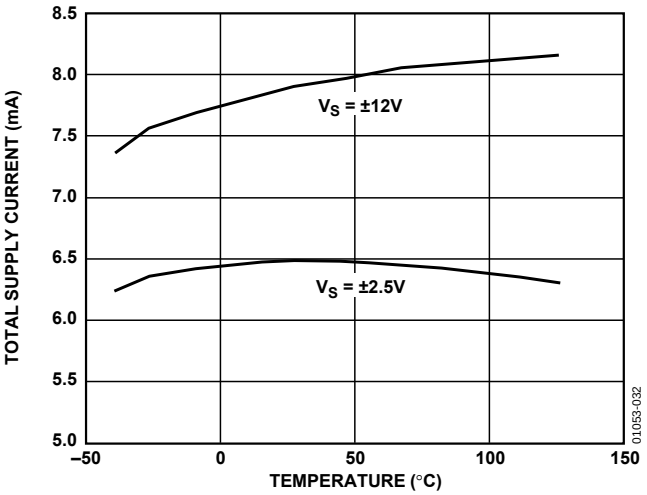

Figure 32. Total Supply Current vs. Temperature

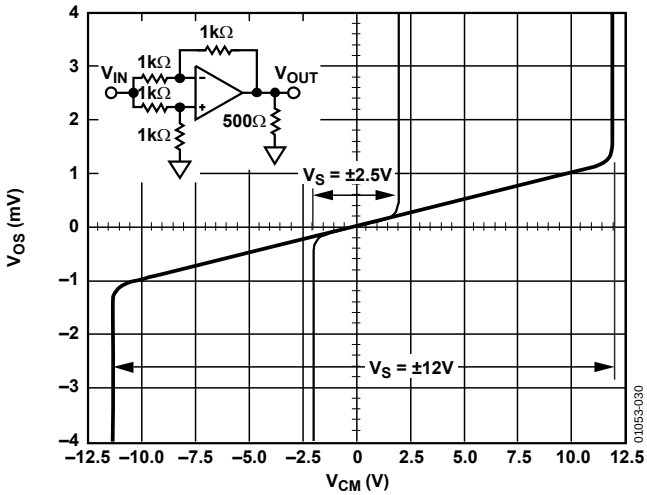

Figure 30. Voltage Offset vs. Input Common-Mode Voltage

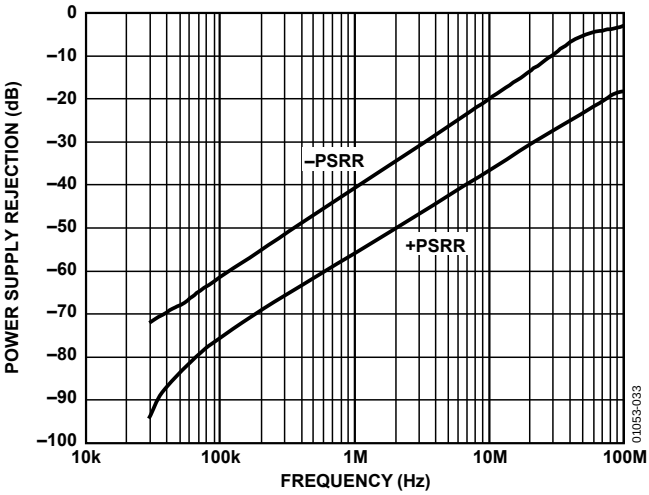

Figure 33. Power Supply Rejection vs. Frequency V_S = ±12 V

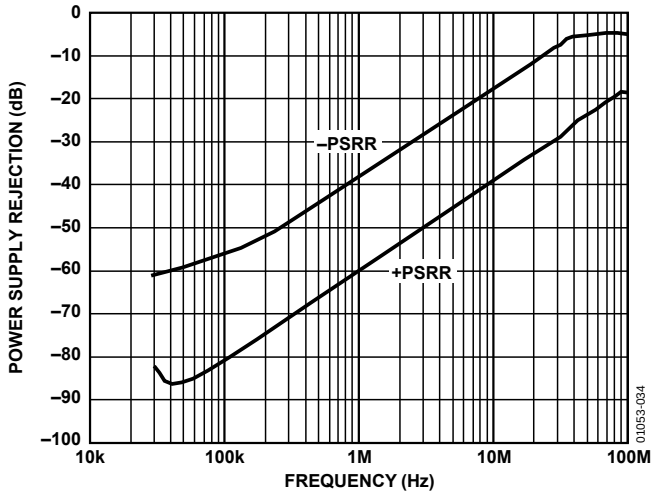

Figure 34. Power Supply Rejection vs. Frequency V_S = ±2.5 V

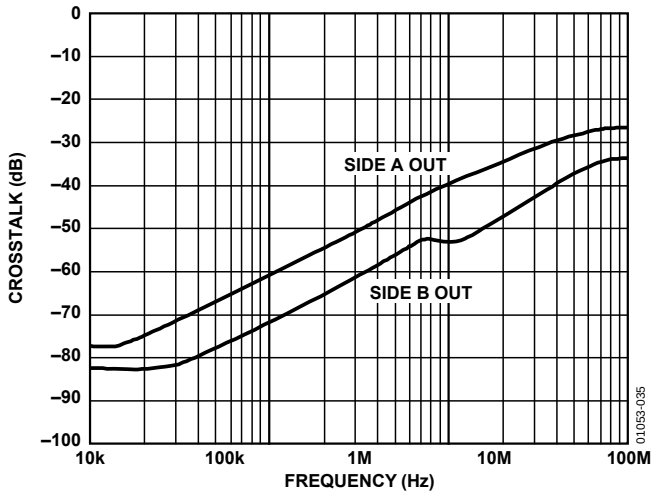

Figure 35. Output-to-Output Crosstalk vs. Frequency, V_S = ±12 V

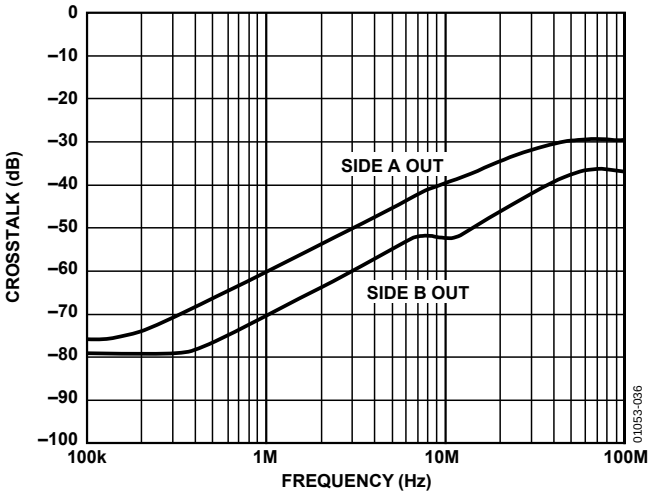

Figure 36. Output-to-Output Crosstalk vs. Frequency, V_S = ±2.5 V

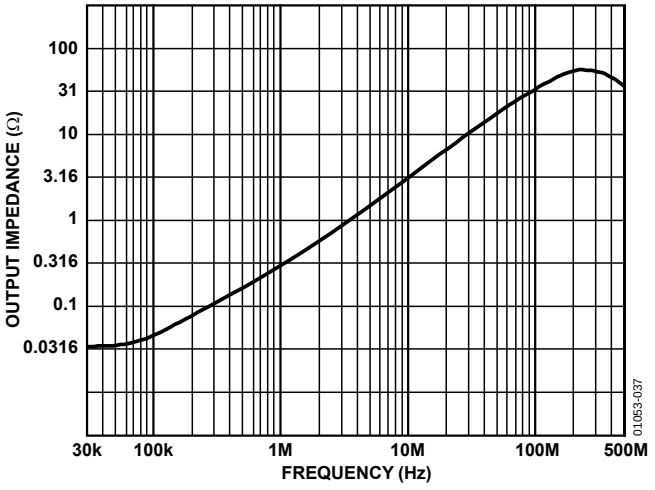

Figure 37. Output Impedance vs. Frequency, V_S = ±12 V

THEORY OF OPERATION

The AD8022 is a voltage-feedback op amp designed especially for ADSL or other applications requiring very low voltage and current noise along with low supply current, low distortion, and ease of use.

The AD8022 is fabricated on Analog Devices' proprietary eXtra-Fast Complementary Bipolar (XFCB) process, which enables the construction of PNP and NPN transistors with similar fTs in the 4 GHz region. The process is dielectrically isolated to eliminate the parasitic and latch-up problems caused by junction isolation. These features enable the construction of high frequency, low distortion amplifiers with low supply currents.

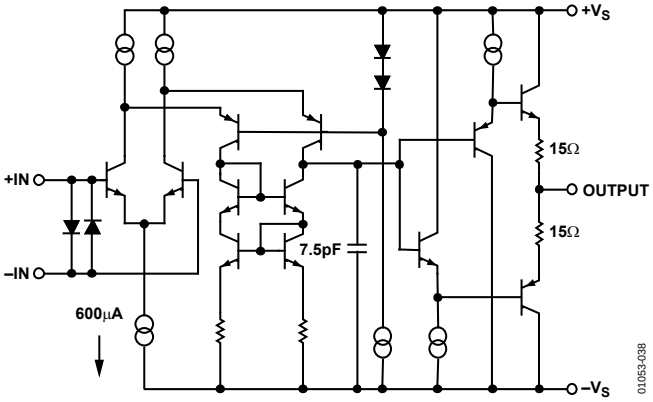

Figure 38. Simplified Schematic

As shown in Figure 38, the AD8022 input stage consists of an NPN differential pair in which each transistor operates a 300 µA collector current. This gives the input devices a high transconductance and therefore gives the AD8022 a low input noise of 2.5 nV/√Hz @ 100 kHz. The input stage drives a folded cascode that consists of a pair of PNP transistors. These PNPs then drive a current mirror that provides a differential input to single-ended output conversion. The output stage provides a high current gain of 10,000 so that the AD8022 can maintain a high dc open-loop gain, even into low load impedances.

APPLICATIONS

The low noise AD8022 dual xDSL receiver amplifier is specifically designed for the dual differential receiver amplifier function within xDSL transceiver hybrids, as well as other low noise amplifier applications. The AD8022 can be used in receiving modulated signals including discrete multitone (DMT) on either end of the subscriber loop. Communication systems designers can be challenged when designing an xDSL modem transceiver hybrid capable of receiving the smallest signals embedded in noise that inherently exists on twisted-pair phone lines. Noise sources include near-end crosstalk (NEXT), far-end crosstalk (FEXT), background, and impulse noise, all of which are fed, to some degree, into the receiver front end. Based on a Bellcore noise survey, the background noise level for typical twisted-pair telephone loops is −140 dBm/√Hz or 31 nV/√Hz. It is therefore important to minimize the noise added by the receiver amplifiers to preserve as much signal-to-noise ratio (SNR) as possible. With careful transceiver hybrid design, using the AD8022 dual, low noise, receiver amplifier to maintain power density levels lower than −140 dBm/√Hz in ADSL modems is easily achieved.

DMT MODULATION AND MULTITONE POWER RATIO (MTPR)

ADSL systems rely on discrete multitone DMT modulation to carry digital data over phone lines. DMT modulation appears in the frequency domain as power contained in several individual frequency subbands, sometimes referred to as tones or bins, each of which is uniformly separated in frequency. (See Figure 24 to Figure 27 for MTPR results while the AD8022 receives DMT driving 800 mV rms across a 500 Ω differential load.) A uniquely encoded quadrature amplitude modulation (QAM) signal occurs at the center frequency of each subband or tone. Difficulties exist when decoding these subbands if a QAM signal from one subband is corrupted by the QAM signal(s) from other subbands, regardless of whether the corruption comes from an adjacent subband or harmonics of other subbands. Conventional methods of expressing the output signal integrity of line receivers, such as spurious-free dynamic range (SFDR), single tone harmonic distortion (THD), two-tone intermodulation distortion (IMD), and third-order intercept (IP3), become significantly less meaningful when amplifiers are required to process DMT and other heavily modulated waveforms. A typical xDSL downstream DMT signal can contain as many as 256 carriers (subbands or tones) of QAM signals. MTPR is the relative difference between the measured power in a typical subband (at one tone or carrier) vs. the power at another subband specifically selected to contain no QAM data.

In other words, a selected subband (or tone) remains open or void of intentional power (without a QAM signal) yielding an empty frequency bin. MTPR, sometimes referred to as the empty bin test, is typically expressed in dBc, similar to expressing the relative difference between single tone fundamentals and second or third harmonic distortion components. Measurements of MTPR are typically made at the output of the receiver directly across the differential load. Other components aside, the receiver function of an ADSL transceiver hybrid is affected by the turns ratio of the selected transformers within the hybrid design. Since a transformer reflects the secondary voltage back to the primary side by the inverse of the turns ratio, 1/N, increasing the turns ratio on the secondary side reduces the voltage across the primary side inputs of the differential receiver. Increasing the turns ratio of the transformers can inadvertently cause a reduction of the SNR by reducing the received signal strength.

CHANNEL CAPACITY AND SNR

The efficiency of an ADSL system in delivering the digital data embedded in the DMT signals can be compromised when the noise power of the transmission system increases. Figure 39 shows the relationship between SNR and the relative maximum number of bits per tone or subband while maintaining a bit error rate at 10^{-7} errors per second.

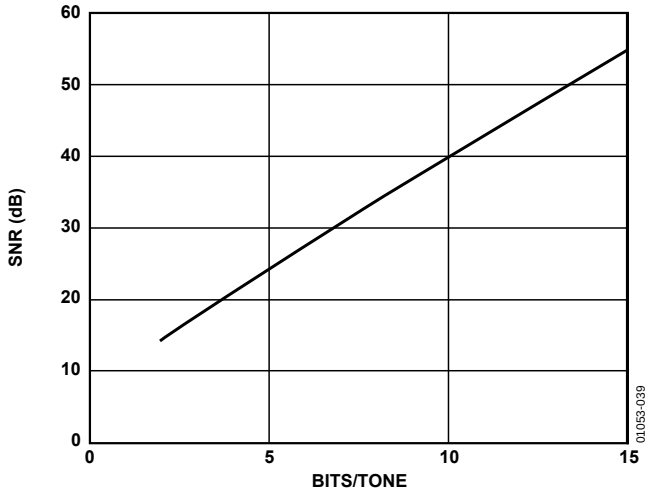

Figure 39. ADSL DMT SNR vs. Bits/Tone

POWER SUPPLY AND DECOUPLING

The AD8022 should be powered with a good quality (that is, low noise) dual supply of ±12 V for the best overall performance. The AD8022 circuit also functions at voltages lower than ±12 V. Careful attention must be paid to decoupling the power supply pins. A pair of 10 µF capacitors located in near proximity to the AD8022 is required to provide good decoupling for lower frequency signals. In addition, 0.1 µF decoupling capacitors should be located as close to each of the power supply pins as is physically possible.

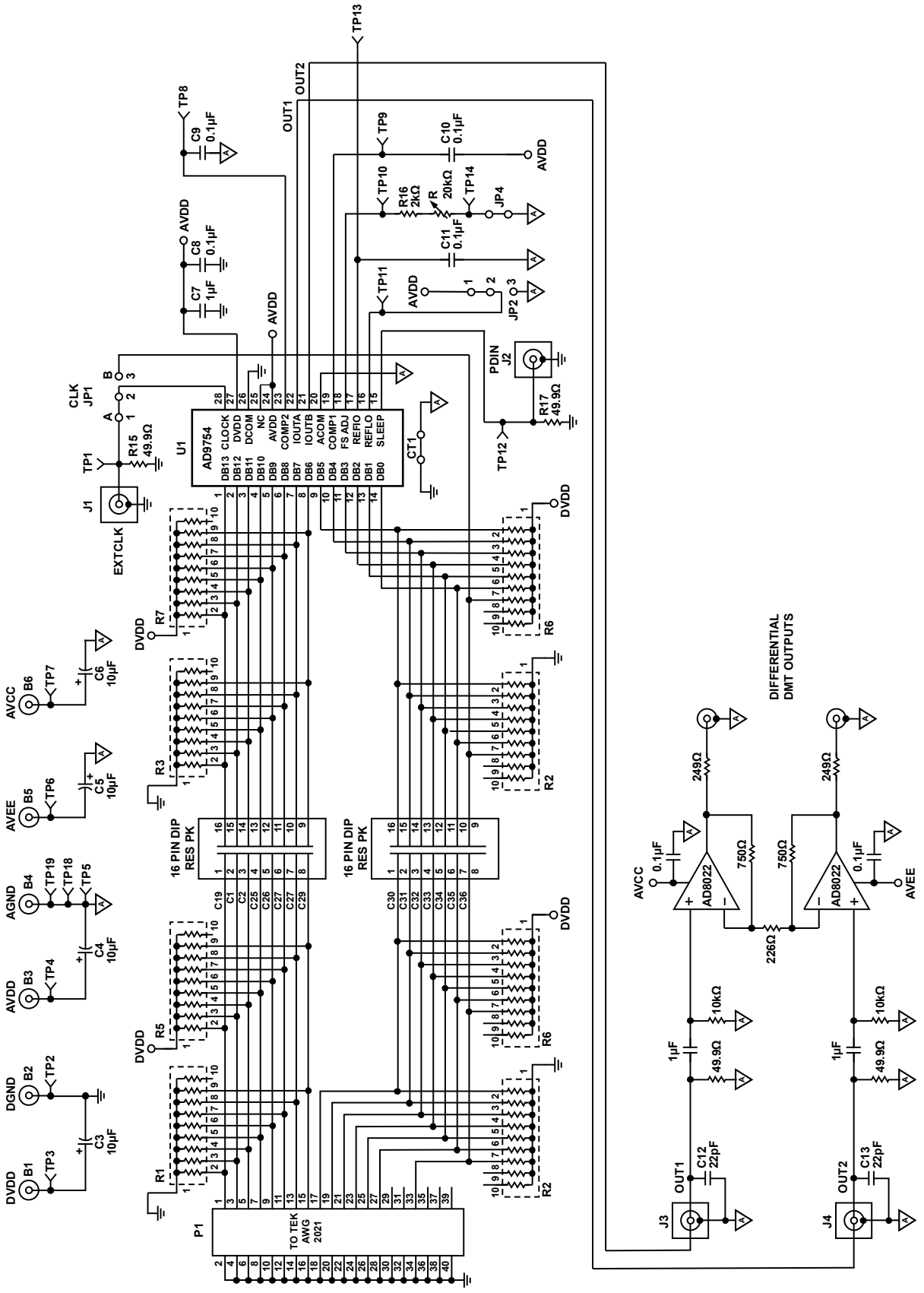

Figure 40. DMT Signal Generator Schematic

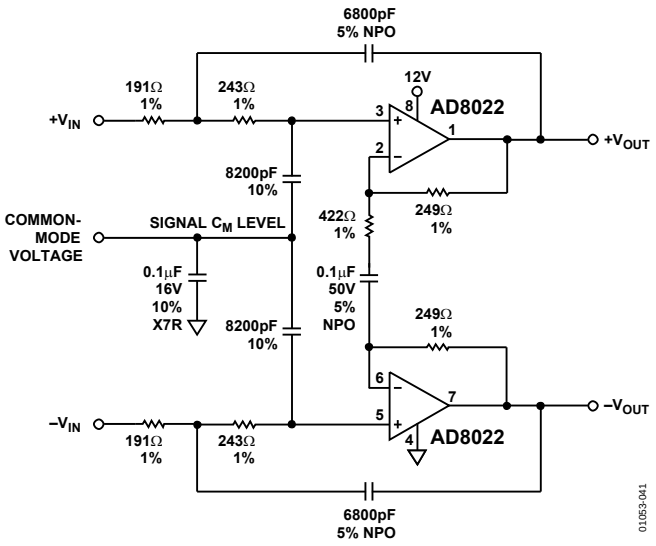

Figure 41. Differential Input Sallen-Key Filter Using AD8022 on Single Supply, +12 V

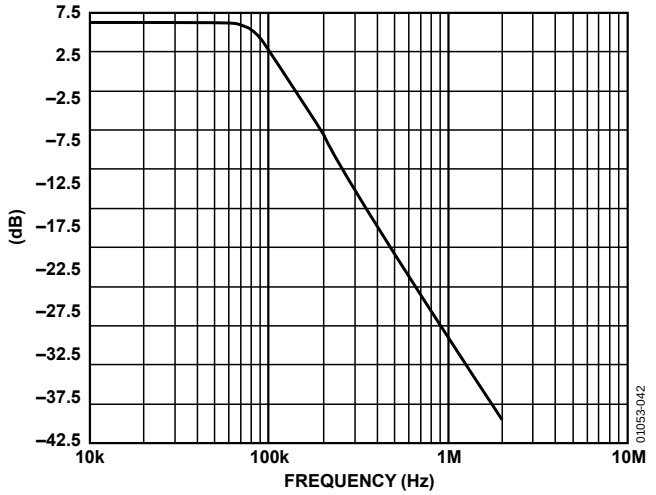

Figure 42. Frequency Response of Sallen-Key Filter

LAYOUT CONSIDERATIONS

As is the case with all high speed amplifiers, careful attention to printed circuit board layout details prevent associated board parasitics from becoming problematic. Proper RF design technique is mandatory. The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance return path. Removing the ground plane from the area near the input signal lines reduces stray capacitance. Chip capacitors should be used for supply bypassing. One end of the capacitor should be connected to the ground plane, and the other should be connected no more than 1/8 inch away from each supply pin. An additional large (0.47 µF to 10 µF) tantalum capacitor should be connected in parallel, although not necessarily as close, in order to supply current for fast, large signal changes at the AD8022 output. Signal lines connecting the feedback and gain resistors should be as short as possible, minimizing the inductance and stray capacitance associated with these traces. Locate termination resistors and loads as close as possible to the input(s) and output, respectively. Adhere to stripline design techniques for long signal traces (greater than about 1 inch). Following these generic guidelines improves the performance of the AD8022 in all applications.

OUTLINE DIMENSIONS

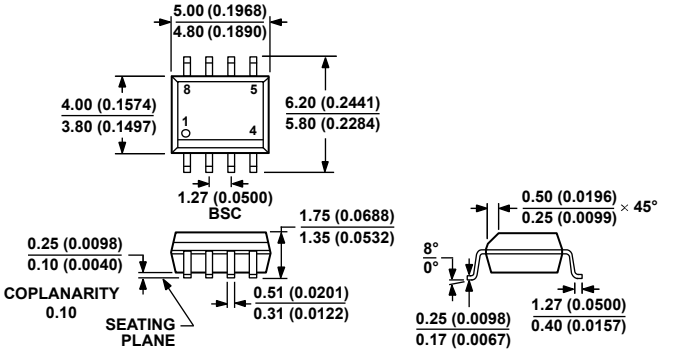

Figure 43. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)—Dimensions shown in millimeters and (inches)

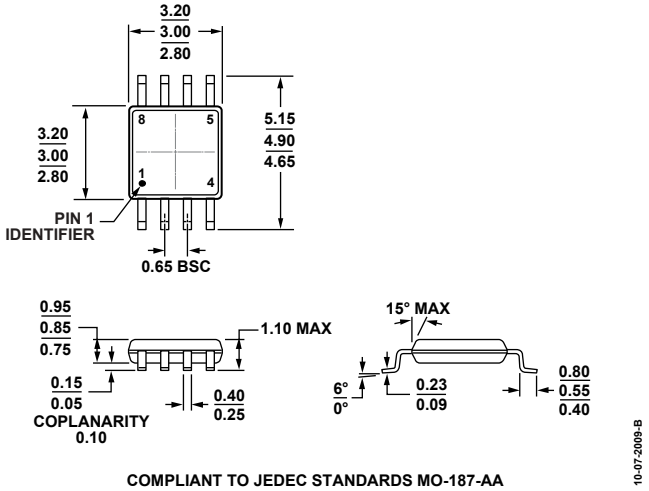

Figure 44. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)—Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8022AR	−40°C to +85°C	8-Lead SOIC_N	R-8
AD8022ARZ	−40°C to +85°C	8-Lead SOIC_N	R-8
AD8022ARZ-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8
AD8022ARZ-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8
AD8022ARMZ	−40°C to +85°C	8-Lead MSOP	RM-8
AD8022ARMZ-REEL	−40°C to +85°C	8-Lead MSOP	RM-8
AD8022ARMZ-REEL7	−40°C to +85°C	8-Lead MSOP	RM-8
AD8022ARM-EBZ		Evaluation Board	
AD8022AR-EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.