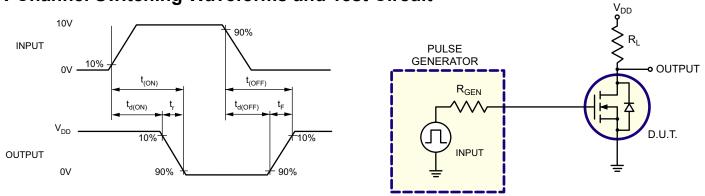
Sym	Parameter	Min Typ Max		Units	Conditions			
$BV_{DSS}$	Drain-to-source breakdown voltage	200	-	-	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 100µA		
$V_{\text{GS(th)}}$	Gate threshold voltage	0.6	-	2.0	V	$V_{GS} = V_{DS}, I_{D} = 1.0 \text{mA}$		
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	-4.5	mV/ºC	$V_{GS} = V_{DS}, I_{D} = 1.0 \text{mA}$		
I <sub>GSS</sub>	Gate body leakage	-	-	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$		
I <sub>DSS</sub>		-	-	1.0	μA	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 100V		
	Zero gate voltage drain current	-	-	10.0	μA	$V_{GS} = 0V,$ $V_{DS} = Max rating$		
		-	-	1.0	mA	$V_{GS} = 0V, T_A = 125^{\circ}C$ $V_{DS} = 0.8$ Max Rating		
I <sub>D(ON)</sub>	On state drain surrent	0.6	-	-	Δ	V <sub>GS</sub> = 4.5V, V <sub>DS</sub> = 25V		
	On-state drain current	1.2	-	-	A	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 25V		
R <sub>DS(ON)</sub>	Static drain-to-source on-state	-	-	8.0	0	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 150mA		
	resistance	-	-	7.0	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 1.0A		
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.0	%/°C	V <sub>GS</sub> = 4.5V, I <sub>D</sub> =150mA		
$G_{FS}$	Forward transconductance	150	-	-	mmho	V <sub>DS</sub> = 25V, I <sub>D</sub> = 200mA		
C <sub>ISS</sub>	Input capacitance	-	-	110		$V_{GS} = 0V,$ $V_{DS} = 25V,$ f = 1.0MHz		
C <sub>oss</sub>	Common source output capacitance	-	-	60	pF			
$C_{RSS}$	Reverse transfer capacitance	-	-	23				
t <sub>d(ON)</sub>	Turn-on delay time	-	-	20		$V_{DD} = 25V,$ $I_{D} = 150mA,$ $R_{GEN} = 25\Omega$		
t,	Rise time	-	-	15				
t <sub>d(OFF)</sub>	Turn-off delay time	-	-	25	ns			
t <sub>r</sub>	Fall time	-	-	25				
V <sub>SD</sub>	Diode forward voltage drop	-	-	1.8	V	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 200mA		
t <sub>rr</sub>	Reverse recovery time	-	300	-	ns	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 200mA		

## N-Channel Electrical Characteristics (T<sub>A</sub> = 25°C unless otherwise specified)

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

2. All A.C. parameters sample tested.

## **N-Channel Switching Waveforms and Test Circuit**



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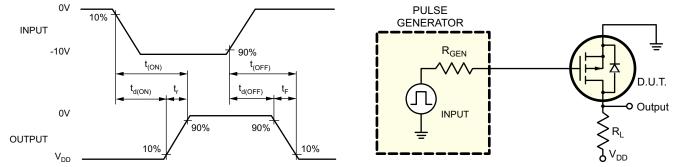
Sym	Parameter	Min Typ		Мах	Units	Conditions			
$BV_{DSS}$	Drain-to-source breakdown voltage	-200	-	-	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -2.0mA			
$V_{GS(th)}$	Gate threshold voltage	-1.0	-	-2.4	V	$V_{GS} = V_{DS}, I_{D} = -1.0 \text{mA}$			
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	4.5	mV/ºC	$V_{_{\rm GS}} = V_{_{\rm DS}}, I_{_{\rm D}} = -1.0 {\rm mA}$			
I <sub>GSS</sub>	Gate body leakage	-	-	-100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$			
I <sub>DSS</sub>		-	-	-10	μA	$V_{GS}$ = 0V, $V_{DS}$ = Max rating			
	Zero gate voltage drain current	-	-	-1.0	mA	$V_{GS} = 0V, T_A = 125^{\circ}C,$ $V_{DS} = 0.8$ Max Rating			
1	On-state drain current	-0.25	-0.7	-	A	V <sub>GS</sub> = -4.5V, V <sub>DS</sub> = -25V			
D(ON)		-0.75	-2.1	-	A	V <sub>GS</sub> = -10V, V <sub>DS</sub> = -25V			
D	Static drain-to-source on-state	-	10	15	Ω	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -100mA			
$R_{DS(ON)}$	resistance	-	8.0	12	12	V <sub>GS</sub> = -10V, I <sub>D</sub> = -200mA			
$\Delta R_{\rm DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.7	%/°C	V <sub>GS</sub> = -10V, I <sub>D</sub> =-200mA			
$G_{FS}$	Forward transconductance	100	250	-	mmho	V <sub>DS</sub> = -25V, I <sub>D</sub> = -200mA			
C <sub>ISS</sub>	Input capacitance	-	75	125		$V_{GS} = 0V,$ $V_{DS} = -25V,$			
C <sub>oss</sub>	Common source output capacitance	-	20	85	pF				
$C_{_{RSS}}$	Reverse transfer capacitance	-	10	35		f = 1.0MHz			
t <sub>d(ON)</sub>	Turn-on delay time	-	-	10					
t <sub>r</sub>	Rise time	-	-	15	ns	$V_{DD} = -25V,$			
$t_{d(OFF)}$	Turn-on delay time	-	-	20		$I_{\rm D} = -0.75 {\rm A},$ $R_{\rm GEN} = 25 {\Omega}$			
t <sub>r</sub>	Fall time	-	-	15					
V <sub>SD</sub>	Diode forward voltage drop	-	-	-1.8	V	V <sub>GS</sub> = 0V, I <sub>SD</sub> = -0.5A			
t <sub>rr</sub>	Reverse recovery time	-	300	-	ns	$V_{GS} = 0V, I_{SD} = -0.5A$			

## P-Channel Electrical Characteristics (T<sub>a</sub> = 25°C unless otherwise specified)

Notes:

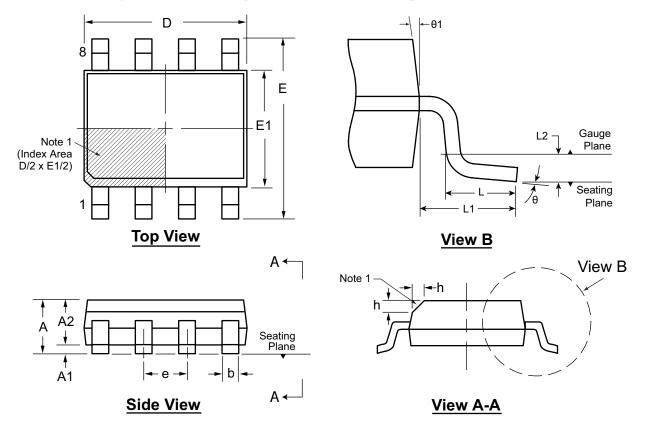
All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
All A.C. parameters sample tested.





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## 8-Lead SOIC (Narrow Body) Package Outline (TG) 4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note:

1. This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		Α	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	<b>0</b> 0	<b>5</b> °
Dimension (mm)	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			<b>8</b> 0	15 <sup>0</sup>

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

\* This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.

Drawings are not to scale.

Supertex Doc. #: DSPD-8SOLGTG, Version H101708.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <u>http://www.supertex.com/packaging.html</u>.)

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