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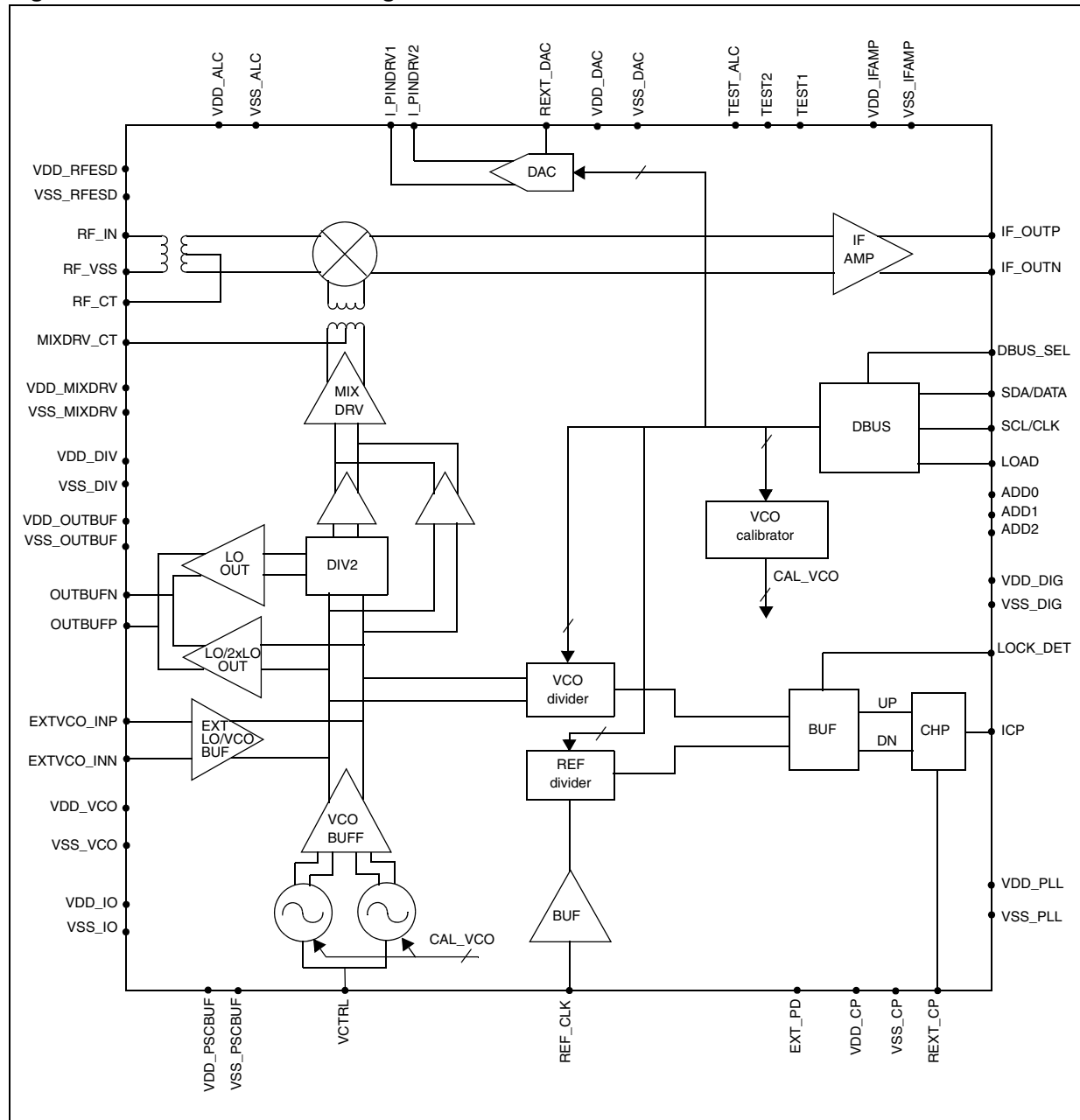
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# 1 Block diagram

Figure 1. STW82103B block diagram



## 2 Pin description

Figure 2. STW82103B pin configuration

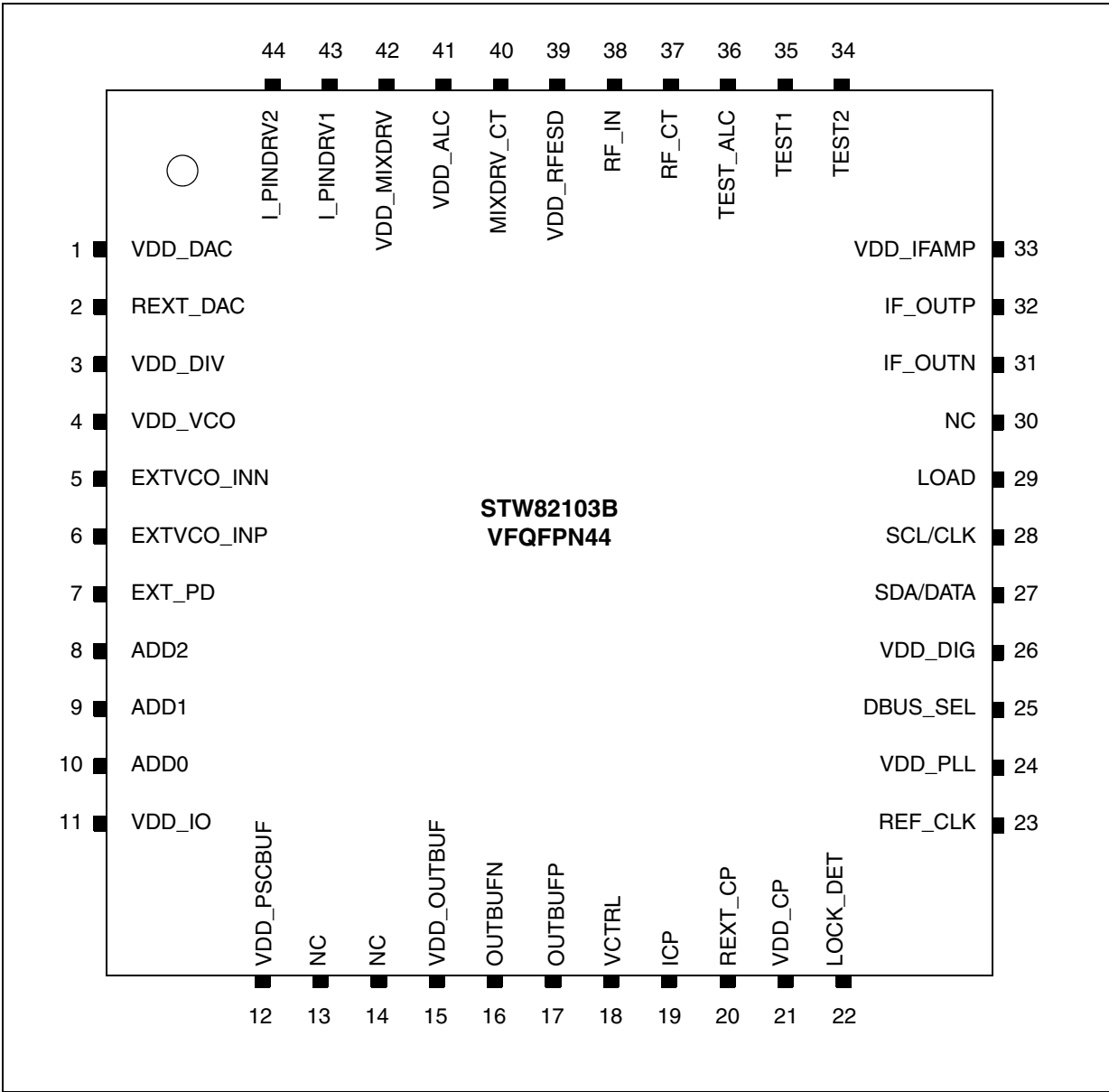


Table 2. Pin list

Pin No	Name	Description	Observation
1	VDD_DAC	DAC power supply	Vsupply analog1= 3.3 V
2	REXT_DAC	External resistance connection for DAC	-
3	VDD_DIV	Divider by 2 power supply	Vsupply analog1= 3.3 V
4	VDD_VCO	VCOs and External VCO Buffer power supply	Vsupply analog1= 3.3 V
5	EXTVCO_INN	External VCO (LO) negative input	Diversity Slave Mode and External VCO Modes; otherwise it must be connected to GND
6	EXTVCO_INP	External VCO (LO) positive input	Diversity Slave Mode and External VCO Modes; otherwise it must be connected to GND
7	EXT_PD	Hardware power down: '0' device ON; '1' device OFF	CMOS Input
8	ADD2	I <sup>2</sup> CBUS address select pin	CMOS Input
9	ADD1	I <sup>2</sup> CBUS address select pin	CMOS Input
10	ADD0	I <sup>2</sup> CBUS address select pin	CMOS Input
11	VDD_IO	Digital IO power supply	Vsupply digital = 3.3 V
12	VDD_PSCBUF	Prescaler input buffer power supply	Vsupply analog1= 3.3 V
13	NC	Not connected	-
14	NC	Not connected	-
15	VDD_OUTBUF	Power supply for LO buffer	Vsupply analog1= 3.3 V
16	OUTBUFN	LO Output buffer negative output	Open collector @ 3.3 V
17	OUTBUFP	LO Output buffer positive output	Open collector @ 3.3 V
18	VCTRL	Control voltage for VCOs	-
19	ICP	PLL charge pump output	-
20	REXT_CP	External resistance connection for PLL charge pump current	-
21	VDD_CP	Power supply for charge pump	Vsupply analog1= 3.3 V
22	LOCK_DET	Lock detector	CMOS Output
23	REF_CLK	Reference frequency input	-
24	VDD_PLL	PLL digital power supply	Vsupply analog1= 3.3 V
25	DBUS_SEL	Digital Bus Interface select	CMOS Input
26	VDD_DIG	Power supply for digital bus interface	Vsupply digital = 3.3 V
27	SDA/DATA	I <sup>2</sup> CBUS /SPI data line	CMOS Bidir Schmitt triggered
28	SCL/CLK	I <sup>2</sup> CBUS /SPI clock line	CMOS Input Schmitt triggered
29	LOAD	SPI load line	CMOS Input Schmitt triggered
30	NC	Not connected	-
31	IF_OUTN	IF amplifier negative output	Open collector @ 5 V <sup>(1)</sup>



Table 2. Pin list (continued)

Pin No	Name	Description	Observation
32	IF_OUTP	IF Amplifier positive output	Open collector @ 5 V <sup>(1)</sup>
33	VDD_IFAMP	IF Amplifier power supply	Vsupply analog1 = 3.3 V
34	TEST2	Test input 2	Test purpose only; it must be connected to GND
35	TEST1	Test input 1	Test purpose only; it must be connected to GND
36	TEST_ALC	Test output	Test purpose only; it must be connected to GND
37	RF_CT	RF balun central tap	-
38	RF_IN	RF input	-
39	VDD_RFESD	RF ESD positive rail power supply	Vsupply analog1 = 3.3 V
40	MIXDRV_CT	Mixer driver balun central tap	Vsupply analog2 = 5 V <sup>(1)</sup>
41	VDD_ALC	ALC power supply	Vsupply analog1 = 3.3 V
42	VDD_MIXDRV	Mixer driver power supply	Vsupply analog1 = 3.3 V
43	I_PINDRV1	DAC current output for external PIN Diode attenuator	PMOS Open drain
44	I_PINDRV2	DAC current output for external PIN Diode attenuator	PMOS Open drain

1. Supply voltage @ 3.3 V in low-current mode operation

### 3 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Values	Unit
AVCC1	Analog supply voltage	0 to 4.6	V
AVCC2	Analog supply voltage	0 to 6	V
DVCC	Digital supply voltage	0 to 4.6	V
Tstg	Storage temperature	+150	°C
ESD (Electro-static discharge)	HBM on pins 16, 17, 31, 32	0.8	kV
	HBM on pin 37, 38, 40	1	
	HBM on all remaining pins	2	
	CDM-JEDEC Standard on pin 38, 40	0.25	
	CDM-JEDEC Standard on all remaining pins	0.5	
	MM	0.2	

## 4 Operating conditions

**Table 4. Operating conditions**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
AVCC1	Analog Supply voltage	-	3.15	3.3	3.45	V
AVCC2	Analog Supply voltage	-	4.75	5	5.25	V
DVCC	Digital Supply voltage	-	3.15	3.3	3.45	V
I <sub>CC3.3V</sub>	Current Consumption at 3.3 V	Standard mode	-	130	150	mA
		External VCO standard mode	-	110	130	mA
		Diversity slave mode	-	105	120	mA
		Diversity master mode	-	155	180	mA
		External VCO diversity master mode	-	145	165	mA
I <sub>CC5V</sub>	Current Consumption	High current mode at 5 V	-	160	185	mA
		Low current mode at 3.3 V	-	90	105	mA
T <sub>A</sub>	Operating ambient temperature	-	-40		85	°C
T <sub>J</sub>	Maximum junction temperature	-	-		125	°C
Θ <sub>JA</sub>	Junction to ambient package thermal resistance <sup>(1)</sup>	Multi-layer JEDEC board	-	33	-	°C/W
Θ <sub>JB</sub>	Junction to board package thermal resistance <sup>(1)</sup>	Multi-layer JEDEC board	-	19	-	°C/W
Θ <sub>JC</sub>	Junction to case package thermal resistance <sup>(1)</sup>	Multi-layer JEDEC board	-	3	-	°C/W
Ψ <sub>JB</sub>	Thermal characterization parameter junction to board <sup>(1)</sup>	Multi-layer JEDEC board	-	18	-	°C/W
Ψ <sub>JT</sub>	Thermal characterization parameter junction to top case <sup>(1)</sup>	Multi-layer JEDEC board	-	0.3	-	°C/W

1. Refer to JEDEC standard JESD 51-12 for a detailed description of the thermal resistances and thermal parameters.

Data here presented are referring to a Multi-layer board according to JEDEC standard.

$T_J = T_A + \Theta_{JA} \cdot P_{diss}$  (in order to estimate  $T_J$  if ambient temperature  $T_A$  and dissipated power  $P_{diss}$  are known)

$T_J = T_B + \Psi_{JB} \cdot P_{diss}$  (in order to estimate  $T_J$  if board temperature  $T_B$  and dissipated power  $P_{diss}$  are known)

$T_J = T_T + \Psi_{JT} \cdot P_{diss}$  (in order to estimate  $T_J$  if top case temperature  $T_T$  and dissipated power  $P_{diss}$  are known)

Table 5. Digital logic levels

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Vil	Low level input voltage	-	-	-	0.2*Vdd	V
Vih	High level input voltage	-	0.8*Vdd	-	-	V
Vhyst	Schmitt trigger hysteresis	-	0.8	-	-	V
Vol	Low level output voltage	-	-	-	0.4	V
Voh	High level output voltage	-	0.85*Vdd	-	-	V

## 5 Test conditions

Unless otherwise specified the following test conditions are applied:

- V<sub>supply digital</sub> = 3.3 V
- V<sub>supply analog1</sub> = 3.3 V
- V<sub>supply analog2</sub> = 5 V
- F<sub>IF</sub> = 150 MHz
- MIX = 0111
- T<sub>ambient</sub> = 27 °C

Refer also to [Section 11: Application information](#).

## 6 Electrical characteristics

Note:  $V_{\text{supply digital}} = 3.3 \text{ V}$ ,  $V_{\text{supply analog1}} = 3.3 \text{ V}$ ,  $V_{\text{supply analog2}} = 5 \text{ V}$ ,  $F_{\text{RF}} = 2500 \text{ MHz}$ ,  $F_{\text{LO}} = 2350 \text{ MHz}$ ,  $T_A = +25^\circ\text{C}$ , RF power = 0 dBm, unless otherwise specified.

**Table 6. Down converter mixer and IF amplifier electrical characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{\text{RF}}$	RF Frequency	-	2300	-	2700	MHz
$F_{\text{LO}}$	LO Frequency	VCOA divided by 2	2200	-	2550	MHz
		VCOB	2500	-	3000	MHz
$F_{\text{IF}}$	IF Center Frequency <sup>(2)</sup>	$F_{\text{IF}} = \text{ABS}(F_{\text{LO}} - F_{\text{RF}})$	70	-	400	MHz
CG	Power Conversion Gain	$R_{\text{in}} = 50 \text{ ohm}$ , $R_{\text{out}} = 200 \text{ ohm}$ $R_{\text{Fin}} = 0 \text{ dBm}$	7.5	8	8.5	dB
$\text{CG}_{\Delta T}$	Power Conversion Gain over Temperature <sup>(3)</sup>	$T = -40 \text{ to } +85^\circ\text{C}$	-	$\pm 0.7$	-	dB
$\text{IP}_{1\text{dB}}$	Input P1dB	High current Mode	-	14	-	dBm
		Low current Mode	-	8	-	
IIP3	Third-order input intercept point <sup>(4)</sup>	High current Mode	23.5	25	-	dBm
		Low current Mode	17.5	19	-	
$\text{IIP3}_{\Delta T}$	IIP3 variation over temperature <sup>(3)</sup>	$T = -40 \text{ to } +85^\circ\text{C}$	-	$\pm 0.5$	-	dB
$nF_{\text{RF}} - nF_{\text{LO}}$	Spurious rejection at IF <sup>(3)</sup>	$2F_{\text{RF}} - 2F_{\text{LO}}$ $F_{\text{RFin}} = -5 \text{ dBm}$ , $F_{\text{IF}} = 150 \text{ MHz}$	-	80	-	dBc
		$3F_{\text{RF}} - 3F_{\text{LO}}$ $F_{\text{RFin}} = -5 \text{ dBm}$ , $F_{\text{IF}} = 150 \text{ MHz}$	-	76	-	dBc
$\text{NF}_{\text{SSB}}$	Noise figure	High-current mode, MIX = 0011	-	10.5	11	dB
		Low-current mode, MIX = 0011	-	10.5	11	dB
-	LO to IF Leakage	1xLO	-	-45	-	dBm
		2xLO	-	-38	-	
-	LO to RF Leakage	-	-	-28	-	dBm
-	RF to IF Isolation	-	-	58	-	dB
$\text{RF}_{\text{RL}}$	RF Return Loss	Matched to 50 ohm	-	20	-	dB
$\text{IF}_{\text{RL}}$	IF Return Loss	Matched to 200 ohm	-	22	-	dB
-	Gain Flatness for TX observation path <sup>(5)</sup>	Maximum deviation from $F_c$ over $\pm 10 \text{ MHz}$ . For any $F_c$ within each TX observation path band.	-0.05	-	+0.05	dB
		Maximum deviation from $F_c$ over $\pm 30 \text{ MHz}$ . For any $F_c$ within each TX observation path band.	-0.10	-	+0.10	dB

**Table 6. Down converter mixer and IF amplifier electrical characteristics<sup>(1)</sup> (continued)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
-	Phase Flatness for TX observation path <sup>(5)</sup>	Maximum deviation from linear phase at $F_c$ over $\pm 10$ MHz. For any $F_c$ within each TX observation path band.	-0.3	-	+0.3	deg
		Maximum deviation from linear phase at $F_c$ over $\pm 30$ MHz. For any $F_c$ within each TX observation path band.	-0.7	-	+0.7	deg
-	Gain Flatness for RX path <sup>(5)</sup>	Maximum ripple over a 4 MHz band. For any $F_c$ within each RX path band.	-	-	0.1	dB pk-pk
-	Phase Flatness for RX path <sup>(5)</sup>	Maximum ripple over a 4 MHz band. For any $F_c$ within each RX path band.	-	-	0.6	deg pk-pk
$ICC_{MD}$	Mixer Driver Current Consumption	3.3 V Supply (pin 41, 42)	-	45	-	mA
		5 V Supply (pin 40)	-	55	-	mA
	Mixer Driver Current Consumption (Low Current Mode)	3.3 V Supply (pin 41, 42)	-	20	-	mA
		3.3 V Supply (pin 40)	-	35	-	mA
$ICC_{IFAM}$	IFAMP Current Consumption	3.3 V Supply (pin 33)	-	10	-	mA
		5 V Supply (pin 31, 32)	-	107	-	mA
	IFAMP Current Consumption (Low Current Mode)	3.3 V Supply (pin 33)	-	6	-	mA
		3.3 V Supply (pin 31, 32)	-	55	-	mA

1. All linearity and NF performances are intended at maximum LO amplitude (LO\_A[1:0]=[11]), tuning capacitors (CAP[2:0]) programmed according to the selected frequency, mixer bias (MIX[3:0]) set to maximize performance and the device operated in high current mode. The performances of conversion gain, NF and linearity are intended at the SMA connectors of a typical application board.
2. The IF frequency range supported by the IF Amplifier is from 70 to 400 MHz. The exact IF frequency range supported for a specific RF frequency can be calculated as  $F_{IF} = ABS(F_{LO} - F_{RF})$  where  $F_{LO}$  is inside the specified LO frequency range.
3. Guaranteed by design and characterization
4.  $R_{Fin} = 0$  dBm/tone, RF tone spacing = 5 MHz
5. Guaranteed by design

**Table 7. Pin diode attenuator driver (dual output current DAC) electrical characteristics**

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
R	Resolution	-	-	10	-	Bit
DNL	Differential non linearity	-	-0.05	-	0.05	LSB
INL	Integral non linearity	-	-0.45	-	0.45	LSB
$I_{FS}$	Full Scale current <sup>(1)</sup>	-	0.28	-	2.8	mA
-	Current Mismatch	-	-	-	2	%
-	Output voltage compliance range	-	0	-	3	V
$V_{R_{EXT\_DAC}}$	Voltage Reference	-	-	1.19	-	V
$R_{EXT\_DAC}$	REXT DAC Range	-	10	-	100	k $\Omega$
$I_{cc\_static}$	Static current consumption	(Iout = 0 mA; pin 1)	-	2.5	-	mA

1. See relationship between IDAC and  $R_{EXT\_DAC}$  in the Circuit Description section (Dual Output Current DAC)

Table 8. Integer-N synthesizer electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCO dividers						
N	VCO Divider Ratio (N)	Prescaler 16/17	256	-	65551	-
		Prescaler 19/20	361	-	77836	-
Reference clock and phase frequency detector						
F <sub>ref</sub>	Reference input frequency	-	10	19.2	200	MHz
-	Reference input sensitivity	-	0.35	1	1.5	V <sub>peak</sub>
R	Reference Divider Ratio	-	2	-	1023	
F <sub>PFD</sub>	PFD input frequency	-	-	-	16	MHz
F <sub>STEP</sub>	Frequency step <sup>(1)</sup>	Prescaler 16/17	F <sub>LO</sub> /65551	-	F <sub>LO</sub> /256	Hz
		Prescaler 19/20	F <sub>LO</sub> /77836	-	F <sub>LO</sub> /361	Hz
Charge pump						
I <sub>CP</sub>	ICP sink/source <sup>(2)</sup>	3bit programmable	-	-	5	mA
V <sub>OCP</sub>	Output voltage compliance range	-	0.4	-	V <sub>dd</sub> -0.3	V
-	Spurious <sup>(3)</sup>	-	-	-70	-	dBc
VCOs						
K <sub>VCOA</sub>	VCOA sensitivity	Higher frequency range	-	85	-	MHz/V
		Intermediate frequency range	-	75	-	MHz/V
		Lower frequency range	-	65	-	MHz/V
K <sub>VCOB</sub>	VCOB sensitivity	Higher frequency range	-	85	-	MHz/V
		Intermediate frequency range	-	70	-	MHz/V
		Lower frequency range	-	60	-	MHz/V
ΔT <sub>LKA</sub>	VCOA Maximum Temperature variation for continuous lock <sup>(4)</sup>	CALTYPE [0]	-	-	100	°C
		CALTYPE [1]	-	-	125	°C
ΔT <sub>LKB</sub>	VCOB Maximum Temperature variation for continuous lock <sup>(4)</sup>	CALTYPE [0]	-	-	125	°C
		CALTYPE [1]	-	-	125	°C
-	VCO A Pushing	-	-	8	-	MHz/V
	VCO B Pushing	-	-	14	-	MHz/V
V <sub>CTRL</sub>	VCO control voltage	-	0.4		V <sub>dd</sub> -0.3	V
-	LO Harmonic Spurious	-	-		-20	dBc
I <sub>VCO</sub>	VCO and VCO buffer current consumption	Amplitude [11] (pin 4)	-	35	-	mA
IDIV <sub>2</sub>	DIVIDER by 2 consumption	(pin 3)	-	20	-	mA



Table 8. Integer-N synthesizer electrical characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>2 x LO output buffer (test purpose only)</b>						
F <sub>OUT</sub>	Frequency range	-	4.4	-	5.1	GHz
P <sub>OUT</sub>	Output level	-	-	0	-	dBm
RL	Return Loss	Matched to 50 ohm	-	10	-	dB
I <sub>2LOBUF</sub>	Current Consumption	(pin 15, 16, 17)	-	35	-	mA
<b>LO output buffer</b>						
F <sub>OUT</sub>	Frequency range	-	2.2	-	3	GHz
P <sub>OUT</sub>	Output level	-	-	0	-	dBm
RL	Return Loss	Matched to 50ohm	-	10	-	dB
I <sub>LOBUF</sub>	Current Consumption	(pin 15, 16, 17)	-	30	-	mA
<b>External VCO (LO) buffer</b>						
f <sub>IN VCO</sub>	Frequency range	-	2.2	-	3	GHz
P <sub>IN</sub>	Input level	-	-	0	-	dBm
I <sub>EXTBUF</sub>	Current Consumption	External VCO Buffer (pin 4)	-	25	-	mA
<b>PLL miscellaneous</b>						
I <sub>PLL</sub>	PLL Current Consumption	Input Buffer, Prescaler, Digital Dividers, misc. (pin 24)	-	8	-	mA
I <sub>PRE</sub>	Prescaler input buffer Current Consumption	(pin 12)	-	3	-	mA
I <sub>CP</sub>	Charge Pump Current Consumption	CPSEL=[111], REXT_CP = 4.7 kΩ (pin 21)	-	4	-	mA
t <sub>LOCK</sub>	Lock up time <sup>(5)</sup>	25 kHz PLL bandwidth; within 1ppm of frequency error	-	150	-	μs

1. The frequency step is related to the PFD input frequency as follows:  $F_{STEP}=F_{PFD}/2$
2. See relationship between I<sub>CP</sub> and R<sub>EXT\_CP</sub> in the Circuit Description section (Charge Pump)
3. The level of spurs may change depending on PFD frequency, Charge Pump current, selected channel and PLL loop BW.
4. When setting a specified output frequency, the VCO calibration procedure must be run first in order to select the best subrange for the VCO covering the desired frequency. Once programmed at the initial temperature T<sub>0</sub> inside the operating temperature range (-40 °C to +85 °C), the synthesizer is able to maintain the lock status if the temperature drift (in either direction) is within the limit specified by ΔT<sub>LK</sub>, provided that the final temperature T<sub>1</sub> is still inside the nominal range.
5. Frequency jump from 2450 to 2300 MHz; it includes the time required by the VCO calibration procedure (7 x F<sub>PFD</sub> cycles = 17.5 μs with F<sub>PFD</sub> = 400 kHz)

**Table 9. Phase noise performance<sup>(1)</sup>**

Parameters	Conditions	Min.	Typ.	Max.	Unit
In band phase noise floor, closed loop <sup>(2)</sup>					
Normalized In Band Phase Noise Floor (LO)	I <sub>CP</sub> =4 mA, PLL BW = 50 kHz (including reference clock contribution)	-	-224	-	dBc/Hz
In Band Phase Noise Floor (LO) VCOA divided by 2		-230+20log(N)+10log(F <sub>PFD</sub> )			dBc/Hz
In Band Phase Noise Floor (LO) VCOB direct		-224+20log(N)+10log(F <sub>PFD</sub> )			
PLL integrated phase noise					
Integrated Phase Noise (single sided) 100 Hz to 40 MHz	F <sub>LO</sub> =2.200 GHz, F <sub>STEP</sub> =200 kHz, I <sub>CP</sub> =3 mA, PLL BW = 25 kHz	-	-44.9	-	dBc
		-	0.46	-	° rms
LOA (2200 MHz to 2550 MHz) – open loop					
Phase Noise @ 1 kHz	-	-	-63	-	dBc/Hz
Phase Noise @ 10 kHz	-	-	-89	-	dBc/Hz
Phase Noise @ 100 kHz	-	-	-113	-	dBc/Hz
Phase Noise @ 1 MHz	-	-	-134	-	dBc/Hz
Phase Noise @ 10 MHz	-	-	-151	-	dBc/Hz
Phase Noise Floor @ 40 MHz	-	-	-155	-	dBc/Hz
LOB (2500 MHz to 3000 MHz) – open loop					
Phase Noise @ 1 kHz	-	-	-64	-	dBc/Hz
Phase Noise @ 10 kHz	-	-	-91	-	dBc/Hz
Phase Noise @ 100 kHz	-	-	-113	-	dBc/Hz
Phase Noise @ 1 MHz	-	-	-134	-	dBc/Hz
Phase Noise @ 10 MHz	-	-	-153	-	dBc/Hz
Phase Noise Floor @ 40 MHz	-	-	-162	-	dBc/Hz

1. Phase Noise SSB. VCO amplitude set to maximum value [11]. All the closed-loop performances are specified using a Reference Clock signal at 76.8 MHz with phase noise of -144 dBc/Hz @ 1 kHz offset, -157 dBc/Hz @ 10 kHz offset and -168 dBc/Hz of noise floor.
2. Normalized PN = Measured LO PN –  $20\log(N)$  –  $10\log(F_{PFD})$  where N is the VCO divider ratio ( $N=B \cdot P+A$ ) and  $F_{PFD}$  is the comparison frequency at the PFD input

## 7 Typical performance characteristics

Note:  $V_{\text{supply digital}} = 3.3 \text{ V}$ ,  $V_{\text{supply analog1}} = 3.3 \text{ V}$ ,  $V_{\text{supply analog2}} = 5 \text{ V}$ ,  $F_{\text{IF}} = 150 \text{ MHz}$ ,  $T_A = +25^\circ\text{C}$ , RF power = 0 dBm, unless otherwise specified.

Figure 3. Conversion gain against RF frequency

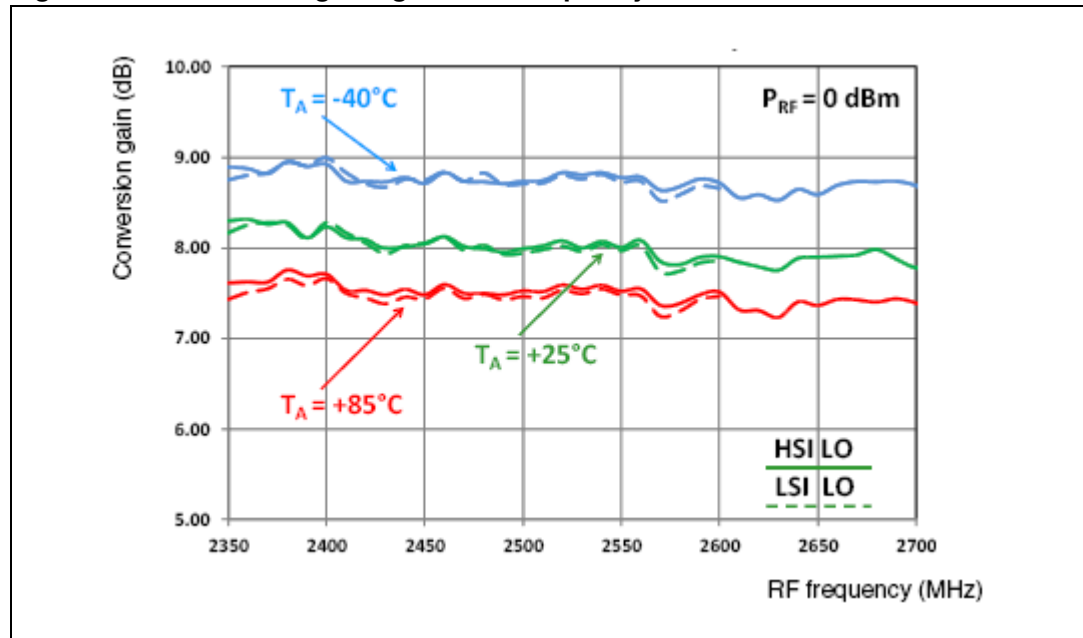


Figure 4. Noise figure against RF frequency

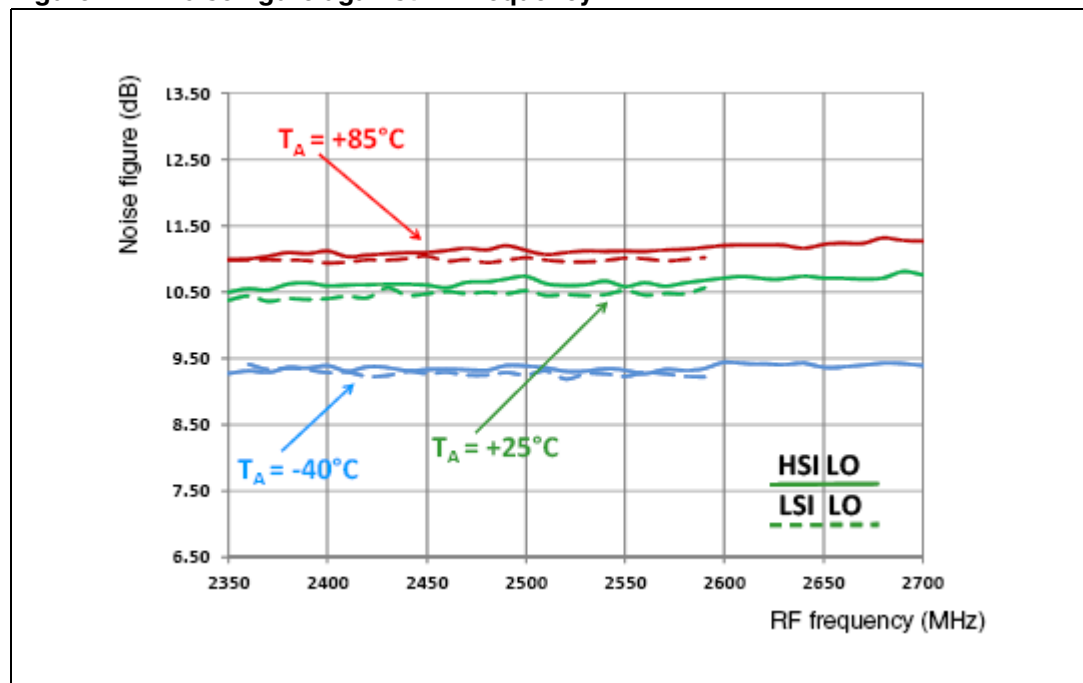


Figure 5. IIP3 against RF frequency

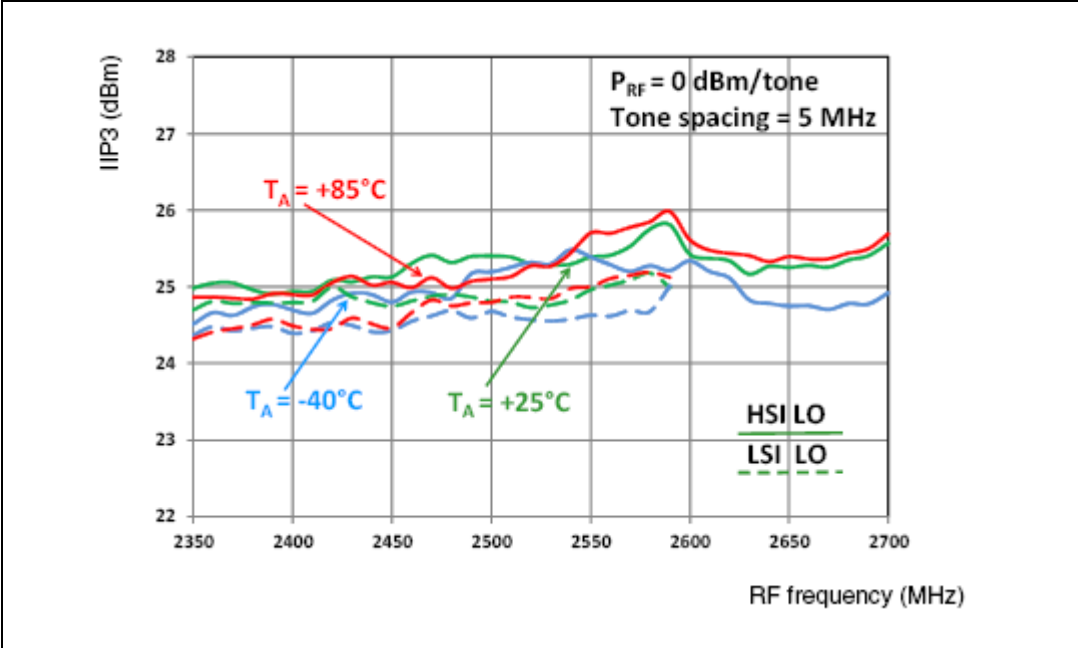


Figure 6. 2RF-2LO response against RF frequency

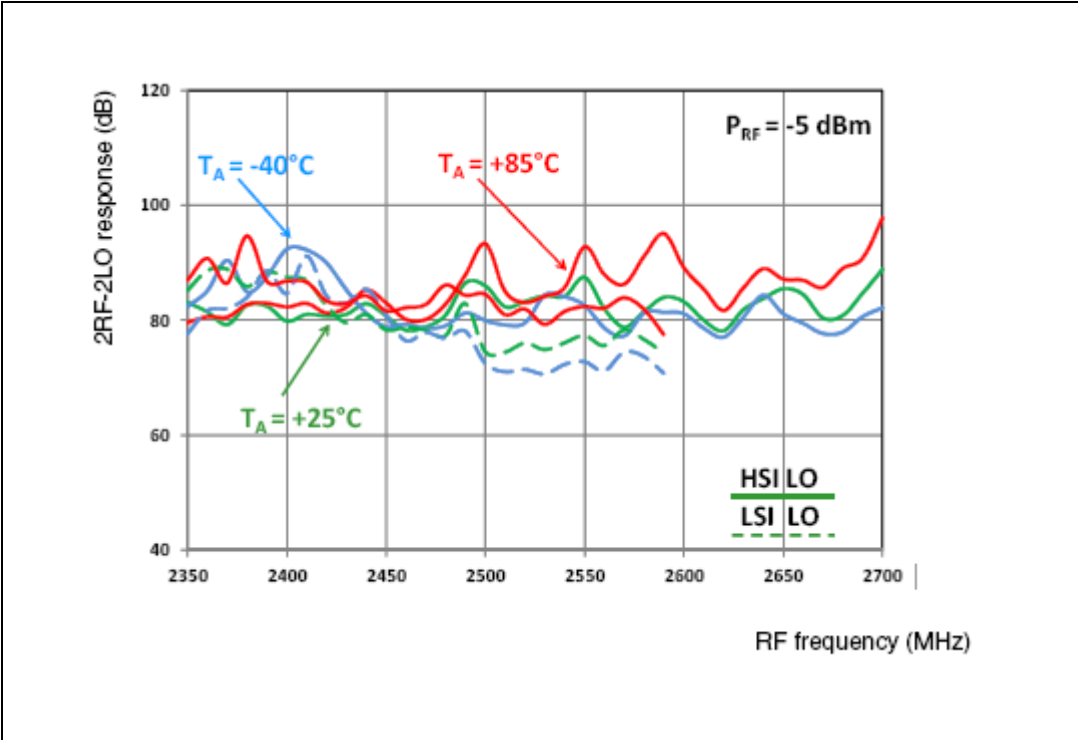


Figure 7. LOA (VCOA div. by 2) closed-loop phase noise at 2.38 GHz,  
( $F_{STEP} = 200$  kHz, ICP = 3 mA)

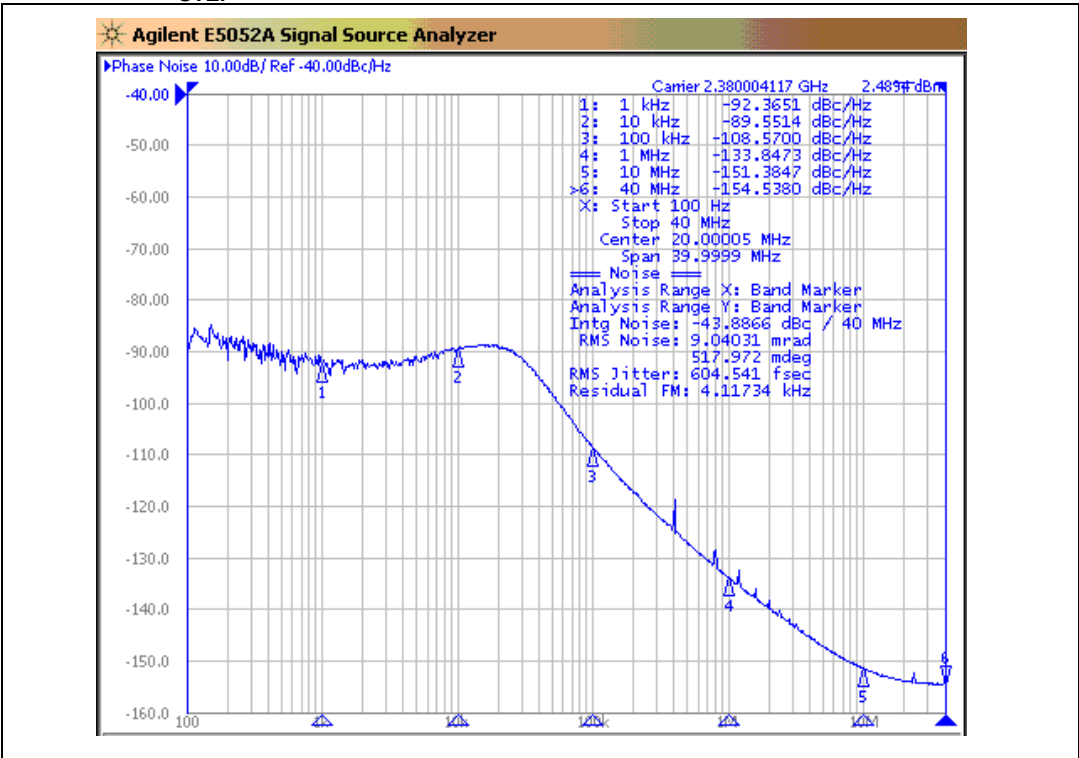
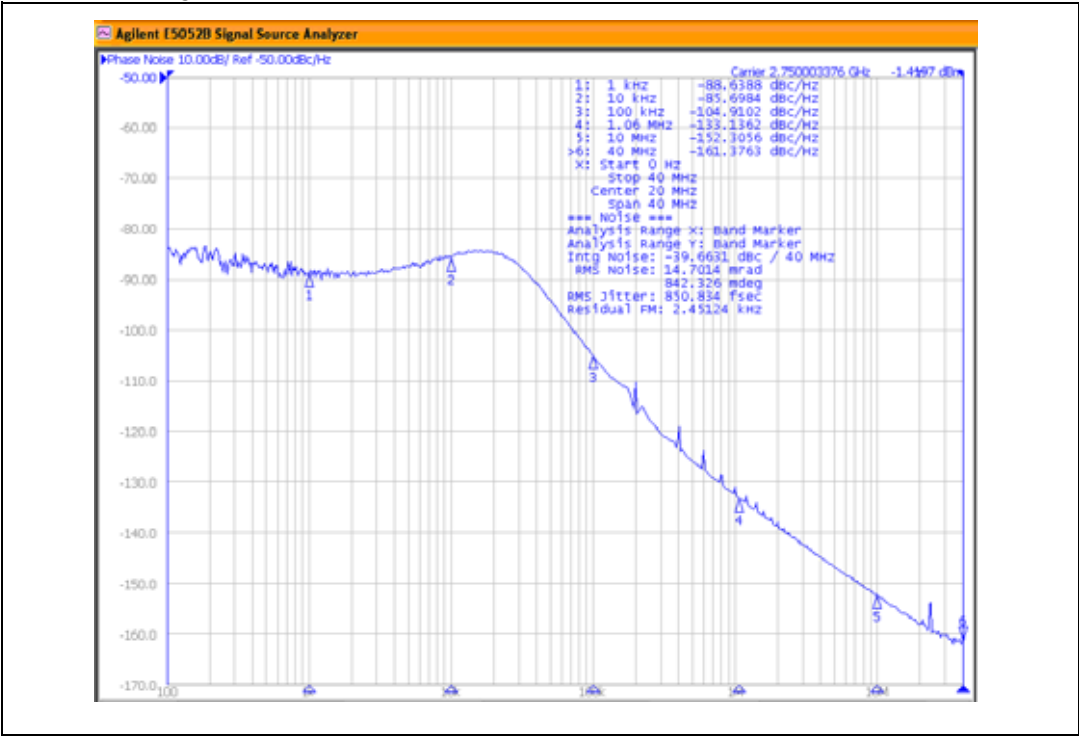


Figure 8. LOB (VCOB div. by 2) closed-loop phase noise at 2.75 GHz,  
( $F_{STEP} = 200$  kHz, ICP = 3 mA)



## 8 General description

The STW82103B (see [Figure 1: STW82103B block diagram on page 7](#)) consists of a high linearity passive CMOS mixer with integrated RF balun, an IF amplifier, a 10-bit current steering DAC with dual output, and an integrated integer-N synthesizer.

The synthesizer embeds 2 internal low-noise VCOs with buffer blocks, a divider by 2, a low noise PFD (Phase Frequency Detector), a precise charge pump, a 10-bit programmable reference divider, two programmable counters and a dual-modulus prescaler. The A-counter (5 bits) and B counter (12 bits) counters, in conjunction with the dual modulus prescaler  $P/P+1$  (16/17 or 19/20), implement an N integer divider, where  $N = B \cdot P + A$ .

The device is controlled through a digital interface ([I2C bus interface](#) or [SPI digital interface](#)).

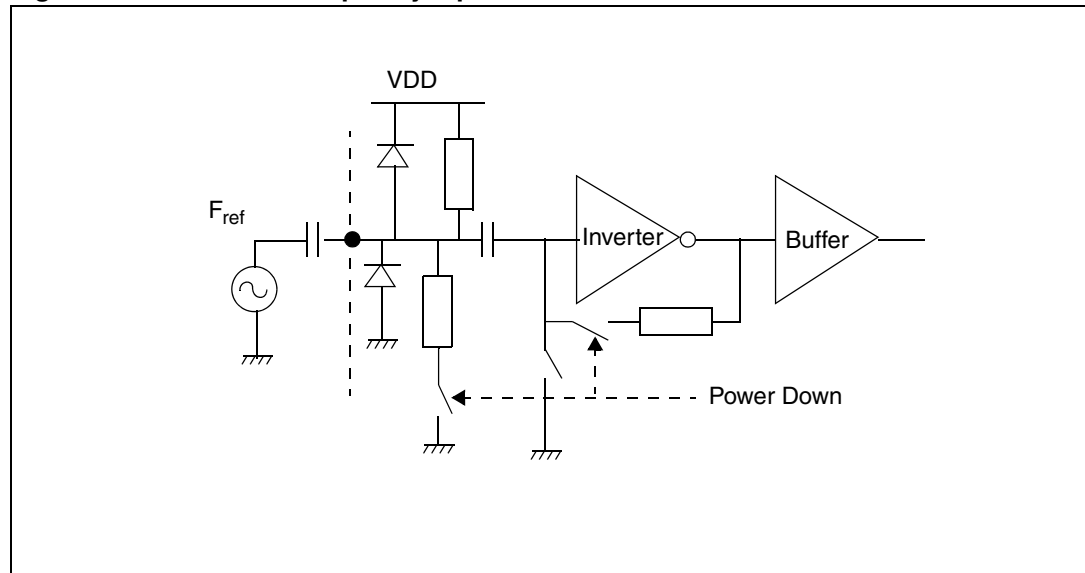
All internal devices operate with a power supply of 3.3 V except for the IF Amplifier output stage and the mixer driver stage operating at 5 V power supply in order to maximize the linearity performance. If the application requires a reduced linearity and noise figure performance the device is programmed in a low-current mode by using the minimum LO amplitude and the minimum biasing current in the IF amplifier. In low-current mode operation the device can use only the 3.3 V power supply thus dissipating less power.

### 8.1 Circuit description

#### 8.1.1 Reference input stage

The reference input stage is shown in [Figure 9](#). The resistor network feeds a DC bias at the  $F_{ref}$  input while the inverter used as the frequency reference buffer is AC coupled.

**Figure 9. Reference frequency input buffer**



### 8.1.2 Reference divider

The 10-bit programmable reference counter allows the input reference frequency to be divided to produce the input clock to the PFD. The division ratio is programmed through the digital interface.

### 8.1.3 Prescaler

The dual-modulus prescaler  $P/P+1$  takes the CML clock from the VCO buffer and divides it down to a manageable frequency for the CMOS A and B counters. The modulus (P) is programmable and can be set to 16 or 19. It is based on a synchronous 4/5 core which division ratio depends on the state of the modulus input.

### 8.1.4 A and B counters

The A (5 bits) and B (12 bits) counters, in conjunction with the selected dual modulus (16/17 or 19/20) prescaler make it possible to generate output frequencies which are spaced only by the reference frequency divided by the reference division ratio. Thus, the division ratio and the VCO output frequency are given by the following formulae:

$$N = B \times P + A$$

$$F_{VCO} = \frac{(B \times P + A) \times F_{ref}}{R}$$

where:

$F_{VCO}$ : VCO output frequency.

P: modulus of dual modulus prescaler (16 or 19 selected through the digital interface).

B: division ratio of the main counter.

A: division ratio of the swallow counter.

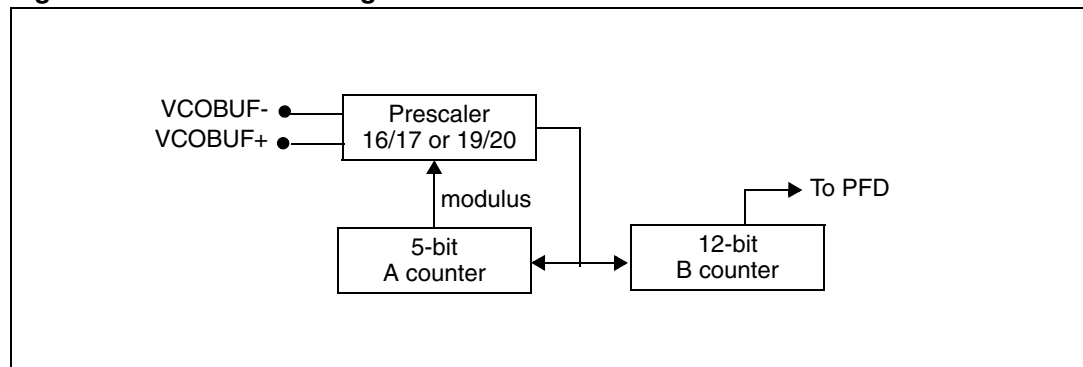
$F_{ref}$ : input reference frequency.

R: division ratio of the reference counter.

N: division ratio of the PLL

The following points should be noted:

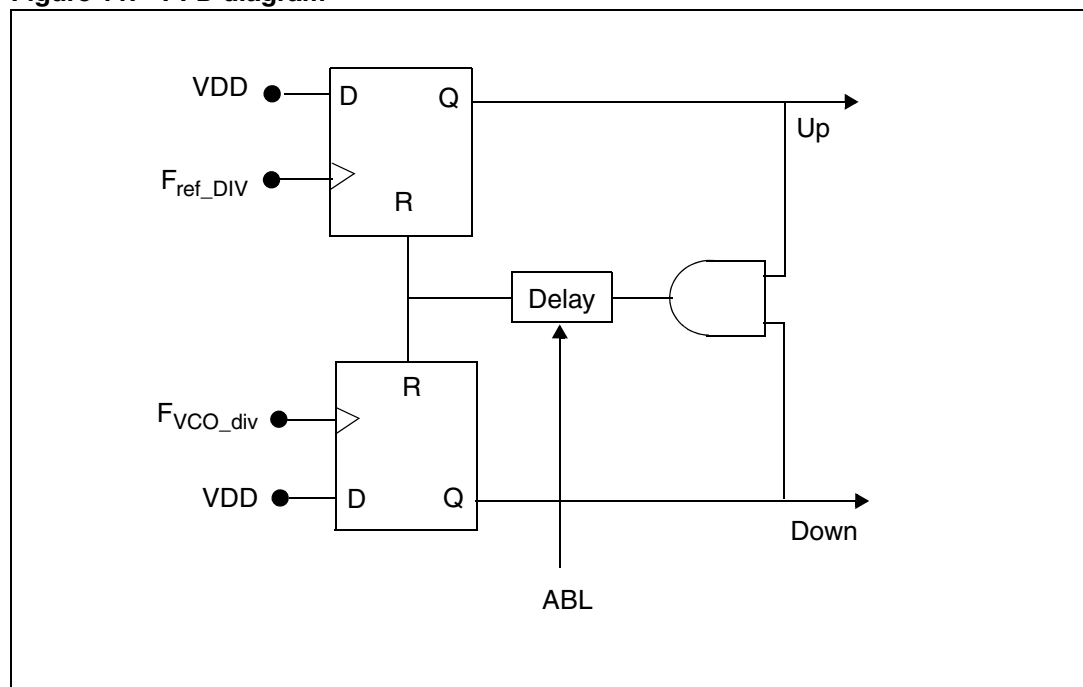
- For the VCO divider to work correctly, B **must** be higher than A.
- A can take any value from 0 to 31.
- Two PLL division ratio (N) ranges are possible, depending on the value of P:
  - 256 to 65551 (when P=16)
  - 361 to 77836 (when P=19).

**Figure 10. VCO divider diagram**

### 8.1.5 Phase frequency detector (PFD)

The PFD takes inputs from the reference and the VCO dividers and produces an output proportional to the phase error. The PFD includes a delay gate that controls the width of the anti-backlash pulse. This pulse ensures that there is no dead zone in the PFD transfer function.

*Figure 11* is a simplified schematic of the PFD.

**Figure 11. PFD diagram**



### 8.1.6 Lock detect

This signal indicates that the difference between rising edges of both UP and DOWN PFD signals is found to be shorter than the fixed delay (roughly 5 ns). The Lock Detect signal is high when the PLL is locked. The Lock Detector consumes current only during PLL transients.

### 8.1.7 Mute until lock

This (software controlled) function shuts down the following elements until the PLL achieves the lock status:

- RF output stage
- LO output buffer
- mixer
- IF amplifier circuitry

Under this setting there is no signal at the IF output stage or the LO output during a frequency jump.

### 8.1.8 Charge pump

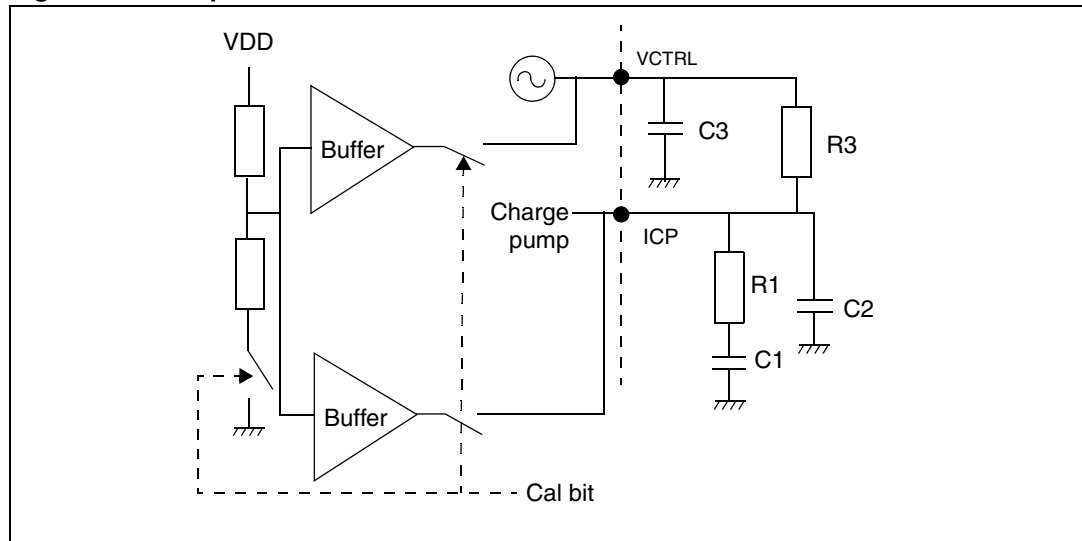
This block drives two matched current sources,  $I_{up}$  and  $I_{down}$ , which are controlled respectively by the UP and DOWN PFD outputs. The nominal value of the output current is controlled by an external resistor (to be connected to the REXT input pin) and the selection of one of 8 possible values by a 3-bit word.

The minimum value of the output current is:  $I_{MIN} = 2 \cdot V_{BG} / R_{EXT\_CP}$  ( $V_{BG} \sim 1.17$  V)

**Table 10. Current values for CPSEL[2:0] selection**

CPSEL2	CPSEL1	CPSEL0	Current	Value for REXT=4.7 kΩ
0	0	0	$I_{MIN}$	0.5 mA
0	0	1	$2 \cdot I_{MIN}$	1.00 mA
0	1	0	$3 \cdot I_{MIN}$	1.50 mA
0	1	1	$4 \cdot I_{MIN}$	2.00 mA
1	0	0	$5 \cdot I_{MIN}$	2.50 mA
1	0	1	$6 \cdot I_{MIN}$	3.00 mA
1	1	0	$7 \cdot I_{MIN}$	3.50 mA
1	1	1	$8 \cdot I_{MIN}$	4.00 mA

*Note:* The current is output on pin ICP. During the VCO auto calibration, ICP and VCTRL pins are forced to VDD/2.

**Figure 12. Loop filter connection**

### 8.1.9 Voltage controlled oscillators

#### VCO selection

Within the STW82103B two low-noise VCOs are integrated to cover a wide band from 2200 MHz to 2550 MHz after the division by 2, and from 2500 MHz to 3000 MHz:

- VCO A frequency range is 4400 MHz to 5100 MHz
- VCO B frequency range is 2500 MHz to 3000 MHz

#### VCO frequency calibration

Both VCOs can operate on 32 frequency ranges that are selected by adding or subtracting capacitors to the resonator. These frequency ranges are intended to cover the wide band of operation and compensate for process variations on the VCO center frequency.

An automatic range selection is performed when the bit SERCAL rises from '0' to '1'. The charge pump is inhibited and the pins ICP and VCTRL are set at a fixed calibration voltage (VCAL). The frequency ranges are then tested to select the nearest one to the desired output frequency ( $F_{OUT} = N \cdot F_{ref} / R$ ) with VCAL input voltage applied. After this selection, the charge pump is once again enabled and the PLL performs a fine adjustment around VCAL on the loop filter voltage to lock  $F_{OUT}$ , thus enabling a fast settling time.

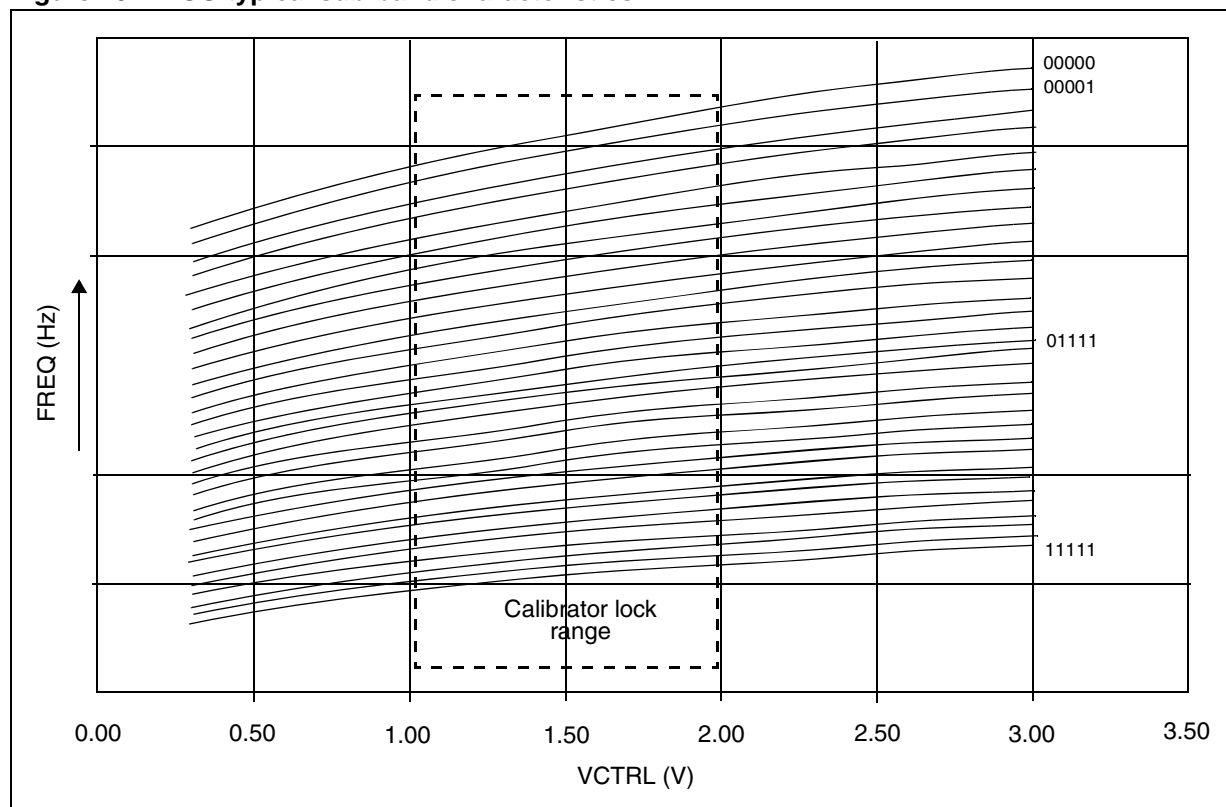
Two calibration algorithms are selectable by setting the CALTYPE bit.

Setting the CALTYPE bit to '1' guarantees the PLL lock versus temperature variations. Once programmed at the initial temperature,  $T_0$ , within the operating temperature range (-40 °C to +85 °C), the synthesizer is able to maintain the lock status if the temperature drift (in either direction) is within the limit specified by  $\Delta T_{LK}$ , and provided that the final temperature,  $T_1$ , is still inside the nominal range.

Setting the CALTYPE bit to '0' fixes VCAL to the mid point of the charge pump output ( $VDD/2$ ). Optimum PLL phase noise performance versus temperature variations with a reduced  $\Delta T_{LK}$  is guaranteed in this case.

The  $\Delta T_{LK}$  parameter, specific to each VCO and calibration type, in the STW82103B is specified in [Table 8: Integer-N synthesizer electrical characteristics](#).

Figure 13. VCO typical sub-band characteristics



The SERCAL bit should be set to '1' at each division ratio change. The calibration takes approximately 7 periods of the Comparison Frequency and the SERCAL bit is automatically reset to '0' at the end of each calibration.

The maximum allowed  $F_{PFD}$  to perform the calibration process is 1 MHz. If a higher  $F_{PFD}$  is used the following procedure should be adopted:

1. Calibrate the VCO at the desired frequency with an  $F_{PFD}$  lower than 1 MHz
2. Set the A, B and R dividers ratio for the desired  $F_{PFD}$

For calibration details refer to [Section 9.4.1: VCO calibration procedure \(I<sup>2</sup>C interface\)](#) or [Section 10.4.1: VCO calibration procedure \(SPI interface\)](#).

**VCO calibration auto-restart feature**

The VCO Calibration Auto-Restart feature, once activated, allows the calibration procedure to be restarted when the Lock Detector reports that the PLL has moved to an unlock condition (trigger on '1' to '0' transition of Lock Detector signal).

This situation could happen if the device experiences a significant temperature variation and the CALTYPE bit is set for optimum PLL phase noise performance (CALTYPE [0]). By enabling the VCO Calibration Auto-Restart feature (through the AUTO\_CAL bit), the device re-selects the proper VCO frequency sub-range, without any external user command.

This feature can be enabled only when the FPF is lower than 1 MHz.

**VCO voltage amplitude control**

The voltage swing of the VCOs can be adjusted over 4 levels by means of two dedicated programming bits (PLL\_A1 and PLL\_A0). This setting trades current consumption with phase noise performances of the VCO. Higher amplitudes provide best phase noise while lower ones save power.

[Table 11](#) and [Table 12](#) give the current consumption and the phase noise at 1 MHz.

**Table 11. VCOA performance against amplitude setting (frequency = 4.6 GHz)**

PLL_A[1:0]	Current Consumption (mA)	PN @ 1 MHz
00	23	-124
01	24	-125
10	32	-127
11	35	-128

**Table 12. VCOB performance against amplitude setting (frequency = 2.8 GHz)**

PLL_A[1:0]	Current Consumption (mA)	PN @ 1 MHz
00	16	-129
01	18	-131
10	27	-133
11	30	-134

### 8.1.10 Output stage

The differential output signal of the synthesizer after the Divider by 2 for VCOA and directly for VCOB is available on pins 16 and 17.

The output stage is selected by programming the PD[4:0] bits.

The output stage is an open-collector structure which is able to meet different requirements over the desired output frequency range by proper connections on the PCB. See [Figure 27: Diversity mode operation with same LO frequencies](#).

### 8.1.11 External VCO buffer

Although the STW82103B includes two wideband and low-noise VCOs, external VCO use capability is also provided.

The external VCO buffer can be used to manage a signal coming from an external VCO in order to build a local oscillator signal by using the STW82103B internal synthesizer as a PLL. This is only possible when External VCO standard mode or External VCO diversity master mode operation are selected. See [Figure 29: External VCO standard mode operation](#) and [Figure 30: External VCO diversity mode operation with same LO](#).

If the STW82103B is operated in Diversity slave mode, the external VCO buffer manage the signal coming from the synthesizer output stage of another STW82103B device. See [Figure 27: Diversity mode operation with same LO frequencies](#) and [Figure 30: External VCO diversity mode operation with same LO](#).

The selection of the external VCO buffer is done by setting the PD[4:0] bits.

The external VCO signal can range from 2200 MHz to 3000 MHz and its minimum power level must be -10 dBm.

## 8.1.12 Mixer and IF amplifier

### LO mixer driver

The LO signal is fed through a driver in order to achieve the high power level needed to drive the passive mixer for maximum performance of linearity and NF.

The LO Mixer Driver is coupled to the mixer with an integrated LO balun. The LO signal level is adjusted by means of an Automatic Level Control loop (ALC) controlled by the bits LO\_A[1:0].

In low current mode the configuration LO\_A[1:0]='00' (minimum LO amplitude) should be selected and the power supply on pin 40 can be set to 3.3 V.

The LO balun resonating frequency can be adjusted by means of the bits CAP[2:0] in order to match the selected LO frequency.

**Table 13. Suggested CAP[2:0] values for LO Frequency range mixer**

CAP[2:0]	LO frequency range
000	2875 MHz ÷ 3000MHz
001	2750 MHz ÷ 2875 MHz
010	2640 MHz ÷ 2750 MHz
011	2530 MHz ÷ 2640 MHz
100	2435 MHz ÷ 2530 MHz
101	2350 MHz ÷ 2435 MHz
110	2280 MHz ÷ 2350 MHz
111	2200 MHz ÷ 2280 MHz

### Mixer

A doubly balanced CMOS passive mixer is internally driven by the high level LO signal in order to achieve high linearity and low noise performance.

The RF integrated balun permits the removal of external components and it is internally matched to 50 ohms.

The gate bias of the CMOS devices in the mixer is programmable with 4 bits (MIX[3:0]) to optimize the input matching and the gain of the signal chain.

Higher values of gate bias (higher decimal values of MIX[3:0]) are suggested to maximize linearity and lower values to maximize the performance of Gain and NF.

### IF amplifier

The integrated IF stage permits a 200-ohm load to be driven (typically a SAW filter) ensuring high linearity.

It is an open collector stage (pin 31, 32) and should be biased to 5 V with choke inductors. The typical output impedance is 200 ohms. The linearity performances are controlled by the bits IFAMP[1:0]. In low current mode the configuration IFAMP[1:0]='00' (minimum linearity) should be selected and the open collector stage can be biased to 3.3 V with choke inductors.

**Table 14. Linearity performance against IFAMP[1:0] configuration (typical condition)**

IFAMP[1:0]	Linearity performance
00	19 dB
01	21 dB
10	23 dB
11	25 dB

### 8.1.13 Dual output current DAC

The STW82103B embeds a 10-bit Dual Output steering current DAC especially suited to drive an external PIN diode attenuator. This provides power level calibration capability at the RF input for the TX observation path applications.

The current sourced by the DAC is related to the  $R_{EXT\_DAC}$  resistor according to the following formulae (where  $V_{R_{EXT\_DAC}}$  is approximately 1.19 V):

$$IDAC_{LSB} = \frac{1}{2} \times \frac{3 \times V_{R_{EXT\_DAC}}}{R_{EXT\_DAC}} \times \frac{1}{64} \quad \text{LSB DAC current}$$

$$IDAC_{FS} = \frac{1}{2} \times \frac{3 \times V_{R_{EXT\_DAC}}}{R_{EXT\_DAC}} \times \frac{1023}{64} \quad \text{Full scale current}$$

With a 10 k $\Omega$   $R_{EXT\_DAC}$  the FS current is approximately 2.8 mA.

## 9 I<sup>2</sup>C bus interface

The I<sup>2</sup>C bus interface is selected by hardware connection of the pin 25 (DBUS\_SEL) to 0 V.

Data transmission from a microprocessor to the STW82103B takes place through the 2 wires (SDA and SCL) I<sup>2</sup>C-bus interface. The STW82103B is always a slave device.

The I<sup>2</sup>C-bus protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as receiver. The device that controls the data transfer is known as the master and the others as slaves. The master always initiates the transfer and provides the serial clock for synchronization.

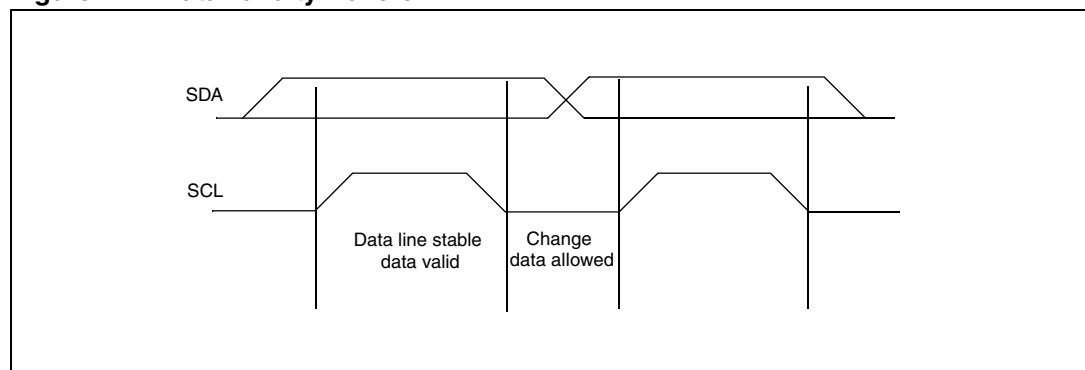
The STW82103B I<sup>2</sup>C bus supports Fast Mode operation (clock frequency up to 1 MHz).

### 9.1 I<sup>2</sup>C general features

#### 9.1.1 Data validity

Data changes on the SDA line must only occur when the SCL is LOW. SDA transitions while the clock is HIGH identify START or STOP conditions.

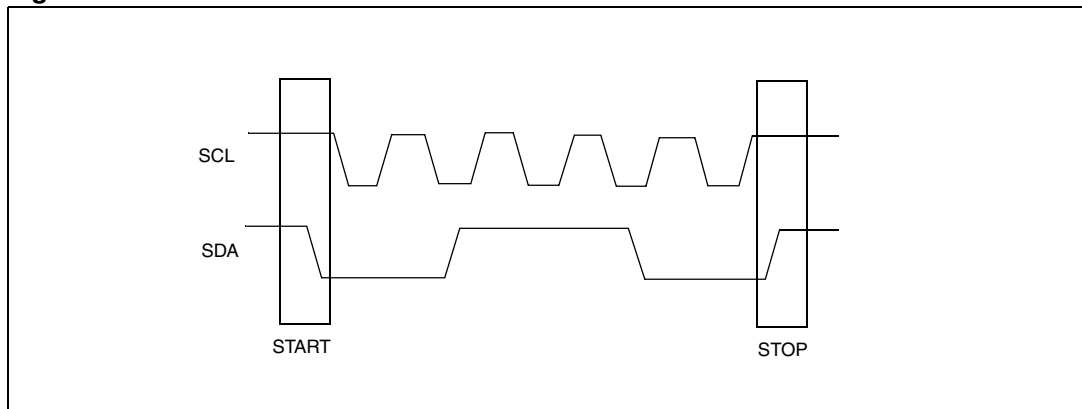
**Figure 14. Data validity waveform**





### 9.1.2 START and STOP conditions

Figure 15. START and STOP condition waveform



#### START condition

A START condition is identified by a HIGH to LOW transition of the data bus SDA while the clock signal SCL is stable in the HIGH state. A Start condition must precede any command for data transfer.

#### STOP condition

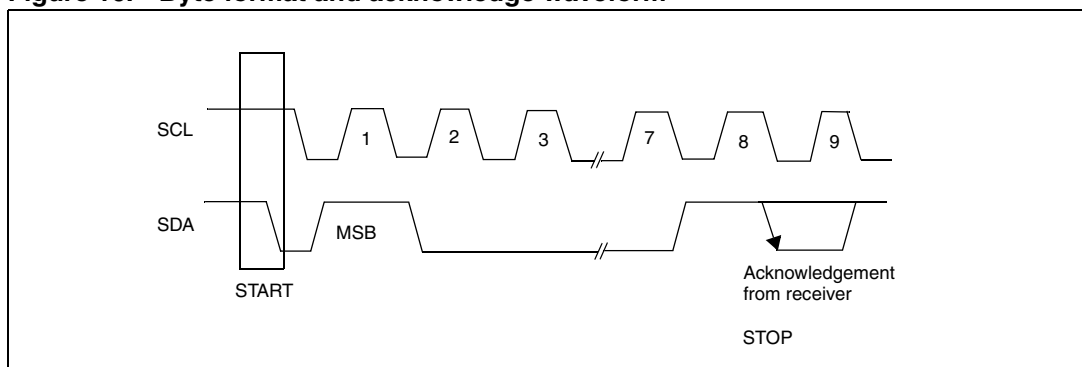
A STOP condition is identified by a transition of the data bus SDA from LOW to HIGH while the clock signal SCL is stable in the HIGH state.. A STOP condition terminates communications between the STW82103B and the Bus Master.

### 9.1.3 Byte format and acknowledge

Every byte (8 bits long) transferred on the SDA line must contain bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

An acknowledge bit indicates a successful data transfer. The transmitter, either master or slave, releases the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA low to acknowledge the receipt of 8 bits of data.

Figure 16. Byte format and acknowledge waveform



### 9.1.4 Device addressing

To start the communication between the Master and the STW82103B, the master must initiate with a START condition. Following this, the master sends onto the SDA line 8 bits (MSB first) corresponding to the device select address and read or write mode.

The first 7 MSBs are the device address identifier, corresponding to the I<sup>2</sup>C-Bus definition. For the STW82103B the address is set as '1101A<sub>2</sub>A<sub>1</sub>A<sub>0</sub>', 3-bits programmable. The 8th bit (LSB) is the read or write operation bit (the RW bit is set to 1 in read mode and to 0 in write mode).

After a START condition the STW82103B identifies the device address on the bus and, if matched, it acknowledge the identification on SDA bus during the 9th clock pulse.

### 9.1.5 Single-byte write mode

Following a START condition the master sends a device select code with the RW bit set to 0. The STW82103B gives an acknowledge and waits for the internal sub-address (1 byte). This byte provides access to any of the internal registers.

After reception of the internal byte sub-address the STW82103B again responds with an acknowledge. A single-byte write to sub-address 0x00 would affect DATA\_OUT[47:40], a single-byte write with sub-address 0x04 would affect DATA\_OUT[15:8] and so on.

S	1101A <sub>2</sub> A <sub>1</sub> A <sub>0</sub>	0	ack	sub-address byte	ack	DATA IN	ack	P
---	--	---	-----	---------------------	-----	---------	-----	---

### 9.1.6 Multi-byte write mode

The multi-byte write mode can start from any internal address. The master sends the data bytes and each one is acknowledged. The master terminates the transfer by generating a STOP condition.

The sub-address determines the starting byte. For example, a multi-byte write with sub-address 0x01 and 4 DATA\_IN bytes affects 4 bytes starting at address 0x01 (registers at addresses 0x01, 0x02, 0x03 and 0x04 are modified).

S	1101A <sub>2</sub> A <sub>1</sub> A <sub>0</sub>	0	ack	sub-address byte	ack	DATA IN	ack	..	DATA IN	ack	P
---	--	---	-----	---------------------	-----	---------	-----	----	------------	-----	---

### 9.1.7 Current byte address read

In the current byte address read mode, following a START condition, the master sends the device address with the RW bit set to 1 (No sub-address is needed as there is only 1 byte read register). The STW82103B acknowledges this and outputs the data byte. The master does not acknowledge the received byte, but terminates the transfer with a STOP condition.

S	1101A <sub>2</sub> A <sub>1</sub> A <sub>0</sub>	1	ack	DATA OUT	No ack	P
---	--	---	-----	----------	--------	---

9.2 I<sup>2</sup>C timing specifications

9.2.1 Data and clock timing specification

Figure 17. I<sup>2</sup>C data and clock waveforms

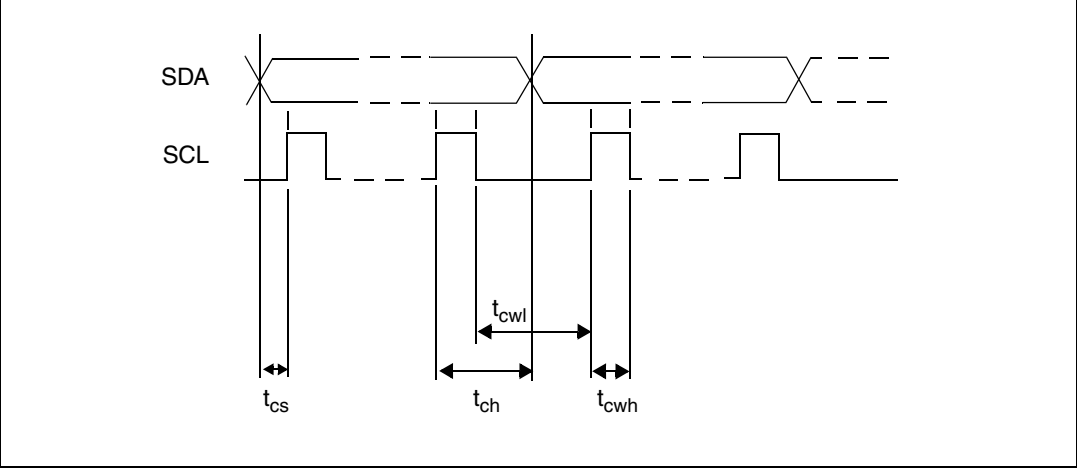


Table 15. I<sup>2</sup>C data and clock timing parameters

Symbol	Parameter	Min	Unit
$T_{cs}$	Data to clock set up time	2	ns
$T_{ch}$	Data to clock hold time	2	
$T_{cwh}$	Clock pulse width high	10	
$T_{cwl}$	Clock pulse width low	5.5	

9.2.2 I<sup>2</sup>C START and STOP timing specification

Figure 18. I<sup>2</sup>C START and STOP timing waveforms

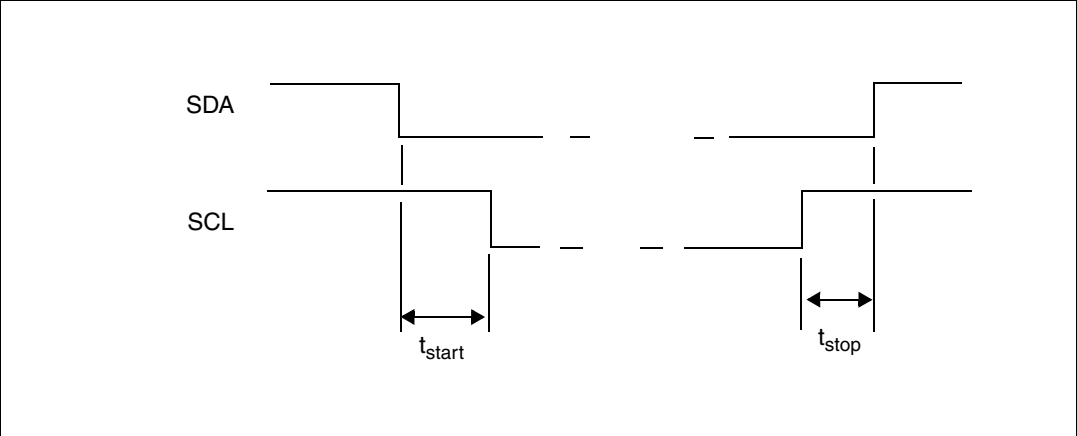


Table 16. I<sup>2</sup>C START and STOP timing parameters

Symbol	Parameter	Min	Unit
T <sub>start</sub>	Clock to data start time	2	ns
T <sub>stop</sub>	Data to clock down stop time	2	

9.2.3 I<sup>2</sup>C acknowledge timing specification

Figure 19. I<sup>2</sup>C acknowledge timing waveforms

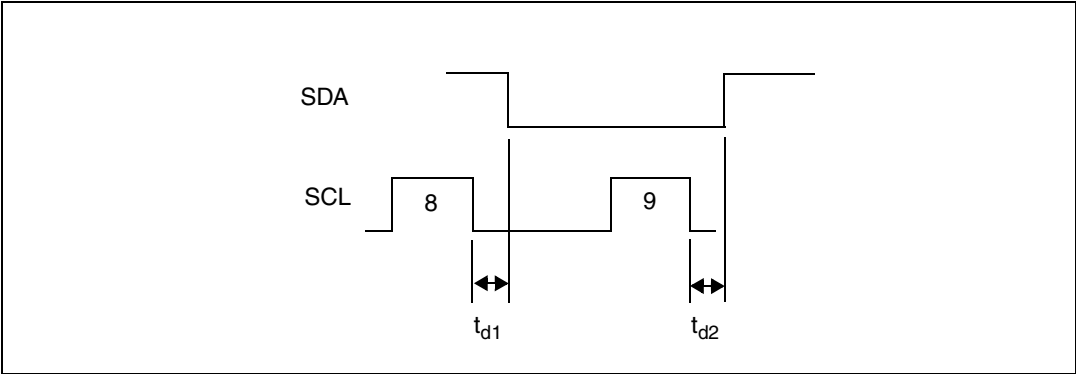


Table 17. I<sup>2</sup>C acknowledge timing parameters

Symbol	Parameter	Max	Unit
T <sub>d1</sub>	Ack begin delay	2	ns
T <sub>d2</sub>	Ack end delay	2	

## 9.3 I<sup>2</sup>C registers

STW82103B has 9 write-only registers and 1 read-only register.

### 9.3.1 I<sup>2</sup>C register summary

The following table gives a short description of the write-only registers list.

**Table 18. I<sup>2</sup>C register list**

Offset	Register name	Description	Page
0x00	FUNCTIONAL_MODE	Functional mode register	<a href="#">on page 39</a>
0x01	B_COUNTER	B counter register	<a href="#">on page 39</a>
0x02	A_COUNTER	A counter register	<a href="#">on page 40</a>
0x03	REF_DIVIDER	Reference clock divider ratio register	<a href="#">on page 40</a>
0x04	CONTROL	PLL control register	<a href="#">on page 41</a>
0x05	MUTE_&_CALIBRATION	Mute and calibration control register	<a href="#">on page 42</a>
0x06	DAC_CONTROL	DAC control register	<a href="#">on page 42</a>
0x07	MIXER_CONTROL	Mixer control register	<a href="#">on page 43</a>
0x08	IFAMP_LO_CONTROL	IF amplifier LO control register	<a href="#">on page 43</a>
0x09	READ_ONLY_REGISTER	Device ID and calibration status register	<a href="#">on page 44</a>

### 9.3.2 I<sup>2</sup>C register definitions

#### FUNCTIONAL\_MODE Functional mode register

7	6	5	4	3	2	1	0
ALC_PD	PKD_EN	PD[4:0]				B11	
W	W	W				W	

**Address:** 0x00

**Type:** W

**Reset:** 0x00

[7] **ALC\_PD**: for test purpose only must be set to '0'. (ALC ON)

[6] **PKD\_EN**: for test purpose only must be set to '0'. (Peak detector output on pin 36 OFF)

[5:1] **PD[4:0]**: bits used to select different functional modes for the STW82103B according to the following table

00000: (0 decimal) Power down mode

00001: (1 decimal) Standard Mode VCOA (VCOA and RX chain ON)

00010: (2 decimal) Standard Mode VCOB (VCOB and RX chain ON)

00011: (3 decimal). Diversity Slave Mode (ExtVCO/LO input buffer and RX Chain ON; internal synthesizer OFF)

00100: (4 decimal) Diversity Master Mode VCOA (VCOA, RX Chain and LO output buffer ON)

00101: (5 decimal) Diversity Master Mode VCOB (VCOB, RX Chain and LO output buffer ON)

00110: (6 decimal) External LO Standard Mode (RX Chain ON; PLL and ExtVCO/LO input buffer ON)

00111: (7 decimal) External LO Diversity Master Mode (RX Chain ON; PLL, ExtVCO/LO input buffer and LO output buffer ON)

[0] **B11**: B counter value (bits B[10:0] in the B\_COUNTER and A\_COUNTER registers)

#### B\_COUNTER B counter register

7	6	5	4	3	2	1	0
B[10:3]							
W							

**Address:** 0x01

**Type:** W

**Reset:** 0x00

**Description:** Most significant bits of the B counter value

[7:0] **B[10:3]**: B counter value (bit B11 in the FUNCTIONAL\_MODE register, bits B[2:0] in the A\_COUNTER register)

A\_COUNTER

A counter register

7	6	5	4	3	2	1	0
B[2:0]			A[4:0]				
W			W				

**Address:** 0x02

**Type:** W

**Reset:** 0x00

**Description:** Least significant bits of the B-counter value. A-counter value.

[7:5] **B[2:0]**: B Counter value (bit B11 in the [FUNCTIONAL\\_MODE](#) register, bits B[10:3] in the [B\\_COUNTER](#) register).

[4:0] **A[4:0]**: A counter value

REF\_DIVIDER

Reference clock divider ratio register

7	6	5	4	3	2	1	0
R[9:2]							
W							

**Address:** 0x03

**Type:** W

**Reset:** 0x00

**Description:** Most significant bits of the reference clock divider ratio value.

[7:0] **R[9:2]**: Reference clock divider ratio (bits R[1:0] in the [CONTROL](#) register)

CONTROL PLL control register

7	6	5	4	3	2	1	0
[R1:0]		PLL_A[1:0]		CPSEL[2:0]		PSC_SEL	
W		W		W		W	

**Address:** 0x04  
**Type:** W  
**Reset:** 0x00  
**Description:** Least significant bits of the reference clock divider ratio value and PLL control bits.

- [7:6] **R[1:0]:** Reference clock divider ratio (bits R[9:2] in the [REF\\_DIVIDER](#) register)  
[5:4] **PLL\_A[1:0]:** VCO amplitude  
[3:1] **CPSEL[2:0]:** Charge Pump output current  
[0] **PSC\_SEL:** Prescaler Modulus select ('0' for P=16, '1' for P=19)

The LO output frequency is programmed by setting the proper value for A, B and R according to the following formula:

$$F_{LO} = D_R \cdot (B \cdot P + A) \cdot \frac{F_{ref}}{R}$$

- Where:
- $D_R$  equals 0.5 for VCOA (VCO output frequency divided by 2) or 1 for VCOB (VCO output frequency)
  - P is the selected Prescaler Modulus



# MUTE\_ &\_ CALIBRATION

## Mute and calibration control register

7	6	5	4	3	2	1	0
CALTYPE	SERCAL	SELEXTCAL	MUTE_EN	MUTE_TYPE	MUTE_LOOUT_EN	MUTE_MIX_EN	MUTE_IFAMP_EN
W	W	W	W	W	W	W	W

**Address:** 0x05  
**Type:** W  
**Reset:** 0x00  
**Description:** For test purposes only

- [7] **CALTYPE:** Calibration algorithm selection  
 0: standard calibration to optimize the phase noise versus temperature  
 1: enhanced calibration to maximize the  $\Delta T_{LK}$  range
- [6] **SERCAL:**  
 1: starts the VCO auto-calibration (automatically reset to '0' at the end of calibration)
- [5] **SELEXTCAL:** test purpose only; must be set to '0'
- [4] **MUTE\_EN:**  
 0: mute function disabled  
 1: mute function enabled
- [3] **MUTE\_TYPE:** must be set to '1' while the mute function is enabled (mute the IF output on Unlock state)
- [2] **MUTE\_LOOUT\_EN:**  
 To be set to '1' to mute the LO output buffer
- [1] **MUTE\_MIX\_EN:**  
 To be set to '1' mute the Mixer circuitry
- [0] **MUTE\_IFAMP\_EN:** To be set to '1' to mute the IF amplifier circuitry

# DAC\_ CONTROL

## DAC control register

7	6	5	4	3	2	1	0
DAC[9:2]							
W							

**Address:** 0x06  
**Type:** W  
**Reset:** 0x00  
**Description:** Most significant bits of the DAC control word

- [7:0] **DAC[9:2]:** DAC input word for DAC current control (bits DAC[1:0] in the [MIXER\\_CONTROL](#) register).

**MIXER\_CONTROL**                      **Mixer control register**

7	6	5	4	3	2	1	0
DAC[1:0]		MIX[3:0]				PD_DAC	CAL_AUTOSTART_EN
W		W				W	W

**Address:** 0x07  
**Type:** W  
**Reset:** 0x00  
**Description:** Least significant bits of DAC control word and mixer control bit fields

- [7:6] **DAC[1:0]**: DAC input word for DAC current control (bits DAC[9:2] in the [DAC\\_CONTROL](#) register)
- [5:2] **MIX[3:0]**: Mixer bias control value
- [1] **PD\_DAC**: DAC power down
- [0] **CAL\_AUTOSTART\_EN**: VCO calibration auto-restart enable ('1' active), permits to automatically restart the VCO calibration procedure in case of PLL unlock

**IFAMP\_LO\_CONTROL**                      **IF amplifier LO control register**

7	6	5	4	3	2	1	0
IFAMP[1:0]		CAP[2:0]			LO_A[1:0]		LPMUX_EN
W		W			W		W

**Address:** 0x08  
**Type:** W  
**Reset:** 0x00

- [7:6] **IFAMP[1:0]**: power consumption/linearity control
- [5:3] **CAP[2:0]**: Tuning capacitors control
- [2:1] **LO\_A[1:0]**: LO amplitude control
- [0] **LPMUX\_EN**: for test purpose only (low power mode for MUX); must be set to '0'

READ-ONLY REGISTER

Device ID and calibration status register

7	6	5	4	3	2	1	0
ID[1:0]		LOCK_DET		INTCAL[4:0]			
R		R		R			

**Address:** 0x09

**Type:** R

**Reset:** 0x00

**Description:** This register is automatically addressed in the ‘current byte address read mode’

- [7:6] **ID[1:0]:** device identification ‘11’ for STW82103B
- [5] **LOCK\_DET:** ‘1’ when PLL is locked
- [4:0] **INTCAL[4:0]:** internal value of the VCO calibration control word

## 9.4 Device calibration through the I<sup>2</sup>C interface

### 9.4.1 VCO calibration procedure (I<sup>2</sup>C interface)

The calibration of the VCO center frequency is activated by setting the SERCAL bit of the MUTE & CALIBRATION register to '1'.

To program the device ensuring a correct VCO calibration, the following procedure is required before every channel change:

1. Program all the Registers using a multi-byte write sequence with the desired setting:
  - Functional Mode
  - B and A counters
  - R counter
  - VCO amplitude
  - Charge Pump
  - Prescaler Modulus
  - DAC
  - Mixer and LO Control
  - all bits of the MUTE & CALIBRATION Register (0x05) set to '0'.
2. Program the MUTE & CALIBRATION register using a single-byte write sequence (sub-address 0x05) with the SERCAL bit set to '1'.

The maximum allowed PFD frequency ( $F_{PFD}$ ) to perform the calibration process is 1 MHz. If the desired  $F_{PFD}$  is higher than 1 MHz the following steps are needed:

3. Perform all the step of the above calibration procedure programming the desired VCO frequency with a proper setting of R, B and A counter so that  $F_{PFD}$  results lower than 1 MHz.
4. Once calibration is completed, program all the Registers by using a multi-byte write sequence (Functional Mode, B and A counters, R counter, VCO amplitude, Charge Pump, Prescaler Modulus, DAC, Mixer and LO Control) with the proper settings for the desired VCO and PFD frequencies.

### 9.4.2 Power ON sequence (I<sup>2</sup>C interface)

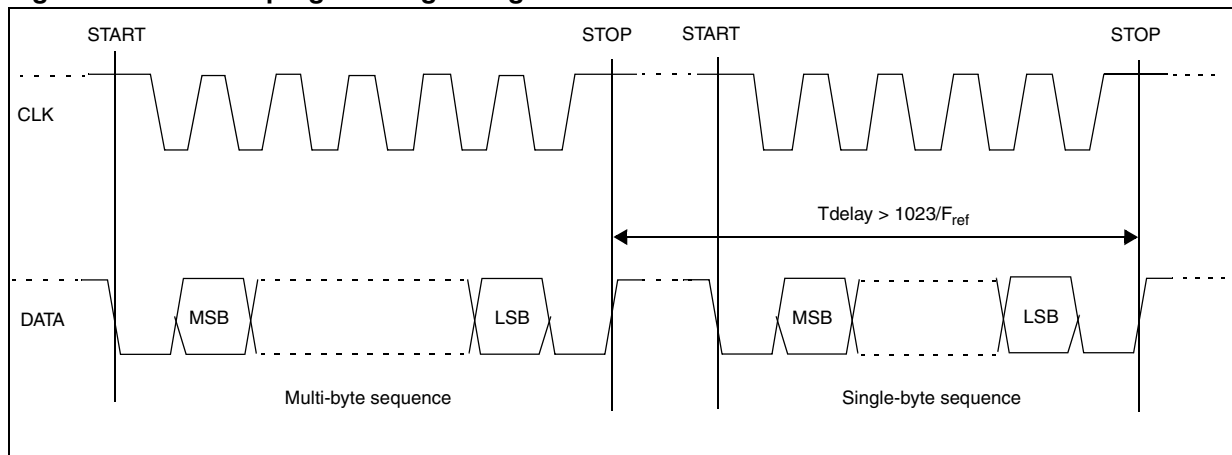
At power-on the device is configured in power-down mode.

In order to guarantee correct setting of the internal circuitry after the power on, the following steps must be followed:

1. Power up the device
2. Provide the Reference clock
3. Implement the first programming sequence with a proper delay time between the STOP condition of the multi-byte write sequence and that of the single-byte write sequence (see [Figure 20](#)). The  $T_{delay}$  value must respect the following condition:

$$T_{delay} > 1023 \times \frac{1}{F_{ref}}$$

$F_{ref}$  is the reference clock frequency.

**Figure 20. I2C first programming timing**

### 9.4.3 VCO calibration auto-restart procedure (I<sup>2</sup>C interface)

The VCO calibration auto-restart feature is enabled in two steps:

1. Set the desired frequency ensuring VCO calibration procedure as described above ([Section 9.4.1](#)).
2. Program the MIXER\_CONTROL register (sub-address 0x07) using a single-byte write sequence with the CAL\_AUTOSTART\_EN bit set to '1' while keeping the others unchanged.

## 10 SPI digital interface

### 10.1 SPI general features

The SPI digital interface is selected by hardware connection of the pin 25 (DBUS\_SEL) to 3.3 V.

The STW82103B IC is programmed by means of a high-speed serial-to-parallel interface with write option only. The 3-wires bus can be clocked at a frequency as high as 100 MHz to allow fast programming of the registers containing the data for RF IC configuration.

The programming of the chip is done through serial words with whole length of 26 bits. The first 2 MSB represent the address of the registers. The others 24 LSB represent the value of the registers.

Each data bit is stored in the internal shift register on the **rising edge** of the CLOCK signal.

On the **rising edge** of the LOAD signal the outputs of the selected register are sent to the device.

**Figure 21. SPI input and output bit order**

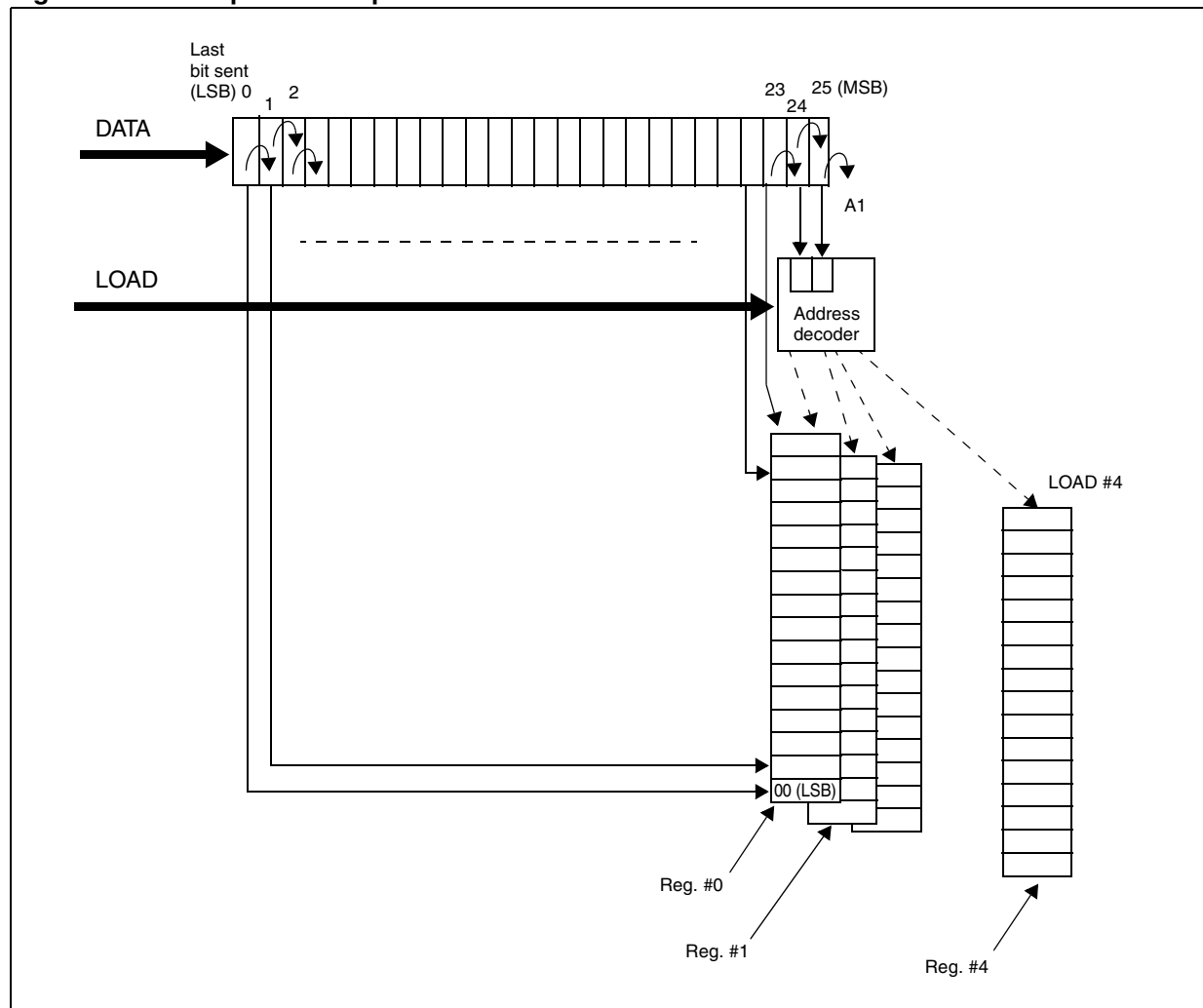


Figure 22. SPI data structure



Table 19. Address decoder and outputs

Address		Outputs			
A1	A0	DATABITS D23-D0	Nº	Name	Function
0	0	24	0	ST1	DAC, Mixer, Tuning capacitors, LO_amplitude
0	1	24	1	ST2	Reference divider, VCO amplitude, VCO Calibration, Charge Pump current, Prescaler Modulus, Mute functions
1	0	24	2	ST3	Functional modes, VCO dividers
1	1	24	3	ST4	Reserved



10.2 SPI timing specification

10.2.1 Data, clock and load timing

Figure 23. SPI timing waveforms

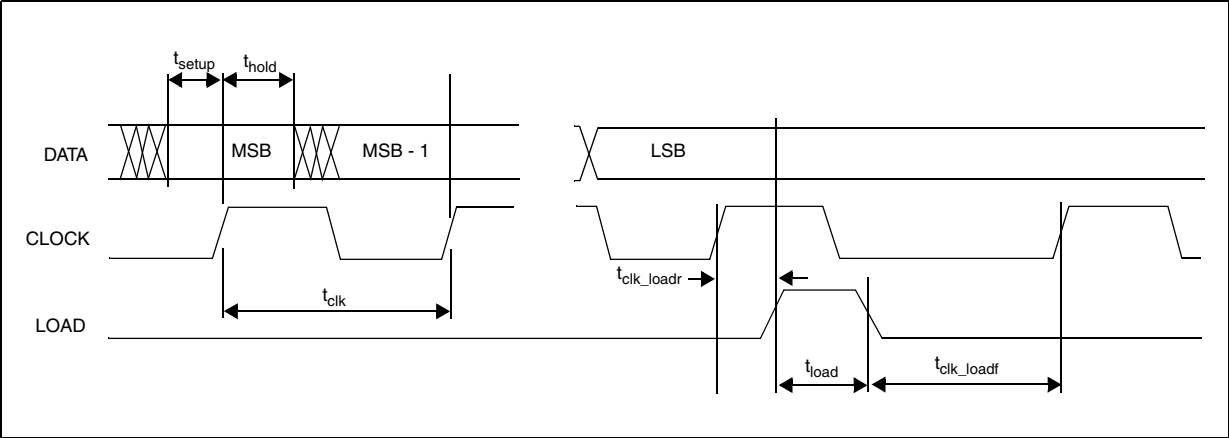


Table 20. SPI timing parameters

Parameter	Description	Min.	Typ.	Max.	Unit
$t_{\text{setup}}$	DATA to CLOCK setup time	1	-	-	ns
$t_{\text{hold}}$	DATA to clock hold time	0.5	-	-	ns
$t_{\text{clk}}$	CLOCK cycle period	10	-	-	ns
$t_{\text{load}}$	LOAD pulse width	3	-	-	ns
$t_{\text{clk\_loadr}}$	CLOCK to LOAD rising edge	0.6	-	-	ns
$t_{\text{clk\_loadf}}$	CLOCK to LOAD falling edge	2.5	-	-	ns



## 10.3 SPI registers

### 10.3.1 SPI register summary

Table 21. SPI register list

Offset	Register name	Description	Page
0x00	ST1	SPI register 1	<a href="#">on page 50</a>
0x01	ST2	SPI register 2	<a href="#">on page 51</a>
0x10	ST3	SPI register 3	<a href="#">on page 52</a>

### 10.3.2 SPI register definitions

#### ST1 SPI register 1

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC[9:0]										MIX[3:0]				PWD_DAC	CAL_AUTOSTART_EN	IF[1:0]		CAP[2:0]		LO_A[1:0]		LPMUX_EN	
W										W	W	W	W	W	W	W	W	W	W	W	W	W	W

**Address:** 0x00

**Type:** W

**Reset:** 0x00

- [23:14] **DAC[9:0]**: DAC input word
- [13:10] **MIX[3:0]**: Mixer bias control
  - [9] **PWD\_DAC**: DAC power down
  - [8] **CAL\_AUTOSTART\_EN**: VCO calibration auto-restart enable
- [7:6] **IF[1:0]**: Power consumption/linearity control
- [5:3] **CAP[2:0]**: Tuning capacitors control
- [2:1] **LO\_A[1:0]**: LO amplitude control
- [0] **LPMUX\_EN**: For test purpose only. Must be set to '0'

## ST2

## SPI register 2

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R[9:0]										PLL_A[1:0]		CPSEL[2:0]			PSC_SEL	CAL_TYPE	SERCAL	SELEXTCAL	MUTE_EN	MUTE_TYPE	MUTE_LOOUT_EN	MUTE_MIX_EN	MUTE_IFAMP_EN
W										W		W			W	W	W	W	W	W	W	W	W

**Address:** 0x01

**Type:** W

**Reset:** 0x00

[23:14] **R[9:0]**: Reference clock divider ratio

[13:12] **PLL\_A[1:0]**: VCO amplitude control

[11:9] **CPSEL[2:0]**: Charge pump output current control

[8] **PSC\_SEL**: Prescaler modulus select ('0' for P=16, '1' for P=19)

[7] **CAL\_TYPE**: Calibration algorithm selection

0: standard calibration to optimize the phase noise versus temperature

1: enhanced calibration to maximize the  $\Delta T_{LK}$  range

[6] **SERCAL**:

at '1' starts the VCO auto-calibration (automatically reset to '0' at the end of calibration)

[5] **SELEXTCAL**: test purpose only. Must be set to '0'

[4] **MUTE\_EN**:

0: mute function disabled

1: mute function enabled

[3] **MUTE\_TYPE**: must be set to '1' while the mute function is enabled (mute IF output on Unlock state)

[2] **MUTE\_LOOUT\_EN**:

To be set to '1' to mute the LO output buffer

[1] **MUTE\_MIX\_EN**:

To be set to '1' to mute the Mixer circuitry

[0] **MUTE\_IFAMP\_EN**:

To be set to '1' to mute the IF amplifier circuitry

## ST3

## SPI register 3

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALC_PD	PKD_EN	PD[4:0]					B[11:0]													A[4:0]			
W	W	W					W													W			

**Address:** 0x10

**Type:** W

**Reset:** 0x00

[23] **ALC\_PD**: Test purpose only; must be set to '0' (ALC ON)

[22] **PKD\_EN**: for test purpose only; must be set to '0'

[21:17] **PD[4:0]**:

00000: (0 decimal) Power down mode

00001: (1 decimal) Standard Mode VCOA (VCOA and RX chain ON)

00010: (2 decimal) Standard Mode VCOB (VCOB and RX chain ON)

00011: (3 decimal) Diversity Slave Mode (ExtVCO/LO input buffer and RX Chain ON; internal synthesizer OFF)

00100: (4 decimal) Diversity Master Mode VCOA (VCOA, RX Chain and LO output buffer ON)

00101: (5 decimal) Diversity Master Mode VCOB (VCOB, RX Chain and LO output buffer ON)

00110: (6 decimal) External LO Standard Mode (RX Chain ON; PLL and ExtVCO/LO input buffer ON)

00111: (7 decimal) External LO Diversity Master Mode (RX Chain ON; PLL, ExtVCO/LO input buffer and LO output buffer ON)

[16:5] **B[11:0]**: B counter bits

[4:0] **A[4:0]**: A Counter Bits

## 10.4 Device calibration through the SPI interface

### 10.4.1 VCO calibration procedure (SPI interface)

The calibration of the VCO center frequency is activated by setting to '1' the SERCAL bit (ST2 Register bit [6]).

In order to program properly the device while ensuring the VCO calibration, the following procedure is required before every channel change:

1. Program the ST1 Register with the desired setting (DAC, Mixer, LO Control)
2. Program the ST3 Register with the desired setting (Functional mode, B and A counters)
3. Program the ST2 Register with the desired setting (R counter, VCO amplitude, Charge Pump, Prescaler Modulus) and SERCAL bit set to '1'

The maximum allowed PFD frequency ( $F_{PFD}$ ) to perform the calibration process is 1 MHz; if the desired  $F_{PFD}$  is higher than 1 MHz the following steps are needed:

4. Perform all the steps of the above calibration procedure programming the desired VCO frequency with a proper setting of R, B and A counter so that  $F_{PFD}$  results lower than 1 MHz.
5. Once calibration is completed program the device with the proper setting for the desired VCO and PFD frequencies according to the following steps:
  - a) Program the ST3 Register with the desired setting (Functional mode, B and A counters)
  - b) Program the ST2 Register with the desired setting (R counter, VCO amplitude, Charge Pump, Prescaler Modulus) with the SERCAL bit set to '0'.

### 10.4.2 Power ON sequence (SPI interface)

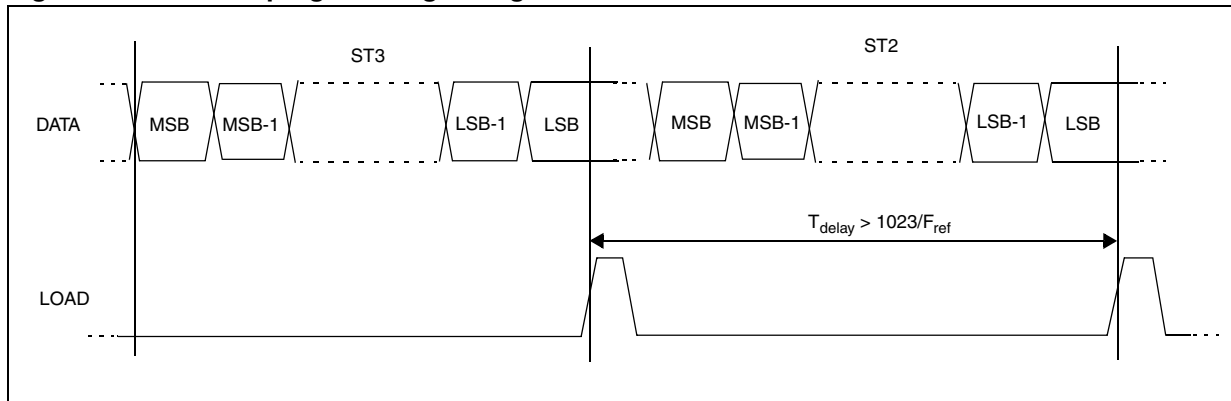
At power-on the device is configured in power-down mode.

In order to guarantee correct setting of the internal circuitry after the power on, the following steps must be followed:

1. Power up the device
2. Provide the reference clock
3. Implement the first programming sequence with a proper delay time between the ST3 and ST2 load rising edges (see [Figure 24](#)). The  $T_{\text{delay}}$  value must respect the following condition:

$$T_{\text{delay}} > 1023 \times \frac{1}{F_{\text{ref}}}$$

$F_{\text{ref}}$  is the reference clock frequency.

**Figure 24. SPI first programming timing**

### 10.4.3 VCO calibration auto-restart procedure (SPI interface)

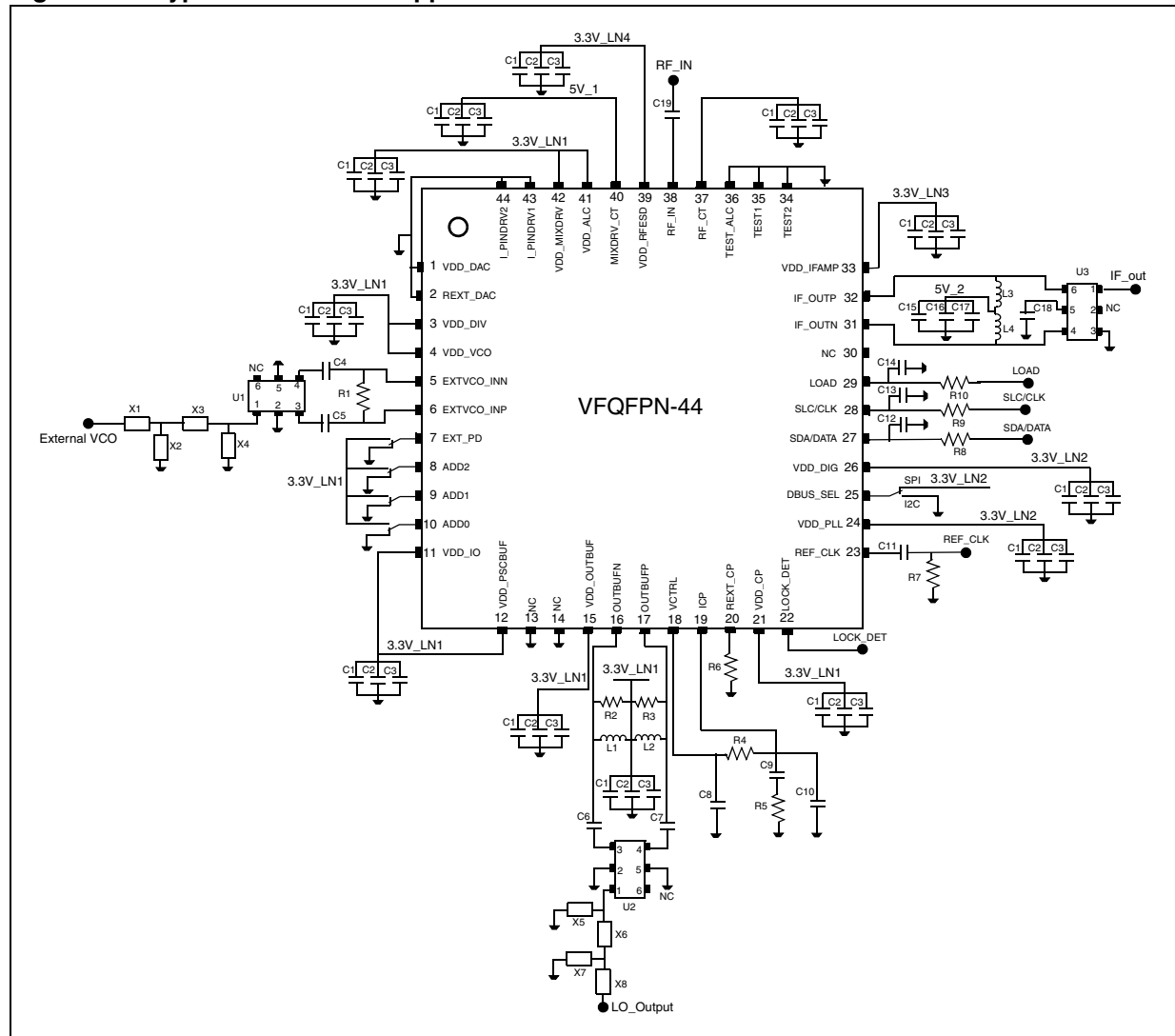
The VCO calibration auto-restart feature is enabled in two steps:

1. Set the desired frequency ensuring VCO calibration as described in [Section 10.4.1](#).
2. Program the ST1 register with the CAL\_AUTOSTART\_EN bit set to '1' while keeping unchanged the others.

## 11 Application information

### 11.1 Application circuit

Figure 25. Typical STW82103B application circuit



**Table 22. Application circuit component values**

Designation	Quantity	Description	Supplier
C1, C15	2	4.7 $\mu$ F capacitors COG (0402)	Murata Manufacturing Co., Ltd
C2, C11	2	1 nF capacitors COG (0402)	
C3	1	10 pF capacitor COG (0402)	
C4,C5	2	3.3 pF capacitors COG (0402)	
C6, C7	2	1.1 pF capacitor COG (0402)	
C8	1	270 pF capacitor COG (0402)	
C9	1	2.7 nF capacitor COG (0402)	Murata Manufacturing Co., Ltd
C10	1	68 pF capacitor COG (0402)	
C12, C13, C14	3	15 pF capacitors COG (0402)	
C16	1	100 nF capacitor COG (0402)	
C17	1	100 pF capacitor COG (0402)	
C18	1	180 pF capacitor COG (0402)	
C19	1	6.8 pF capacitor COG (0402)	
R1	1	100 ohm resistors (0402)	-
R2,R3,R7	3	50 ohm resistors (0402)	-
R4	1	2.2 kohm resistor (0402)	-
R5	1	8.2 kohm resistor (0402)	-
R6	1	4.7 kohm resistor (0402)	-
R8, R9, R10	3	100 ohm resistors (0402)	-
U1, U2	2	Balun JTI - 2450BL15K100	JOHANSON TECHNOLOGY
U3	1	Balun ADT4-5WT	Mini Circuits
X1	1	7.5 nH inductor CS (0402)	Coilcraft, Inc
X2	1	0.2 pF capacitor COG (0402)	Murata Manufacturing Co., Ltd
X3	1	10 nH inductor CS (0402)	Coilcraft, Inc
X4	0	NC	-
X5	0	NC	-
X6, X8	2	12 nH inductor CS (0402)	Coilcraft, Inc
X7	0	NC	-
X9	1	1 pF capacitor COG (0402)	Murata Manufacturing Co., Ltd
L1, L2	2	11 nH inductors CS (0402)	Coilcraft, Inc
L3, L4	2	220 nH inductors CS (1206)	

Note: 1 For optimum performance a low-noise 3.3 V power supply must be used.

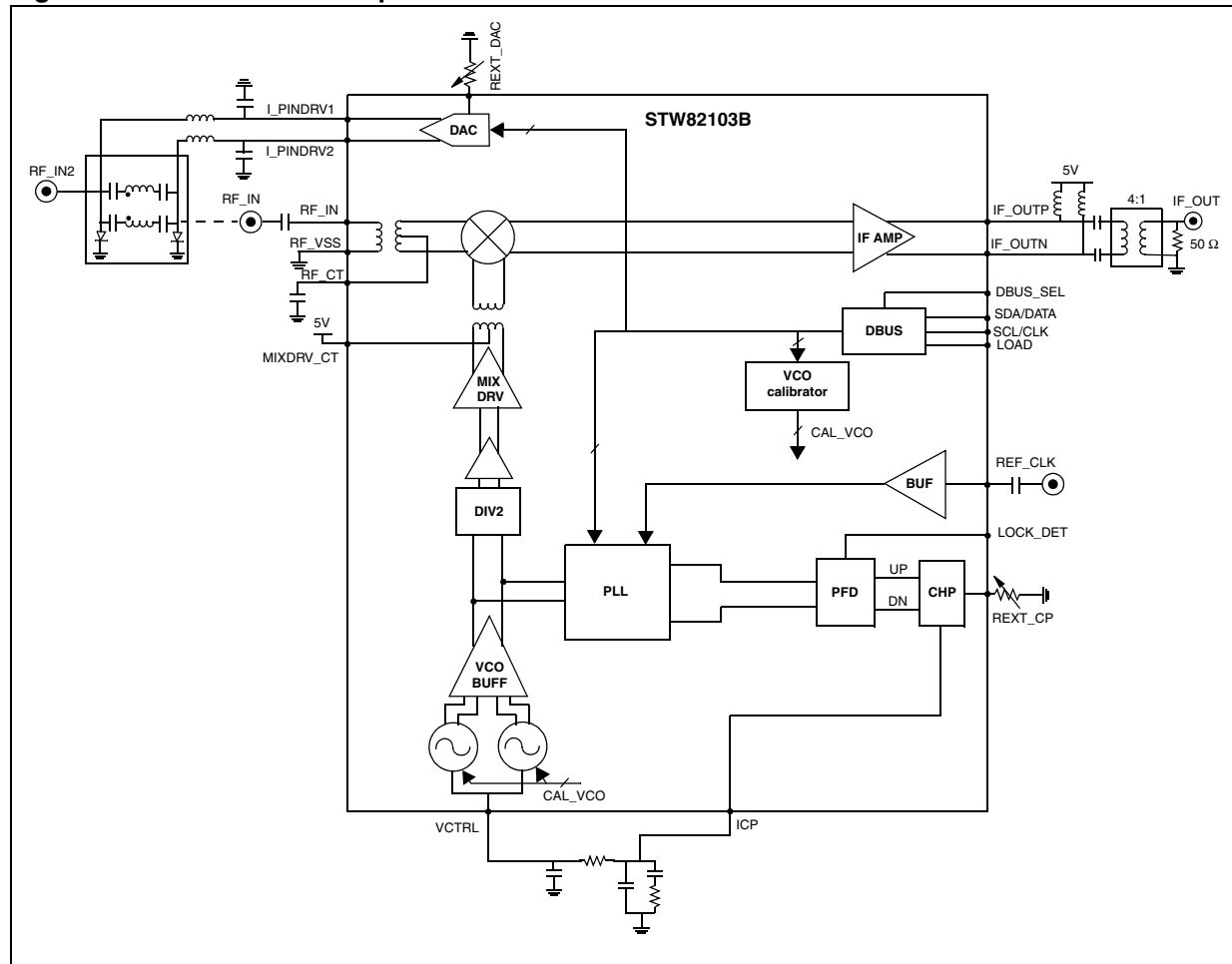
2 The 3.3 V and 5 V power supplies are split in order to maximize the isolation between RF, LO, IF and digital sections.

## 11.2 Standard Mode Operation

The STW82103B can be used in Standard Mode for both RX path and TX observation path (RX Chain ON and Synthesizer ON).

In such a case the 10-bit internal DAC can drive an external PIN diode attenuator in order to calibrate the signal level at the input of the device.

**Figure 26. Standard mode operation**

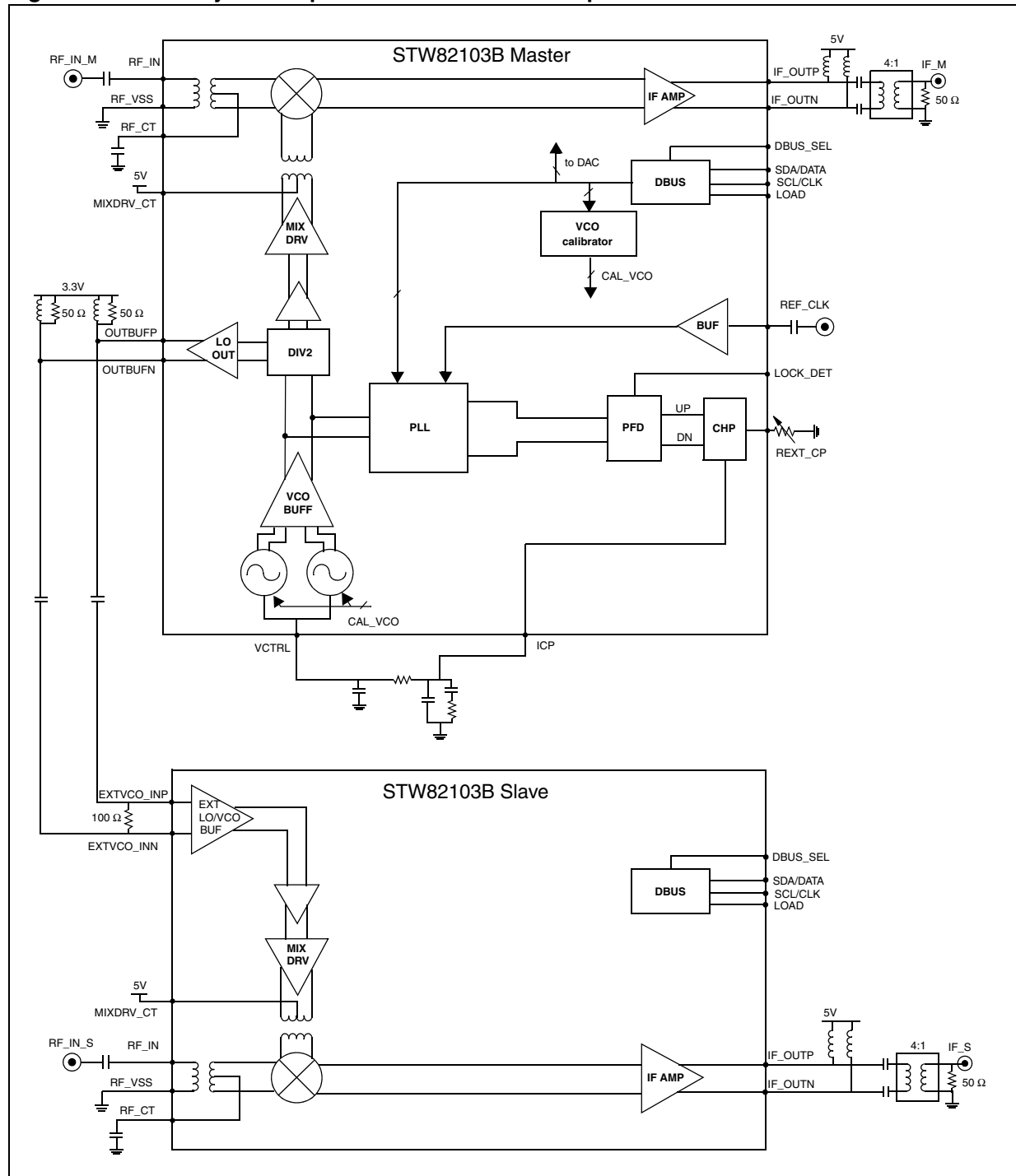




### 11.3 Diversity mode operation with same LO frequency

The STW82103B supports the Diversity mode with the same LO frequency by using one STW82103B in Master Mode (RX Chain ON, Synthesizer ON and LO output buffer ON) and the other in Slave Mode (RX Chain ON, Synthesizer OFF and EXT VCO/LO buffer ON). This operation mode is suitable for antenna diversity.

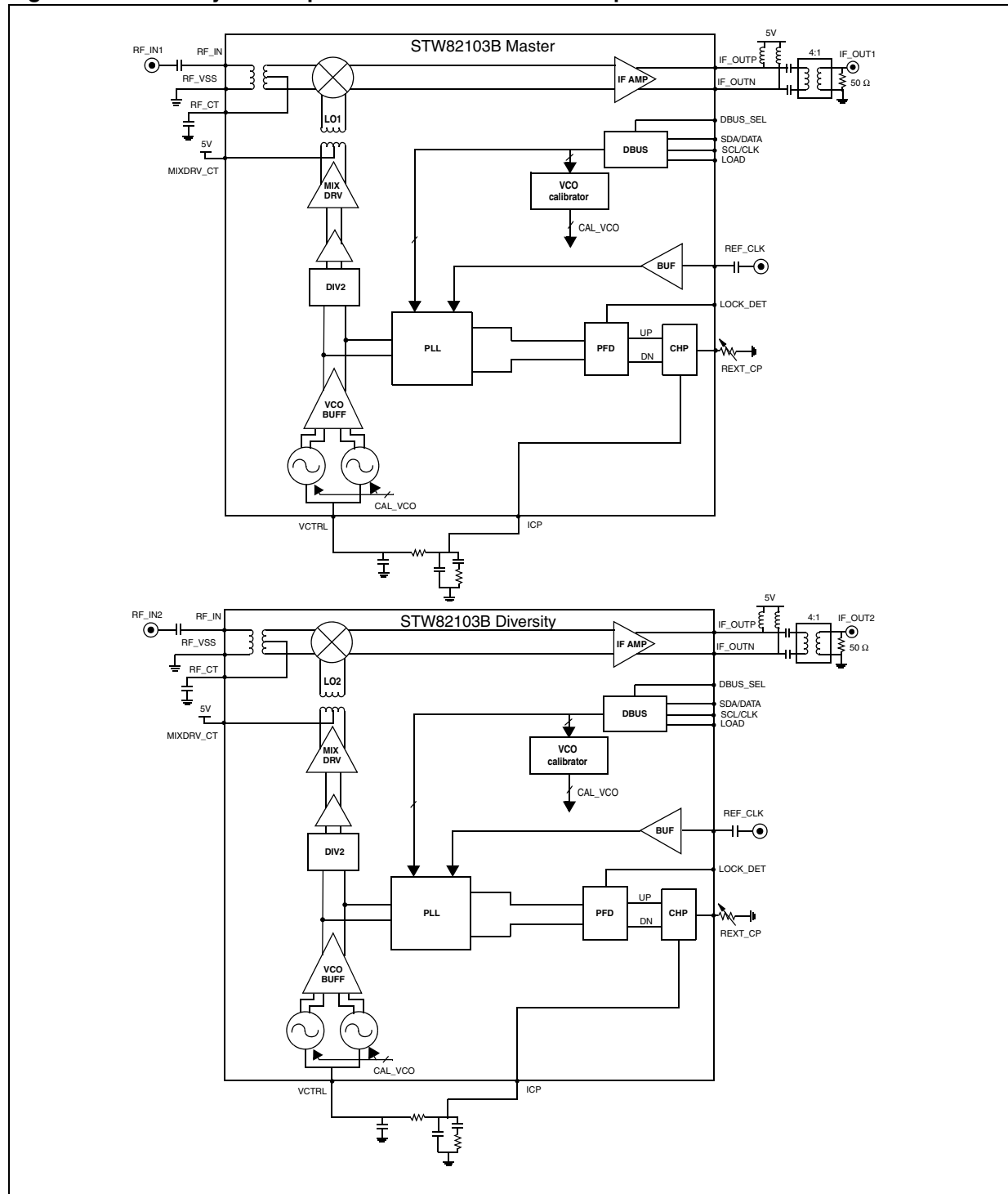
**Figure 27. Diversity mode operation with same LO frequencies**



## 11.4 Diversity mode operation with different LO frequencies

The STW82103B is particularly suitable for Diversity schemes using different LO frequencies such as the Interferer Diversity. In these schemes two STW82103Bs are used, each one set in Standard Mode and with different LO frequencies.

**Figure 28. Diversity mode operation with different LO frequencies**

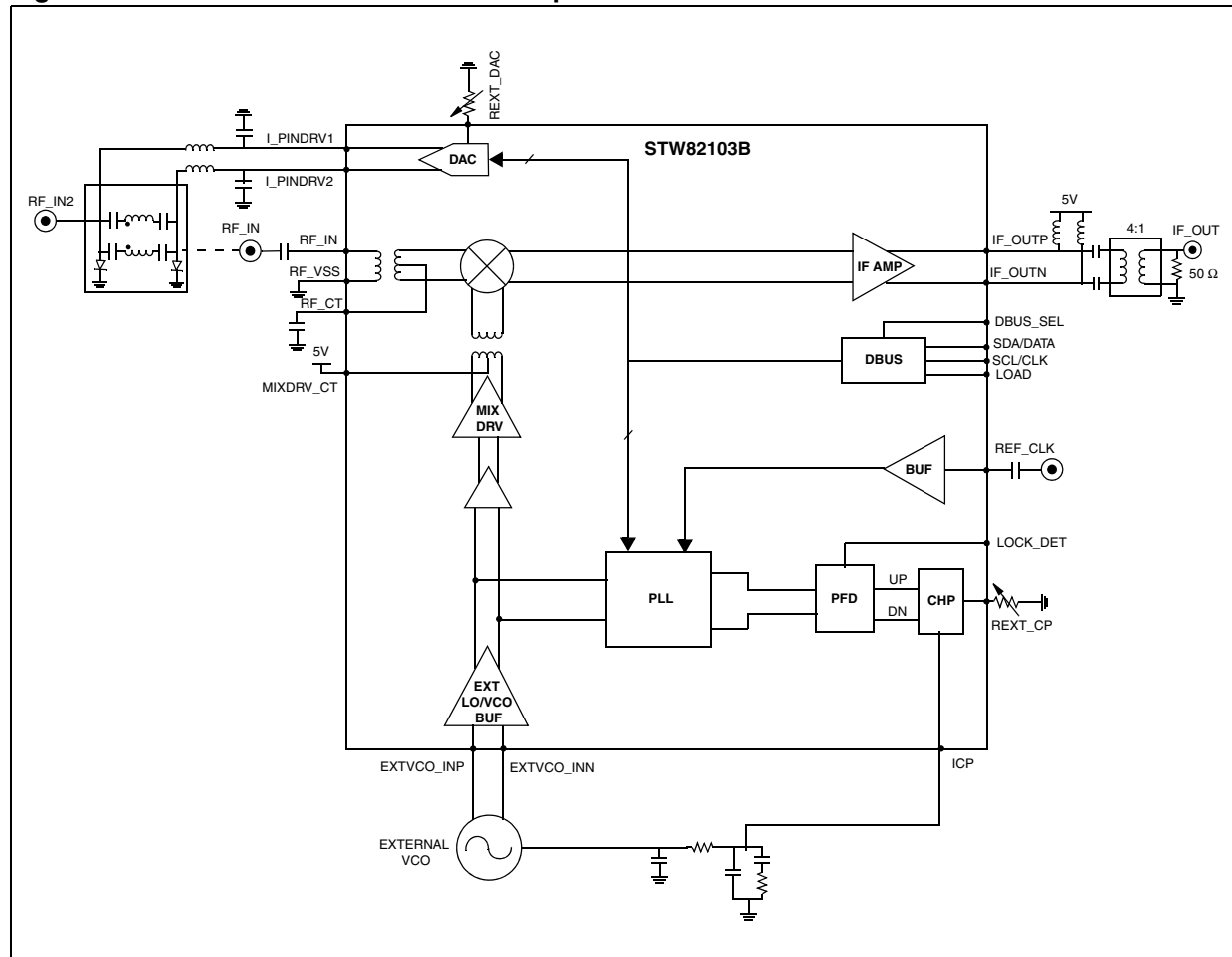


## 11.5 External VCO standard mode operation

The STW82103B can be used in Ext VCO Mode for both RX path and TX observation path (RX Chain ON, Synthesizer ON, EXT VCO/LO buffer ON and with an external VCO).

In such a case the 10-bit internal DAC can drive an external PIN diode attenuator in order to calibrate the signal level at the input of the device.

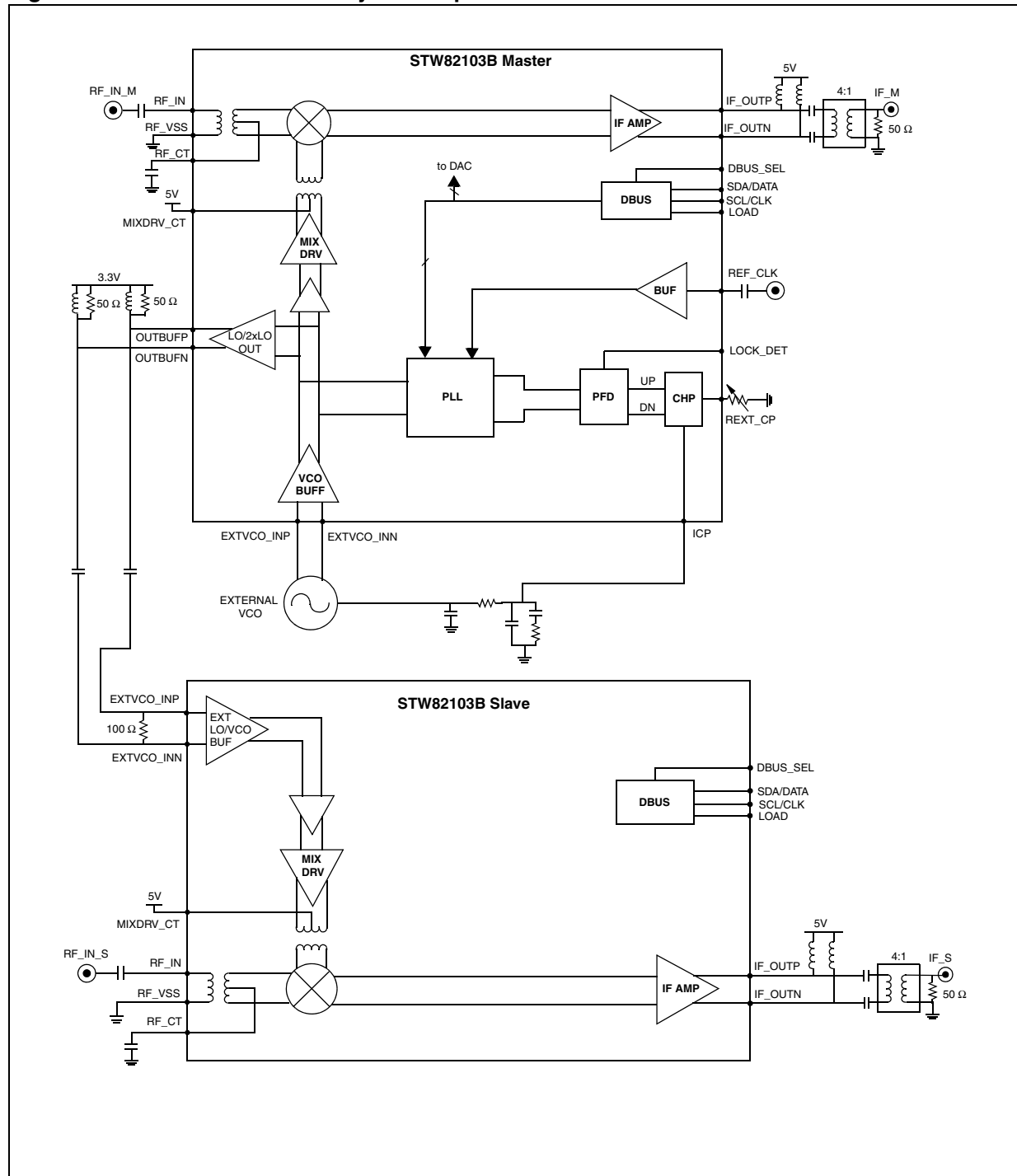
**Figure 29. External VCO standard mode operation**



## 11.6 External VCO diversity mode operation with same LO

The STW82103B can be used in Diversity mode using one STW82103B in Master Mode (RX Chain ON, Synthesizer ON, EXT VCO/LO buffer ON, LO output buffer ON and with an external VCO) and the other one in Slave Mode (RX Chain ON, Synthesizer OFF and EXT VCO/LO buffer ON).

**Figure 30. External VCO diversity mode operation with same LO**



## 12 Evaluation kit

An evaluation kit can be delivered upon request, including the following:

- Evaluation board
- GUI (graphical user interface) to program the device
- PLLSim software for PLL loop filter design and noise simulation

When ordering, please specify the following order code:

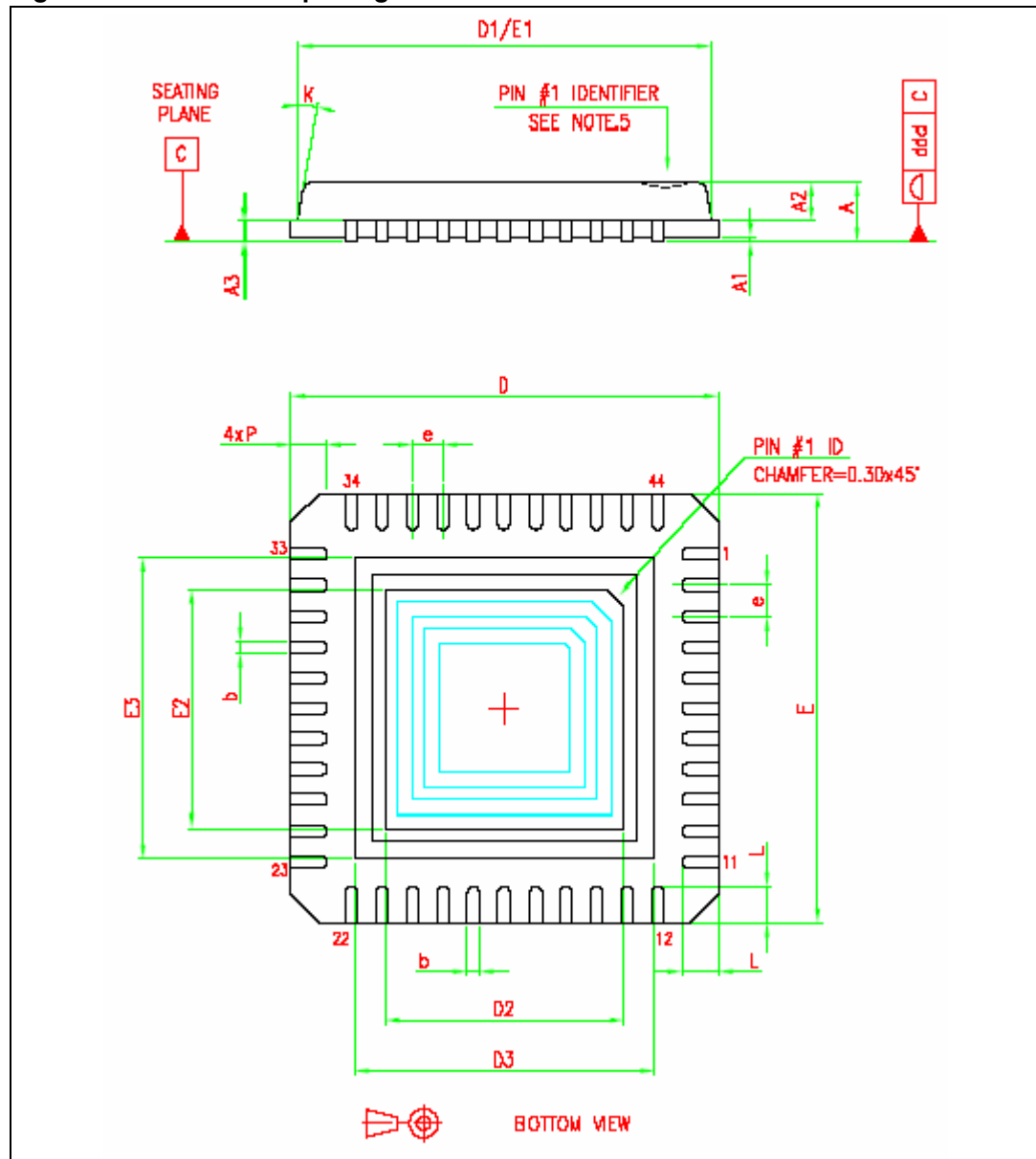
**Table 23. Evaluation kit order code**

Part number	Description
STW82103B-EVB	STW82103B evaluation kit, 2.3 to 2.7 GHz RF frequency range

## 13 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

**Figure 31. VFQFPN-44 package outline**



**Table 24. VFQFPN-44 package dimensions**

Symbol	Dimensions in mm		
	Min	Typ	Max
A	0.80	0.90	1.00
A1	-	0.02	0.05
A2	-	0.65	1.00
A3	-	0.200	-
b	0.18	0.25	0.30
D	6.85	7.00	7.15
D1	-	6.750	-
D2	3.80	3.90	4.00
D3	-	4.90	-
E	6.85	7.00	7.15
E1	-	6.750	-
E2	3.80	3.90	4.00
E3	-	4.90	-
e	-	0.50	-
L	0.35	0.55	0.75
P	-	-	0.60
K (degree)	-	-	12
ddd	-	-	0.08

- Note:**
- 1 VFQFPN stands for *Thermally Enhanced Very thin Fine pitch Quad Flat Package No lead*.  
Very thin: A=1.00 Max.
  - 2 Details of terminal 1 identifier are optional but must be located on the top surface of the package by using either a mold or marked features.

## 14 Revision history

**Table 25. Document revision history**

Date	Revision	Changes
11-Mar-2011	1	First release
19-Apr-2012	2	<p>Cover page:</p> <ul style="list-style-type: none"> <li>– IIP3 value changed to +25 dBm</li> <li>– 2FRF-2FLO spurious rejection changed to 80 dBc</li> <li>– Noise figure NF changed to 10.5 dB</li> <li>– Removed 'Preliminary Data' tags.</li> </ul> <p>Table 3 moved to new <a href="#">Section 3: Absolute maximum ratings</a></p> <p>Section 2.1 becomes <a href="#">Section 4: Operating conditions</a></p> <p>Section 2.2 becomes <a href="#">Section 5: Test conditions</a></p> <p>Section 2.3 becomes <a href="#">Section 6: Electrical characteristics</a></p> <p><a href="#">Table 4: Operating conditions</a> updated current consumption:</p> <ul style="list-style-type: none"> <li>– <math>I_{CC3.3V}</math>: Updated typical values of diversity master modes. Added maximum values.</li> <li>– <math>I_{CC5V}</math>: Updated typical and added maximum values.</li> </ul> <p><a href="#">Section 6: Electrical characteristics</a>. Added note about <math>V_{supply}</math>, RF frequency range, ambient temperature and RF power conditions.</p> <p><a href="#">Table 6: Down converter mixer and IF amplifier electrical characteristics</a> : updated:</p> <ul style="list-style-type: none"> <li>– CG added minimum and max values.</li> <li>– <math>IP_{1dB}</math> updated high-current mode value</li> <li>– IIP3 added minimum values and updated typical values</li> <li>– nFRF-nFLO modified typical values</li> <li>– <math>NF_{SSB}</math> added maximum values</li> <li>– LO to RF leakage typical value modified</li> <li>– RF to IF isolation typical value modified</li> <li>– <math>IF_{RL}</math> typical value modified</li> <li>– <math>ICC_{MD}</math> 3.3 V on pins 41 and 42, modified typical values</li> <li>– <math>ICC_{IFAM}</math> 5 V supply value on pins 31 and 32, modified typical value</li> </ul> <p><a href="#">Table 8: Integer-N synthesizer electrical characteristics</a> updated:</p> <ul style="list-style-type: none"> <li>– <math>K_{VCOA}</math> typical values for high and intermediate frequency ranges</li> <li>– <math>K_{VCOB}</math> typical values for all frequency ranges</li> <li>– <math>\Delta T_{LK}</math> split into <math>\Delta T_{LK A}</math> and <math>\Delta T_{LK B}</math> (for VCOA and VCOB). Specified as maximum values.</li> <li>– modified table footnote 4</li> </ul> <p><a href="#">Table 9: Phase noise performance</a> updated typical values of:</p> <ul style="list-style-type: none"> <li>– Integrated Phase Noise (single sided) 100 Hz to 40 MHz</li> <li>– LOA open-loop phase noise @ 1 kHz, 10 kHz, 100 kHz, 10 MHz and phase noise floor @ 40 MHz</li> <li>– LOB open-loop phase noise @ 1 kHz, 10 kHz, 100 kHz, 1 MHz, 10 MHz and phase noise floor @ 40 MHz</li> </ul>



Table 25. Document revision history (continued)

Date	Revision	Changes
19-Apr-2012	2	<p>Added <a href="#">Section 7: Typical performance characteristics</a>.  <a href="#">Section 8.1.9: Voltage controlled oscillators</a>. Modified :</p> <ul style="list-style-type: none"> <li>– <a href="#">VCO frequency calibration</a></li> <li>– <a href="#">VCO calibration auto-restart feature</a></li> <li>– <a href="#">Table 12: VCOB performance against amplitude setting (frequency = 2.8 GHz)</a> values of PN @ 1 MHz</li> </ul> <p><a href="#">Table 12: VCOB performance against amplitude setting (frequency = 2.8 GHz)</a>, modified values of linearity performance.</p> <p><a href="#">Section 9.3.2: I<sup>2</sup>C register definitions</a>. Updated description of bitfield CALTYPE and MUTE_TYPE in registers <a href="#">MUTE_&amp;_CALIBRATION</a></p> <p>Added <a href="#">Section 9.4.2: Power ON sequence (I<sup>2</sup>C interface)</a></p> <ul style="list-style-type: none"> <li>– modified <a href="#">Figure 23: SPI timing waveforms</a></li> <li>– modified <a href="#">Table 20: SPI timing parameters</a> minimum values of <math>t_{\text{clk\_loadr}}</math> and <math>t_{\text{clk\_loadf}}</math>.</li> </ul> <p><a href="#">Section 10.3.2: SPI register definitions</a>: updated</p> <ul style="list-style-type: none"> <li>– description of bitfields CALTYPE and MUTE_TYPE in register <a href="#">ST2</a></li> <li>– description of bitfield PD[4:0] in register <a href="#">ST3</a></li> </ul> <p>Added <a href="#">Section 10.4.2: Power ON sequence (SPI interface)</a></p> <p>Added <a href="#">Section 12: Evaluation kit</a>.</p>

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