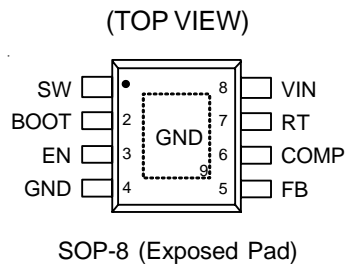


## Pin Configurations



## Functional Pin Description

Pin No.	Pin Name	Pin Function
1	SW	Switch Node. Connect to external L-C filter.
2	BOOT	Bootstrap Supply for the High-Side MOSFET. Connect a 100nF or greater capacitor between the BOOT and SW pins.
3	EN	Enable Control Input. A logic-high enables the converter; a logic-low forces the device into shutdown mode.
4, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum thermal dissipation.
5	FB	Feedback Voltage Input. This pin is used to set the output voltage of the converter to regulate to the desired value via an resistive divider.
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a R-C network from the COMP to GND. In some cases, an additional capacitor from COMP to GND is required.
7	RT	Switching Frequency Setting. Connect an external resistor to set the switching frequency from 300kHz to 1MHz.
8	VIN	Power Input. The input voltage range is from 4.5V to 36V. Must bypass with a suitable large ceramic capacitor at this pin.



**Absolute Maximum Ratings** (Note 1)

Supply Voltage, $V_{IN}$	-----	-0.3V to 40V
Switch Voltage, $SW$	-----	-0.3V to ( $V_{IN} + 0.3V$ )
BOOT Pin	-----	-0.3V to 46.3V
EN Pin (with REN (150k $\Omega$ to 600k $\Omega$ ) to $V_{IN}$ )	-----	-0.3V to 40V
SW Voltage ( $t < 10ns$ )	-----	-5V to 46.3V
EN Pin	-----	-0.3V to 3.6V
Other Pins	-----	-0.3V to 6V
Power Dissipation, $P_D$ @ $T_A = 25^\circ C$		
SOP-8 (Exposed Pad)	-----	2.041W
Package Thermal Resistance (Note 2)		
SOP-8 (Exposed Pad), $\theta_{JA}$	-----	49°C/W
SOP-8 (Exposed Pad), $\theta_{JC}$	-----	8°C/W
Lead Temperature (Soldering, 10 sec.)	-----	260°C
Junction Temperature	-----	150°C
Storage Temperature Range	-----	-65°C to 150°C
ESD Susceptibility (Note 3)		
HBM (Human Body Model)	-----	2kV

**Recommended Operating Conditions** (Note 4)

Supply Input Voltage, $V_{IN}$	-----	4.5V to 36V
Junction Temperature Range	-----	-40°C to 125°C
Ambient Temperature Range	-----	-40°C to 85°C

**Electrical Characteristics**

( $V_{IN} = 12V$ ,  $C_{IN} = 20\mu F$ ,  $T_A = -40^\circ C$  to  $85^\circ C$ , unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Supply Current			$V_{EN} = 0V$	--	--	10	$\mu A$
Quiescent Current		$I_Q$	$V_{EN} = 3V$ , $V_{FB} = 0.9V$	--	1	1.3	mA
Feedback Reference Voltage		$V_{REF}$	$4.5V \leq V_{IN} \leq 36V$	0.784	0.8	0.816	V
Switch On-Resistance	High-Side	$R_{DS(ON)1}$		--	105	190	m $\Omega$
	Low-Side	$R_{DS(ON)2}$		--	80	145	
High-Side Switch Current Limit Range		$U_{OC}$		4.25	5	5.75	A
Low-Side Switch Current Limit			From Drain to Source	--	1.7	--	A
Oscillation Frequency		$f_{OSC1}$	$R_T = 191k\Omega$	264	300	336	kHz
			$R_T = 113k\Omega$	440	500	560	
			$R_T = 51k\Omega$	880	1000	1120	
Short-Circuit Oscillation Frequency		$f_{OSC2}$	$V_{FB} = 0V$ , $R_T = 113k\Omega$	--	50	--	kHz
Maximum Duty Cycle		$D_{MAX}$	$V_{FB} = 0.7V$	--	95	--	%
Minimum On-Time		$t_{ON}$		--	100	120	ns

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Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
EN Input Voltage	Logic-High	V <sub>IH</sub>		2	--	3.3	V
	Logic-Low	V <sub>IL</sub>		--	--	0.4	
Input Under-Voltage Lockout Threshold		V <sub>UVLO</sub>	V <sub>IN</sub> Rising	3.7	4.2	4.5	V
Input Under-Voltage Lockout Hysteresis		ΔV <sub>UVLO</sub>		--	250	--	mV
Thermal Shutdown Threshold		T <sub>SD</sub>		--	150	--	°C
Thermal Shutdown Hysteresis		ΔT <sub>SD</sub>		--	25	--	°C
COMP to Current Sense Trans-conductance		G <sub>CS</sub>	ΔI <sub>COMP</sub> = ±10μA	--	4.1	--	A/V
Error Amplifier Trans-conductance		G <sub>EA</sub>		--	950	--	μA/V

**Note 1.** Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** θ<sub>JA</sub> is measured at T<sub>A</sub> = 25 °C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ<sub>JC</sub> is measured at the exposed pad of the package. The PCB copper area with exposed pad is 70mm<sup>2</sup>.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

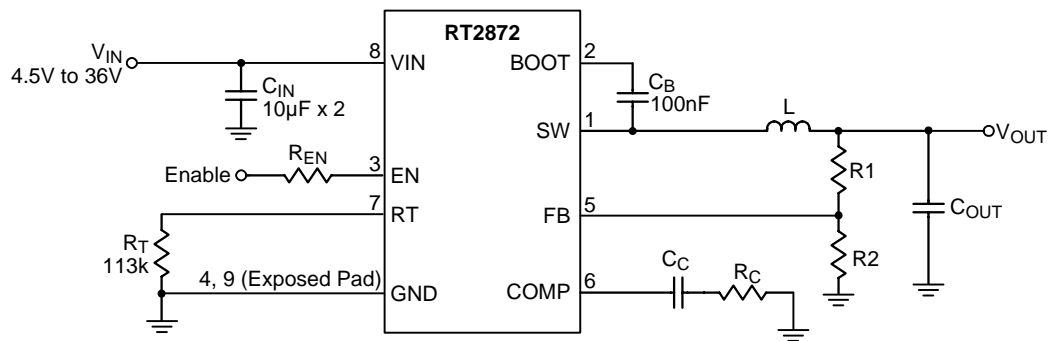
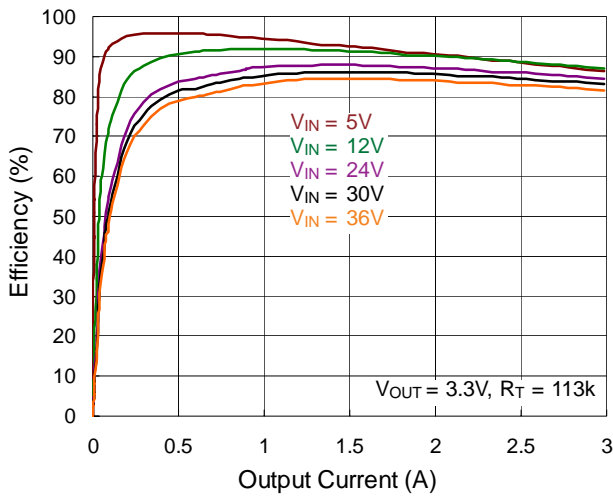


Table 1. Suggested Component Values

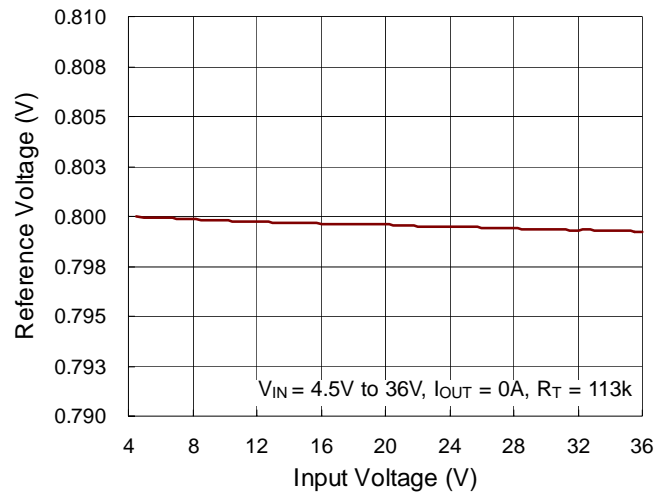
V <sub>OUT</sub> (V)	R <sub>1</sub> (kΩ)	R <sub>2</sub> (kΩ)	R <sub>C</sub> (kΩ)	L (μH)	C <sub>C</sub> (nF)	C <sub>OUT</sub> (μF)
12	47	3.35	47	10	2.7	22 x 2
8	27	3	36	8.2	2.7	22 x 2
5	62	11.8	24	6.8	2.7	22 x 2
3.3	75	24	16	4.7	2.7	22 x 2
2.5	25.5	12	12	3.6	2.7	22 x 2
1.2	30	60	6.8	2.2	2.7	22 x 2

## Typical Operating Characteristics

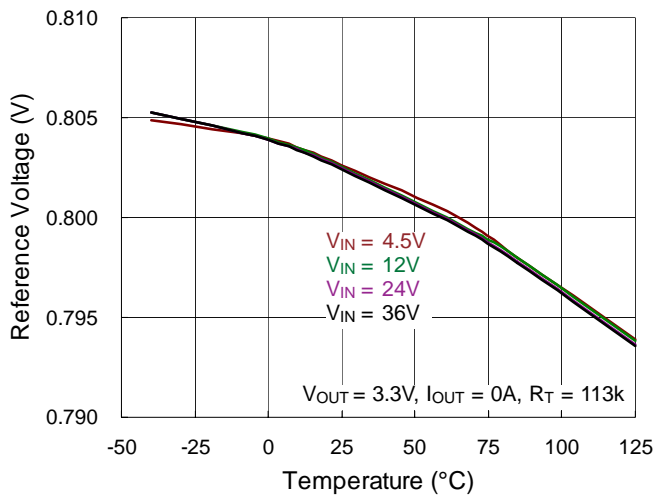
Efficiency vs. Output Current



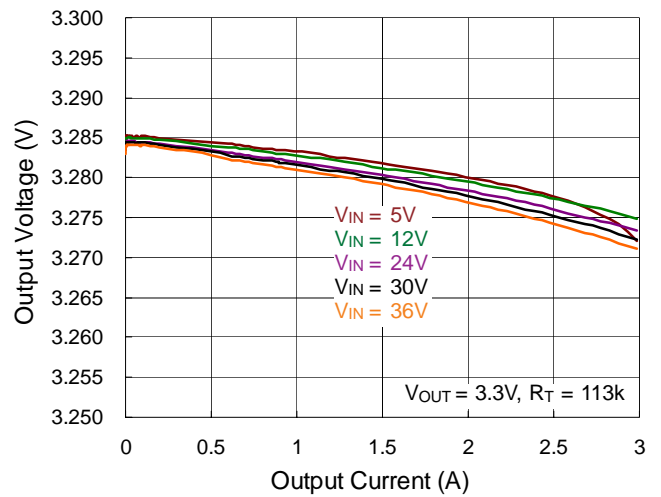
Reference Voltage vs. Input Voltage



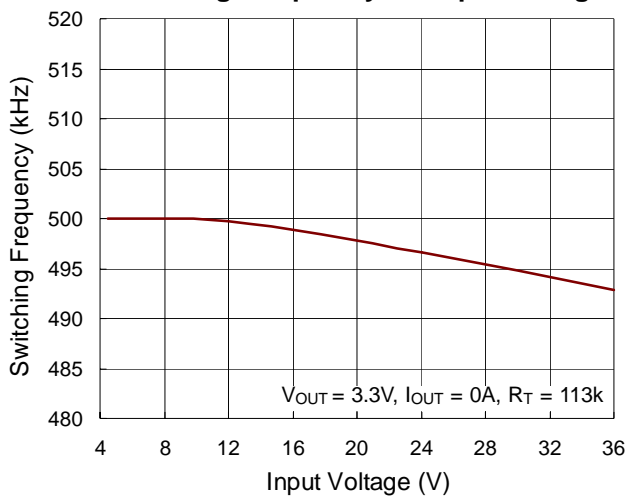
Reference vs. Temperature



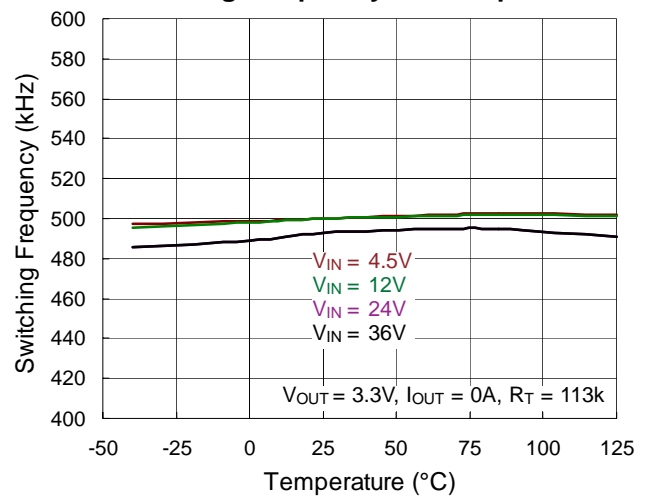
Output Voltage vs. Output Current



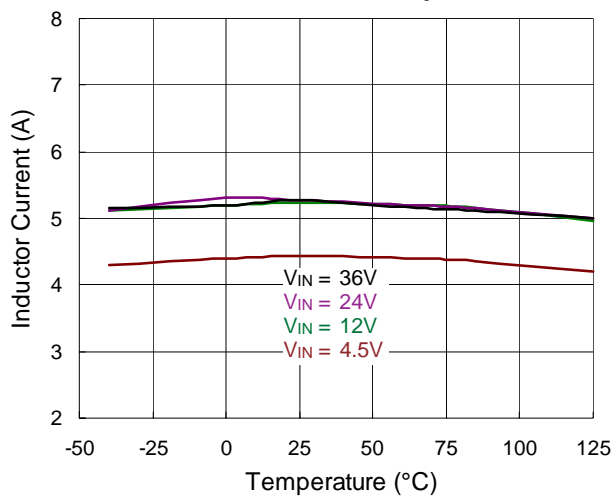
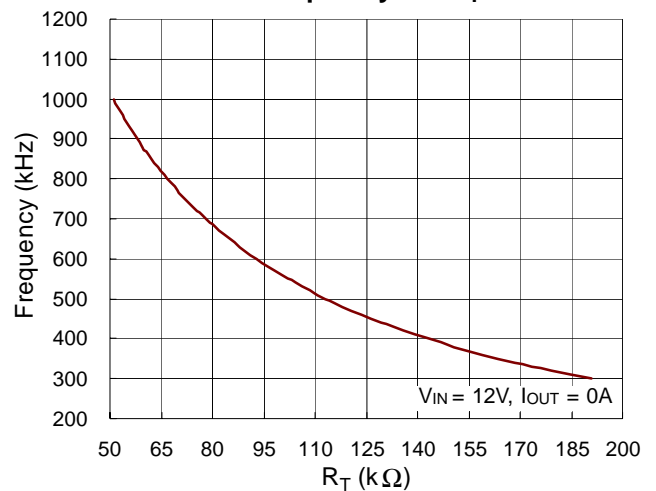
Switching Frequency vs. Input Voltage



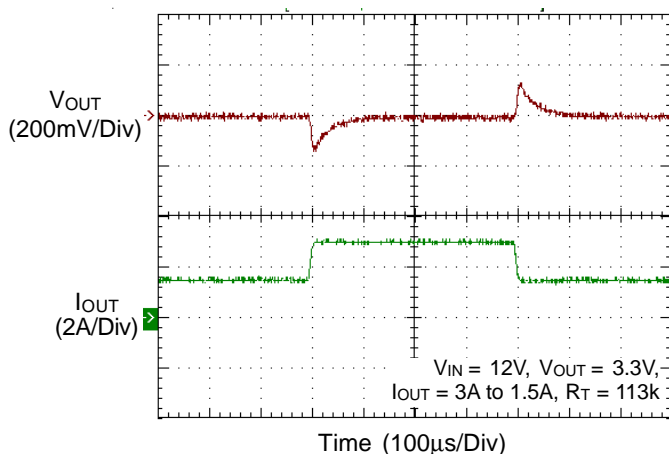
Switching Frequency vs. Temperature



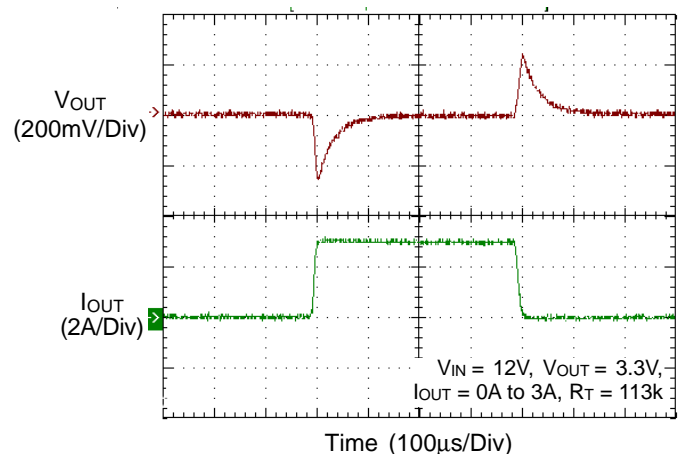
Current Limit vs. Temperature

Frequency vs.  $R_T$ 

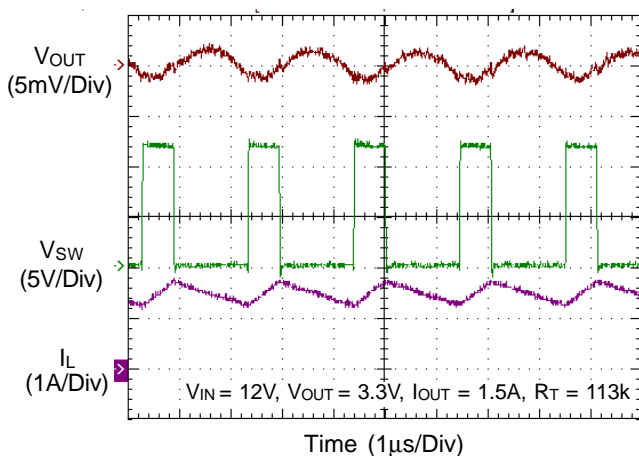
Load Transient Response



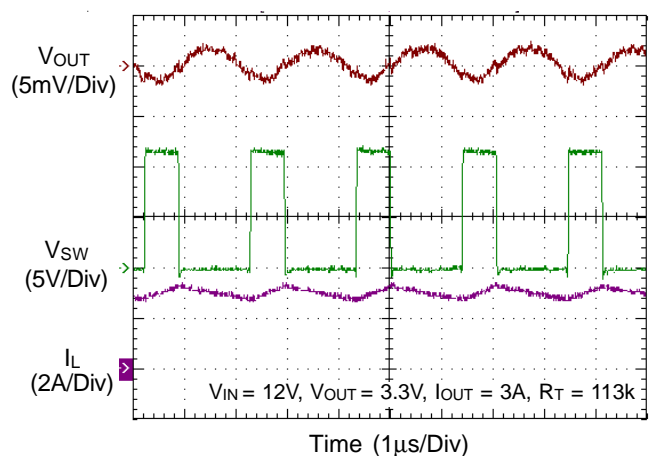
Load Transient Response



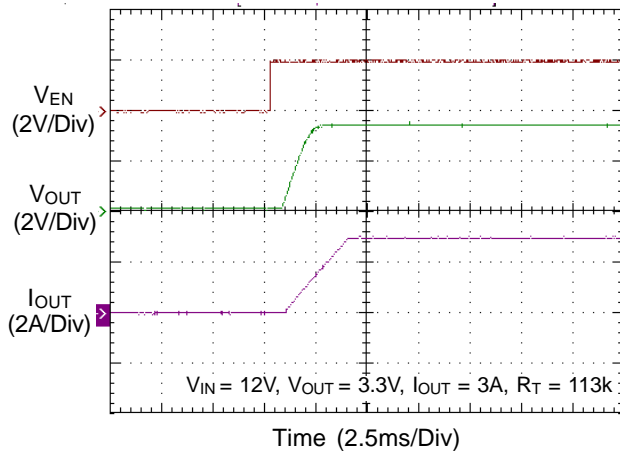
Switching



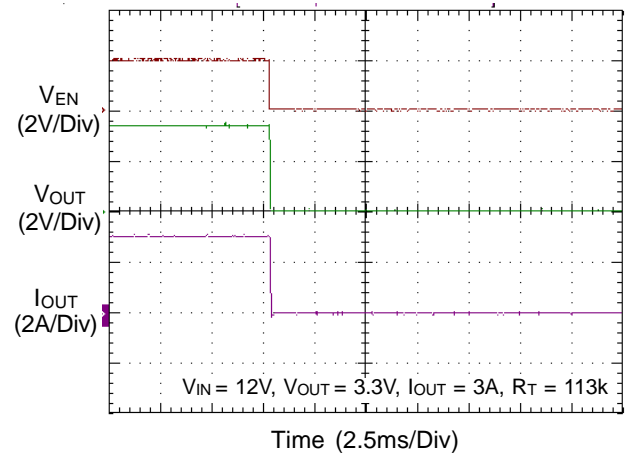
Switching



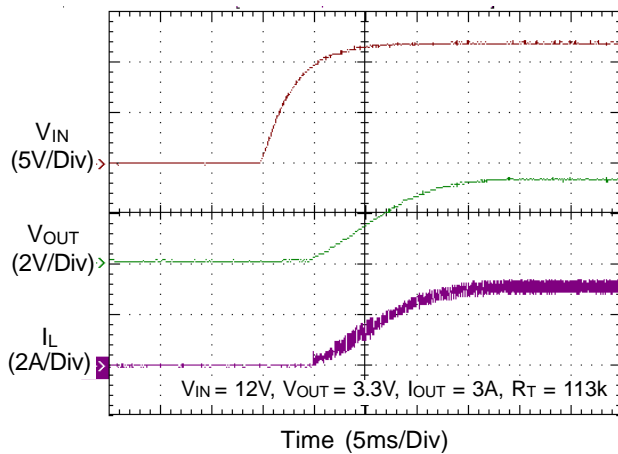
Power On from EN



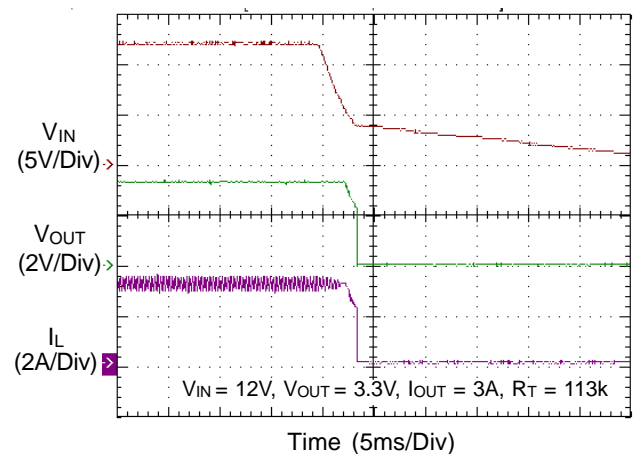
Power Off from EN



Power On from VIN



Power Off from VIN



## Application Information

### Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage as shown in Figure 1.

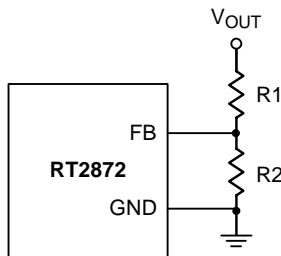


Figure 1. Output Voltage Setting

The output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{REF} \left( 1 + \frac{R1}{R2} \right)$$

where  $V_{REF}$  is the reference voltage (0.8V typ.).

### External Bootstrap Diode

Connect a 0.1μF low ESR ceramic capacitor between the BOOT and SW pins. This capacitor provides the gate driver voltage for the high-side MOSFET.

It is recommended to add an external bootstrap diode between an external 5V and BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65% .The bootstrap diode can be a low cost one such as IN4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the RT2872. Note that the external boot voltage must be lower than 5.5V

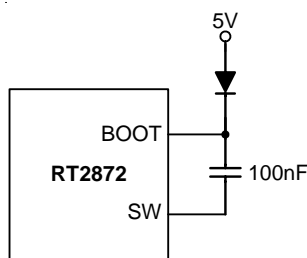


Figure 2. External Bootstrap Diode

### Chip Enable Operation

The EN pin is the chip enable input. Pulling the EN pin low (<0.4V) will shutdown the device. During shutdown mode, the RT2872 quiescent current drops to lower than 3μA. Driving the EN pin high (>2.5V, <3.3V) will turn on the device again. For external timing control, the EN pin can also be externally pulled high by adding a  $R_{EN}$  resistor and  $C_{EN}$  capacitor from the VIN pin (see Figure 3).

$R_{EN}$  must be chose between 150kΩ to 600kΩ, which is to avoid huge leak current into chip.

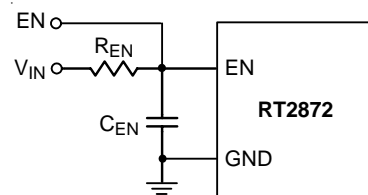


Figure 3. Enable Timing Control

An external MOSFET can be added to implement digital control on the EN pin when no system voltage above 2.5V is available, as shown in Figure 4. In this case, a 300kΩ pull-up resistor,  $R_{EN}$ , is connected between  $V_{IN}$  and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin.

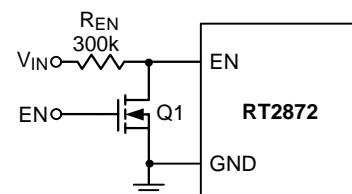


Figure 4. Digital Enable Control Circuit

### Under-Voltage Protection

#### Hiccup Mode

The RT2872 provides Hiccup Mode Under-Voltage Protection (UVP). When the  $V_{FB}$  voltage drops below 0.4V, the UVP function will be triggered to shut down switching operation. If the UVP condition remains for a period, the RT2872 will retry automatically. When the UVP condition is removed, the converter will resume operation. The UVP is disabled during soft-start period.

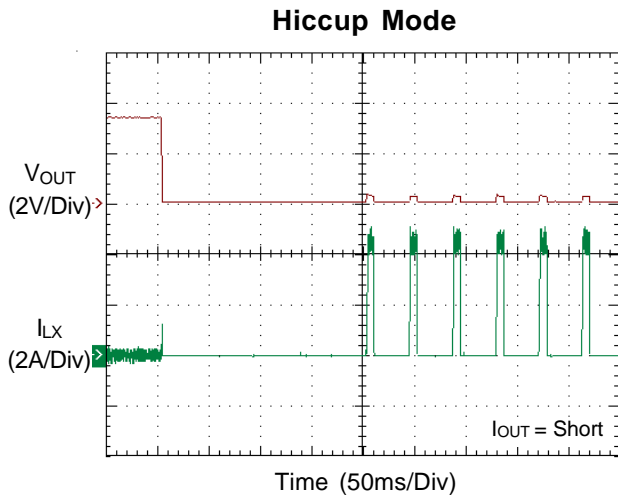


Figure 5. Hiccup Mode Under-Voltage Protection

### Over-Temperature Protection

The RT2872 features an Over-Temperature Protection (OTP) circuitry to prevent overheat due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C, the converter will resume operation. To maintain continuous operation, the maximum junction temperature should be lower than 125°C.

### Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current  $\Delta I_L$  increases with higher  $V_{IN}$  and decreases with higher inductance.

$$\Delta I_L = \left[ \frac{V_{OUT}}{f \times L} \right] \times \left[ 1 - \frac{V_{OUT}}{V_{IN}} \right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve the highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of  $\Delta I_L = 0.24(I_{MAX})$  will be a reasonable starting point. The largest ripple current occurs at the highest  $V_{IN}$ . To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[ \frac{V_{OUT}}{f \times \Delta I_L(MAX)} \right] \times \left[ 1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right]$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit. Please see Table 2 for the inductor selection reference.

Table 2. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions (mm)
TDK	VLF10045	10 x 9.7 x 4.5
TDK	SLF12565	12.5 x 12.5 x 6.5
TAIYO YUDEN	NR8040	8 x 8 x 4

### C<sub>IN</sub> and C<sub>OUT</sub> Selection

The input capacitance,  $C_{IN}$ , is needed to filter the trapezoidal current at the Source of the high-side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The approximate RMS current equation is given :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at  $V_{IN} = 2V_{OUT}$ , where  $I_{RMS} = I_{OUT} / 2$ . This simple worst case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

For the input capacitor, two 10μF low ESR ceramic capacitors are suggested. For the suggested capacitor, please refer to Table 3 for more details.

The selection of  $C_{OUT}$  is determined by the required ESR to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for  $C_{OUT}$  selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple,  $\Delta V_{OUT}$ , is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple will be the highest at the maximum input voltage since  $\Delta I_L$  increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input,  $V_{IN}$ . At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at  $V_{IN}$  large enough to damage the part.

## Switching Frequency Setting

The switching frequency can be set by using extra resistor  $R_T$ . Switching frequency range is from 300kHz to 1MHz. Through extra resistor  $R_T$  connect to  $R_T$  pin to setting the switching frequency  $f_S$ , below offer approximate formula equation :

$$\frac{1000}{\frac{1000}{f_S (\text{kHz})} - 0.22} = \frac{66876}{R_T (\text{k}\Omega)} - 29.405$$

## Thermal Considerations

For continuous operation, do not exceed the maximum operation junction temperature  $125^\circ\text{C}$ . The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(\text{MAX})} = (T_{J(\text{MAX})} - T_A) / \theta_{JA}$$

Where  $T_{J(\text{MAX})}$  is the maximum operation junction temperature,  $T_A$  is the ambient temperature and the  $\theta_{JA}$  is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT2872, the maximum junction temperature is  $125^\circ\text{C}$ . The junction to ambient thermal resistance  $\theta_{JA}$  is layout dependent. For SOP-8 (Exposed Pad) package, the

thermal resistance  $\theta_{JA}$  is  $75^\circ\text{C/W}$  on the standard JEDEC 51-7 four-layers thermal test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by following formula :

$$P_{D(\text{MAX})} = (125^\circ\text{C} - 25^\circ\text{C}) / (75^\circ\text{C/W}) = 1.333\text{W} \quad (\text{min.copper area PCB layout})$$

$$P_{D(\text{MAX})} = (125^\circ\text{C} - 25^\circ\text{C}) / (49^\circ\text{C/W}) = 2.04\text{W} \quad (70\text{mm}^2\text{copper area PCB layout})$$

The thermal resistance  $\theta_{JA}$  of SOP-8 (Exposed Pad) is determined by the package architecture design and the PCB layout design. However, the package architecture design had been designed. If possible, it's useful to increase thermal performance by the PCB layout copper design. The thermal resistance  $\theta_{JA}$  can be decreased by adding copper area under the exposed pad of SOP-8 (Exposed Pad) package.

As shown in Figure 6, the amount of copper area to which the SOP-8 (Exposed Pad) is mounted affects thermal performance. When mounted to the standard SOP-8 (Exposed Pad) pad (Figure 6.a),  $\theta_{JA}$  is  $75^\circ\text{C/W}$ . Adding copper area of pad under the SOP-8 (Exposed Pad) (Figure 6.b) reduces the  $\theta_{JA}$  to  $64^\circ\text{C/W}$ . Even further, increasing the copper area of pad to  $70\text{mm}^2$  (Figure 6.e) reduces the  $\theta_{JA}$  to  $49^\circ\text{C/W}$ .

The maximum power dissipation depends on operating ambient temperature for fixed  $T_{J(\text{MAX})}$  and thermal resistance  $\theta_{JA}$ . The Figure 7 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

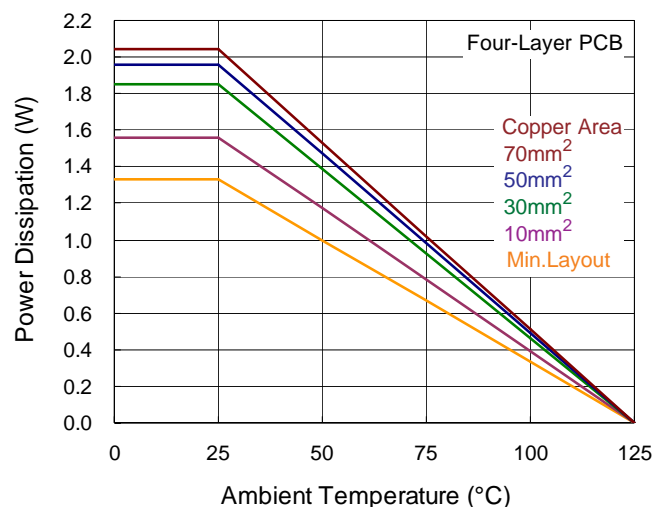
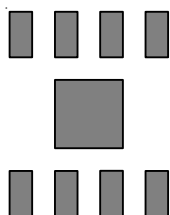
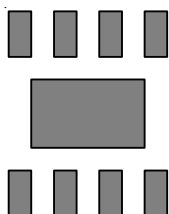


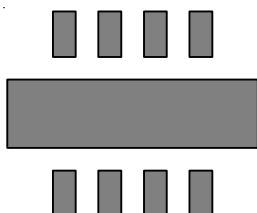
Figure 7. Derating Curve of Maximum Power Dissipation



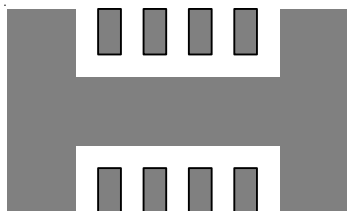
(a) Copper Area =  $(2.3 \times 2.3) \text{ mm}^2$ ,  $\theta_{JA} = 75^\circ\text{C/W}$



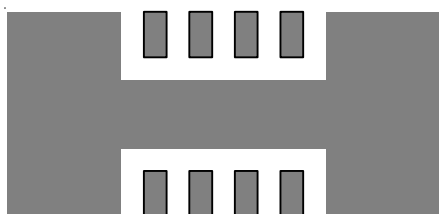
(b) Copper Area =  $10 \text{ mm}^2$ ,  $\theta_{JA} = 64^\circ\text{C/W}$



(c) Copper Area =  $30 \text{ mm}^2$ ,  $\theta_{JA} = 54^\circ\text{C/W}$



(d) Copper Area =  $50 \text{ mm}^2$ ,  $\theta_{JA} = 51^\circ\text{C/W}$



(e) Copper Area =  $70 \text{ mm}^2$ ,  $\theta_{JA} = 49^\circ\text{C/W}$

Figure 6. Thermal Resistance vs. Copper Area Layout Design

### Layout Considerations

For best performance of the RT2872, the following layout guidelines must be strictly followed.

- ▶ Input capacitor must be placed as close to the IC as possible.
- ▶ SW should be connected to inductor by wide and short trace. Keep sensitive components away from this trace.
- ▶ The  $R_T$  resistor, compensator and feedback components must be connected as close to the device as possible.

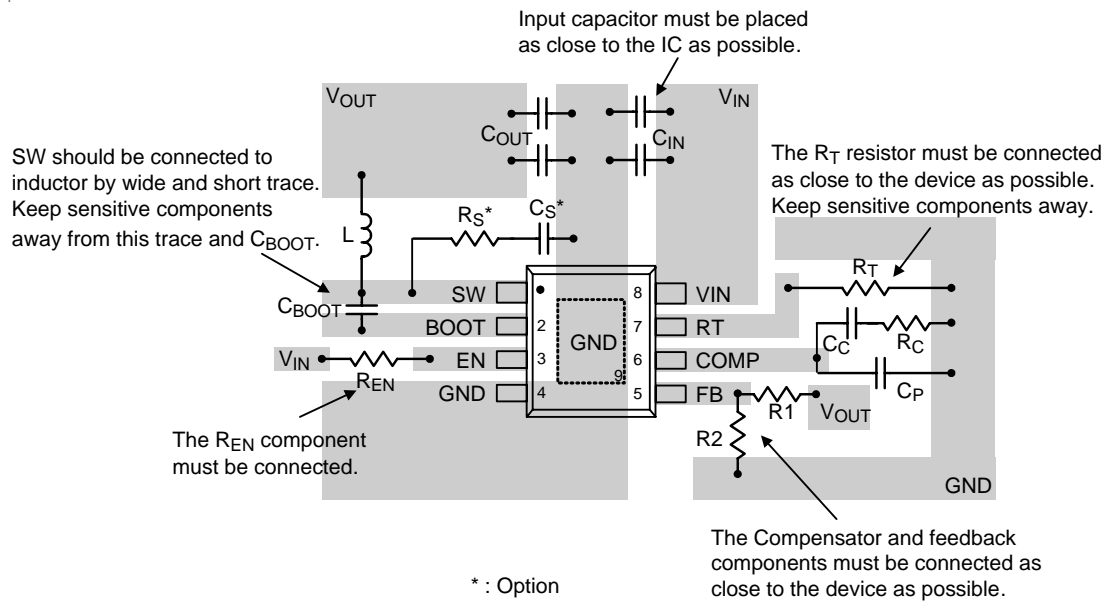
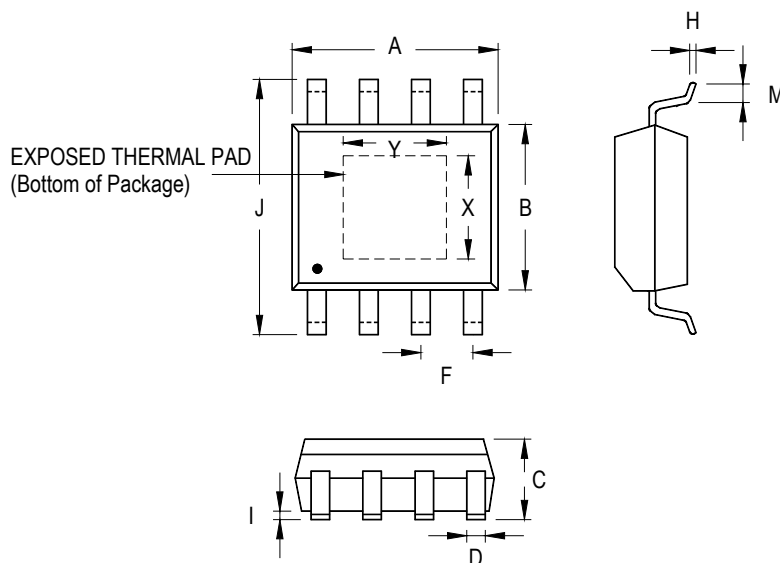


Figure 8. PCB Layout Guide

Table 3. Suggested Capacitors for  $C_{IN}$  and  $C_{OUT}$ 

Location	Component Supplier	Part No.	Capacitance ( $\mu F$ )	Case Size
$C_{IN}$	MURATA	GRM32ER71H475K	4.7	1206
$C_{IN}$	TAIYO YUDEN	UMK325BJ475MM-T	4.7	1206
$C_{IN}$	MURATA	GRM31CR61E106K	10	1206
$C_{IN}$	TDK	C3225X5R1E106K	10	1206
$C_{IN}$	TAIYO YUDEN	TMK316BJ106ML	10	1206
$C_{OUT}$	MURATA	GRM31CR60J476M	47	1206
$C_{OUT}$	TDK	C3225X5R0J476M	47	1210
$C_{OUT}$	MURATA	GRM32ER71C226M	22	1210
$C_{OUT}$	TDK	C3225X5R1C22M	22	1210

# Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

**8-Lead SOP (Exposed Pad) Plastic Package**

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