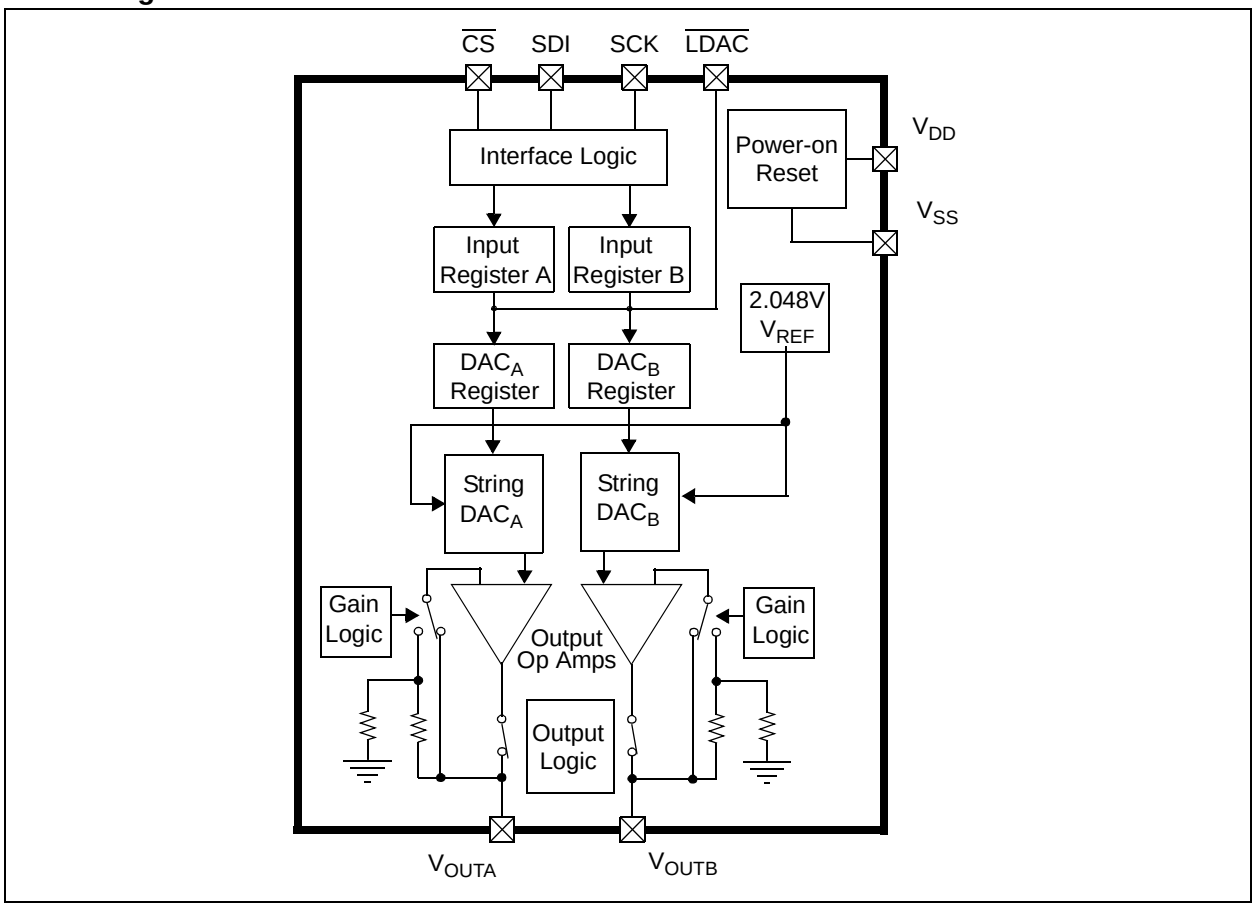
Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD}..... 6.5V
All inputs and outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Current at Input Pins ..... ±2 mA
Current at Supply Pins ..... ±50 mA
Current at Output Pins ..... ±25 mA
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -55°C to +125°C
ESD protection on all pins ≥ 4 kV (HBM), ≥ 400V (MM)
Maximum Junction Temperature (T_J).....+150°C

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Output Buffer Gain (G) = 2x, R_L = 5 kΩ to GND, C_L = 100 pF, T_A = -40 to +85°C. Typical values are at +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Power Requirements						
Input Voltage	V_{DD}	2.7	—	5.5	V	
Input Current	I_{DD}	—	415	750	µA	All digital inputs are grounded, all analog outputs (V_{OUT}) are unloaded. Code = 0x000h
Software Shutdown Current	I_{SHDN_SW}	—	3.3	6	µA	
Power-on Reset Threshold	V_{POR}	—	2.0	—	V	
DC Accuracy						
MCP4802						
Resolution	n	8	—	—	Bits	
INL Error	INL	-1	±0.125	1	LSb	
DNL	DNL	-0.5	±0.1	+0.5	LSb	**Note 1**
MCP4812						
Resolution	n	10	—	—	Bits	
INL Error	INL	-3.5	±0.5	3.5	LSb	
DNL	DNL	-0.5	±0.1	+0.5	LSb	**Note 1**
MCP4822						
Resolution	n	12	—	—	Bits	
INL Error	INL	-12	±2	12	LSb	
DNL	DNL	-0.75	±0.2	+0.75	LSb	**Note 1**
Offset Error	V_{OS}	-1	±0.02	1	% of FSR	Code = 0x000h
Offset Error Temperature Coefficient	V_{OS}/°C	—	0.16	—	ppm/°C	-45°C to +25°C
		—	-0.44	—	ppm/°C	+25°C to +85°C
Gain Error	g_E	-2	-0.10	2	% of FSR	Code = 0xFFFh, not including offset error
Gain Error Temperature Coefficient	ΔG/°C	—	-3	—	ppm/°C	

Note 1: Guaranteed monotonic by design over all codes.
2: This parameter is ensured by design, and not 100% tested.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Output Buffer Gain (G) = 2x, R_L = 5 kΩ to GND, C_L = 100 pF, T_A = -40 to +85°C. Typical values are at +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Internal Voltage Reference (V_{REF})						
Internal Reference Voltage	V_{REF}	2.008	2.048	2.088	V	V_{OUTA} when G = 1x and Code = 0xFFFh
Temperature Coefficient (Note 2)	ΔV_{REF}/°C	—	125	325	ppm/°C	-40°C to 0°C
		—	0.25	0.65	LSb/°C	-40°C to 0°C
		—	45	160	ppm/°C	0°C to +85°C
		—	0.09	0.32	LSb/°C	0°C to +85°C
Output Noise (V_{REF} Noise)	E_{NREF} (0.1-10 Hz)	—	290	—	μV_{p-p}	Code = 0xFFFh, G = 1x
Output Noise Density	e_{NREF} (1 kHz)	—	1.2	—	μV/√Hz	Code = 0xFFFh, G = 1x
	e_{NREF} (10 kHz)	—	1.0	—	μV/√Hz	Code = 0xFFFh, G = 1x
1/f Corner Frequency	f_{CORNER}	—	400	—	Hz	
Output Amplifier						
Output Swing	V_{OUT}	—	0.01 to V_{DD} – 0.04	—	V	Accuracy is better than 1 LSb for V_{OUT} = 10 mV to (V_{DD}–40 mV)
Phase Margin	PM	—	66	—	Degree (°)	C_L= 400 pF, R_L = ∞
Slew Rate	SR	—	0.55	—	V/μs	
Short Circuit Current	I_{SC}	—	15	24	mA	
Settling Time	$t_{SETTLING}$	—	4.5	—	μs	Within 1/2 LSb of final value from 1/4 to 3/4 full-scale range
Dynamic Performance (Note 2)						
DAC-to-DAC Crosstalk		—	<10	—	nV-s	
Major Code Transition Glitch		—	45	—	nV-s	1 LSb change around major carry (`0111...1111` to `1000...0000`)
Digital Feedthrough		—	<10	—	nV-s	
Analog Crosstalk		—	<10	—	nV-s	

Note 1: Guaranteed monotonic by design over all codes.

2: This parameter is ensured by design, and not 100% tested.

ELECTRICAL CHARACTERISTIC WITH EXTENDED TEMPERATURE

Electrical Specifications: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Output Buffer Gain (G) = 2x, R_L = 5 kΩ to GND, C_L = 100 pF. Typical values are at +125°C by characterization or simulation.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Power Requirements						
Input Voltage	V_{DD}	2.7	—	5.5	V	
Input Current	I_{DD}	—	440	—	µA	All digital inputs are grounded, all analog outputs (V_{OUT}) are unloaded. Code = 0x000h.
Software Shutdown Current	I_{SHDN_SW}	—	5	—	µA	
Power-On Reset threshold	V_{POR}	—	1.85	—	V	
DC Accuracy						
MCP4802						
Resolution	n	8	—	—	Bits	
INL Error	INL	—	±0.25	—	LSb	
DNL	DNL	—	±0.2	—	LSb	**Note 1**
MCP4812						
Resolution	n	10	—	—	Bits	
INL Error	INL	—	±1	—	LSb	
DNL	DNL	—	±0.2	—	LSb	**Note 1**
MCP4822						
Resolution	n	12	—	—	Bits	
INL Error	INL	—	±4	—	LSb	
DNL	DNL	—	±0.25	—	LSb	**Note 1**
Offset Error	V_{OS}	—	±0.02	—	% of FSR	Code = 0x000h
Offset Error Temperature Coefficient	V_{OS}/°C	—	-5	—	ppm/°C	+25°C to +125°C
Gain Error	g_E	—	-0.10	—	% of FSR	Code = 0xFFFh, not including offset error
Gain Error Temperature Coefficient	ΔG/°C	—	-3	—	ppm/°C	
Internal Voltage Reference (V_{REF})						
Internal Reference Voltage	V_{REF}	—	2.048	—	V	V_{OUTA} when G = 1x and Code = 0xFFFh
Temperature Coefficient (**Note 2**)	ΔV_{REF}/°C	—	125	—	ppm/°C	-40°C to 0°C
		—	0.25	—	LSb/°C	-40°C to 0°C
		—	45	—	ppm/°C	0°C to +85°C
		—	0.09	—	LSb/°C	0°C to +85°C
Output Noise (V_{REF} Noise)	E_{NREF} (0.1 – 10 Hz)	—	290	—	μV_{p-p}	Code = 0xFFFh, G = 1x
Output Noise Density	e_{NREF} (1 kHz)	—	1.2	—	µV/√Hz	Code = 0xFFFh, G = 1x
	e_{NREF} (10 kHz)	—	1.0	—	µV/√Hz	Code = 0xFFFh, G = 1x
1/f Corner Frequency	f_{CORNER}	—	400	—	Hz	

Note 1: Guaranteed monotonic by design over all codes.

2: This parameter is ensured by design, and not 100% tested.

ELECTRICAL CHARACTERISTIC WITH EXTENDED TEMPERATURE (CONTINUED)

Electrical Specifications: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Output Buffer Gain (G) = 2x, R_L = 5 kΩ to GND, C_L = 100 pF. Typical values are at +125°C by characterization or simulation.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Output Amplifier						
Output Swing	V_{OUT}	—	0.01 to V_{DD} – 0.04	—	V	Accuracy is better than 1 LSb for V_{OUT} = 10 mV to (V_{DD} – 40 mV)
Phase Margin	PM	—	66	—	Degree (°)	C_L = 400 pF, R_L = ∞
Slew Rate	SR	—	0.55	—	V/µs	
Short Circuit Current	I_{SC}	—	17	—	mA	
Settling Time	$t_{SETTLING}$	—	4.5	—	µs	Within 1/2 LSb of final value from 1/4 to 3/4 full-scale range
Dynamic Performance (Note 2)						
DAC-to-DAC Crosstalk		—	<10	—	nV-s	
Major Code Transition Glitch		—	45	—	nV-s	1 LSb change around major carry (`0111...1111` to `1000...0000`)
Digital Feedthrough		—	<10	—	nV-s	
Analog Crosstalk		—	<10	—	nV-s	

Note 1: Guaranteed monotonic by design over all codes.
2: This parameter is ensured by design, and not 100% tested.

AC CHARACTERISTICS (SPI TIMING SPECIFICATIONS)

Electrical Specifications: Unless otherwise indicated, V_{DD} = 2.7V – 5.5V, T_A= -40 to +125°C. Typical values are at +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Schmitt Trigger High-Level Input Voltage (All digital input pins)	V_{IH}	0.7 V_{DD}	—	—	V	
Schmitt Trigger Low-Level Input Voltage (All digital input pins)	V_{IL}	—	—	0.2 V_{DD}	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	0.05 V_{DD}	—	V	
Input Leakage Current	$I_{LEAKAGE}$	-1	—	1	µA	$\overline{LDAC}$ = $\overline{CS}$ = SDI = SCK = V_{DD} or V_{SS}
Digital Pin Capacitance (All inputs/outputs)	C_{IN}, C_{OUT}	—	10	—	pF	V_{DD} = 5.0V, T_A = +25°C, f_{CLK} = 1 MHz **(Note 1)**
Clock Frequency	F_{CLK}	—	—	20	MHz	T_A = +25°C **(Note 1)**
Clock High Time	t_{HI}	15	—	—	ns	**Note 1**
Clock Low Time	t_{LO}	15	—	—	ns	**Note 1**
$\overline{CS}$ Fall to First Rising CLK Edge	t_{CSSR}	40	—	—	ns	Applies only when $\overline{CS}$ falls with CLK high. **(Note 1)**
Data Input Setup Time	t_{SU}	15	—	—	ns	**Note 1**
Data Input Hold Time	t_{HD}	10	—	—	ns	**Note 1**
SCK Rise to $\overline{CS}$ Rise Hold Time	t_{CHS}	15	—	—	ns	**Note 1**

Note 1: This parameter is ensured by design and not 100% tested.

AC CHARACTERISTICS (SPI TIMING SPECIFICATIONS)

Electrical Specifications: Unless otherwise indicated, V_{DD} = 2.7V – 5.5V, T_A= -40 to +125°C. Typical values are at +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ High Time	t_{CSH}	15	—	—	ns	**Note 1**
$\overline{LDAC}$ Pulse Width	t_{LD}	100	—	—	ns	**Note 1**
$\overline{LDAC}$ Setup Time	t_{LS}	40	—	—	ns	**Note 1**
SCK Idle Time before $\overline{CS}$ Fall	t_{IDLE}	40	—	—	ns	**Note 1**

Note 1: This parameter is ensured by design and not 100% tested.

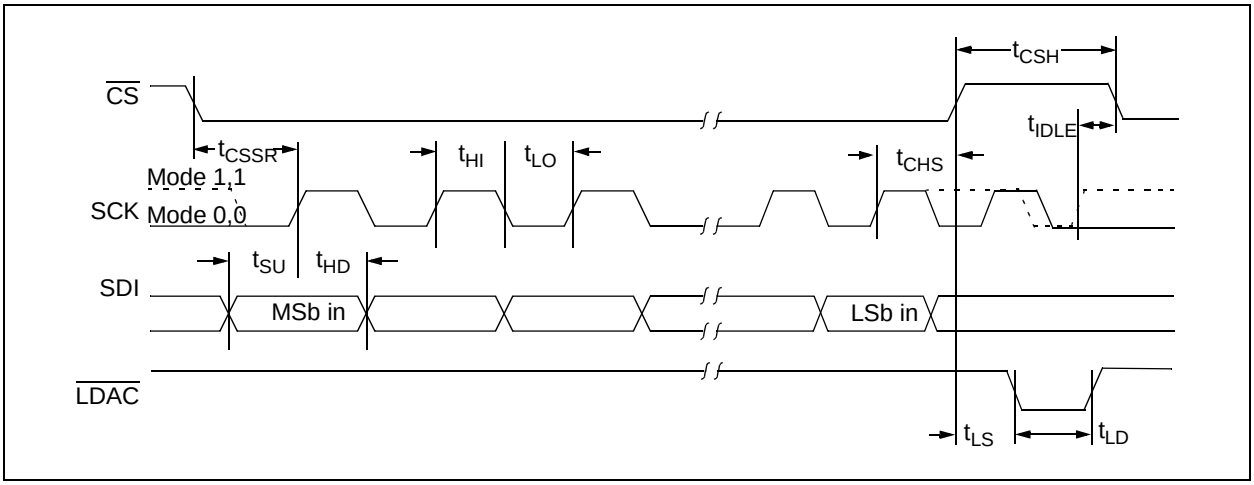


FIGURE 1-1: *SPI Input Timing Data.*

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-MSOP	θ_{JA}	—	211	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	90	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	150	—	°C/W	

Note 1: The MCP4802/4812/4822 devices operate over this extended temperature range, but with reduced performance. Operation in this range must not cause T_J to exceed the maximum junction temperature of +150°C.

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Gain = 2x, R_L = 5 kΩ, C_L = 100 pF.

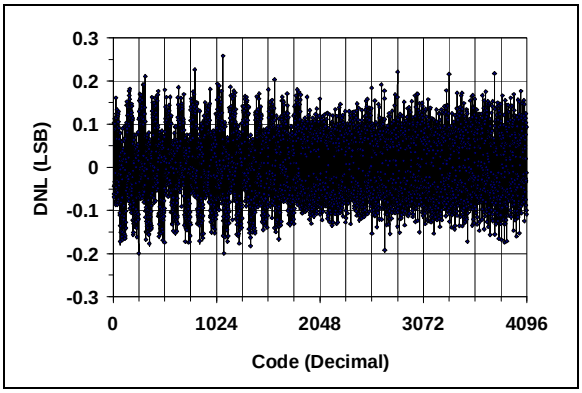


FIGURE 2-1: *DNL vs. Code (MCP4822).*

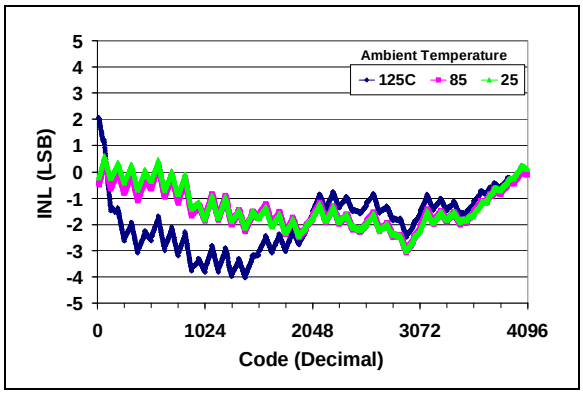


FIGURE 2-4: *INL vs. Code and Temperature (MCP4822).*

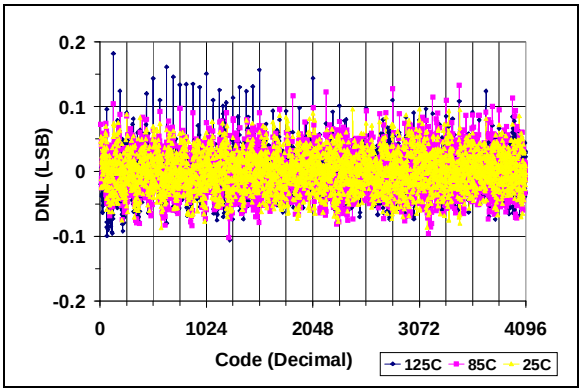


FIGURE 2-2: *DNL vs. Code and Temperature (MCP4822).*

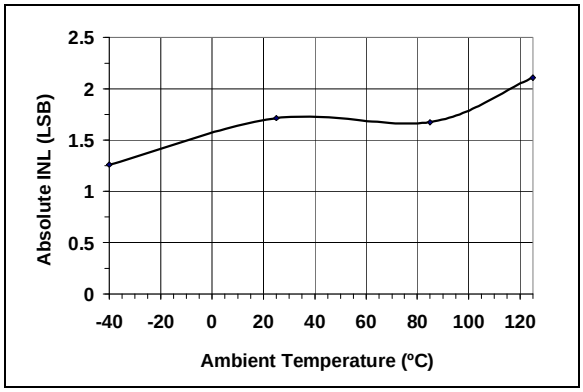


FIGURE 2-5: *Absolute INL vs. Temperature (MCP4822).*

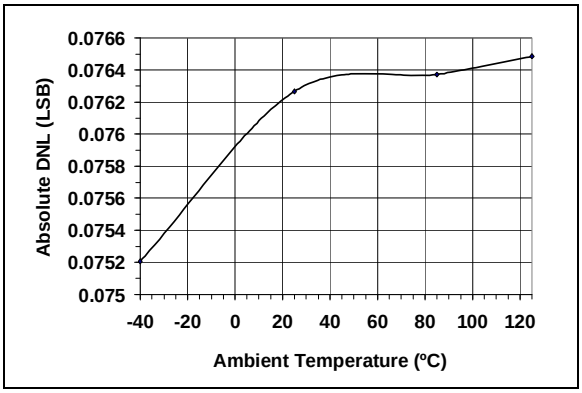


FIGURE 2-3: *Absolute DNL vs. Temperature (MCP4822).*

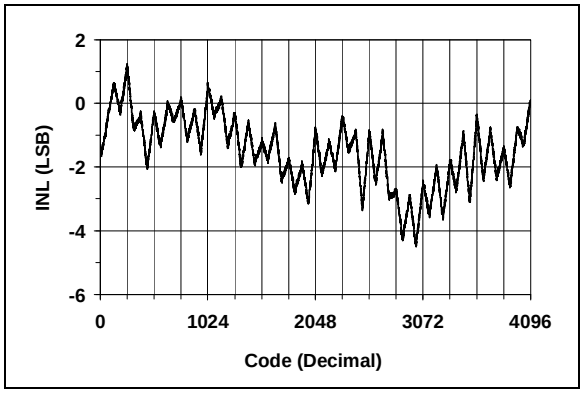


FIGURE 2-6: *INL vs. Code (MCP4822).*

Note: Single device graph for illustration of 64 code effect.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Gain = 2x, R_L = 5 kΩ, C_L = 100 pF.

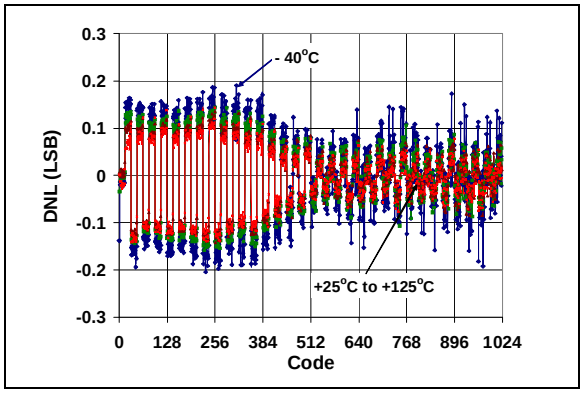


FIGURE 2-7: *DNL vs. Code and Temperature (MCP4812).*

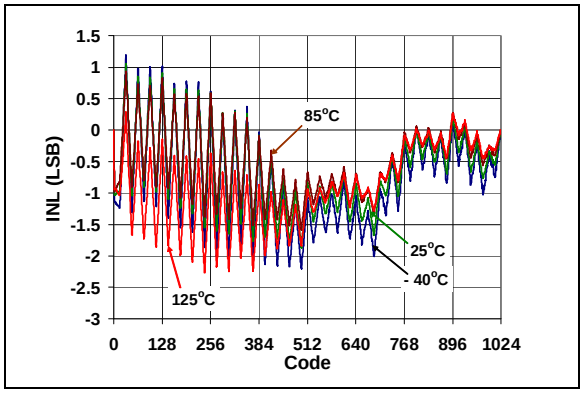


FIGURE 2-8: *INL vs. Code and Temperature (MCP4812).*

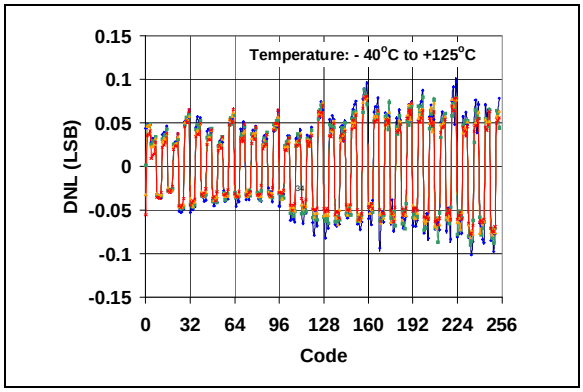


FIGURE 2-9: *DNL vs. Code and Temperature (MCP4802).*

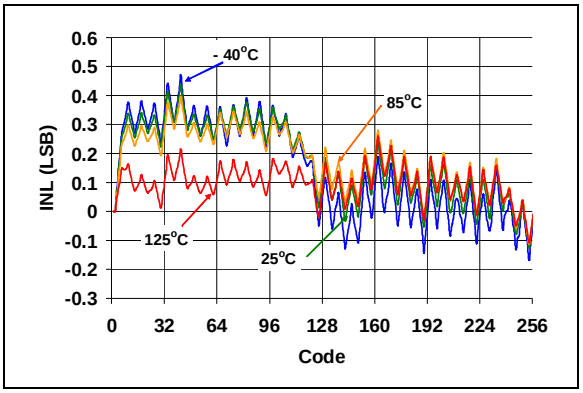


FIGURE 2-10: *INL vs. Code and Temperature (MCP4802).*

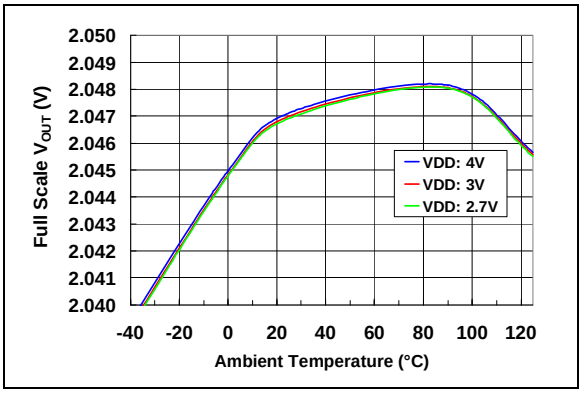


FIGURE 2-11: *Full-Scale V_{OUTA} vs. Ambient Temperature and V_{DD}. Gain = 1x.*

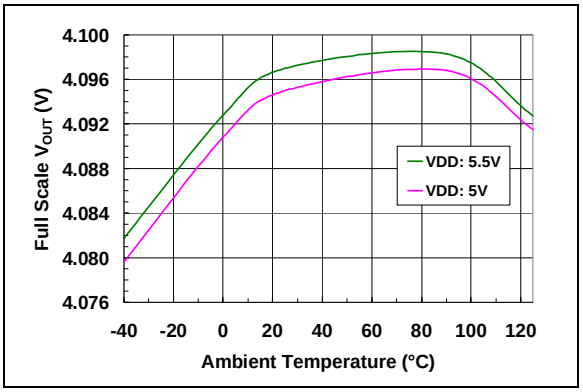


FIGURE 2-12: *Full-Scale V_{OUTA} vs. Ambient Temperature and V_{DD}. Gain = 2x.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Gain = 2x, R_L = 5 kΩ, C_L = 100 pF.

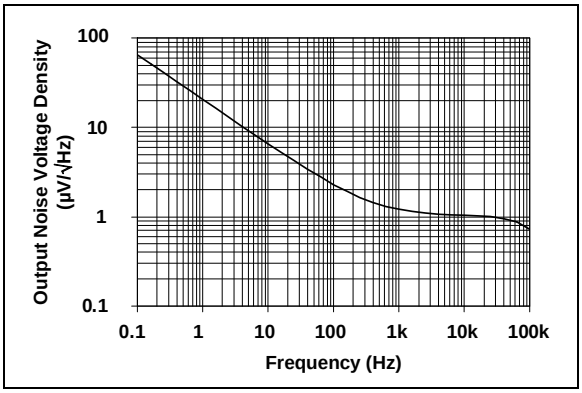


FIGURE 2-13: *Output Noise Voltage Density (V_{REF} Noise Density) vs. Frequency. Gain = 1x.*

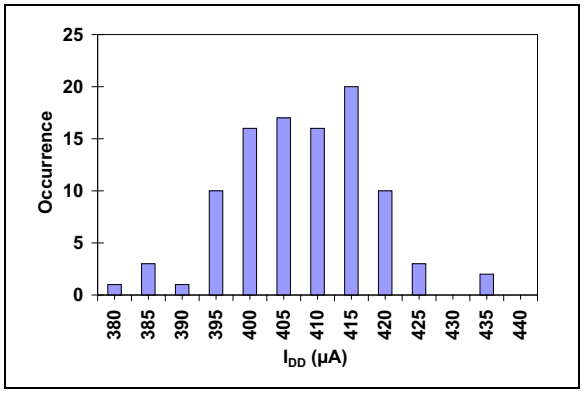


FIGURE 2-16: *I_{DD} Histogram (V_{DD} = 2.7V).*

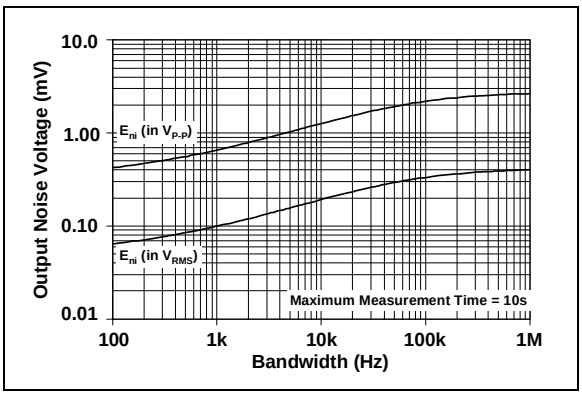


FIGURE 2-14: *Output Noise Voltage (V_{REF} Noise Voltage) vs. Bandwidth. Gain = 1x.*

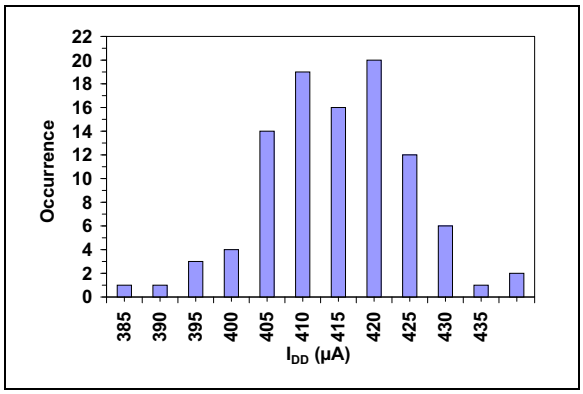


FIGURE 2-17: *I_{DD} Histogram (V_{DD} = 5.0V).*

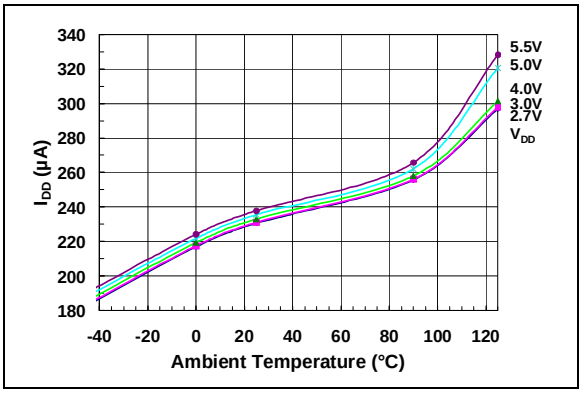


FIGURE 2-15: *I_{DD} vs. Temperature and V_{DD}.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Gain = 2x, R_L = 5 kΩ, C_L = 100 pF.

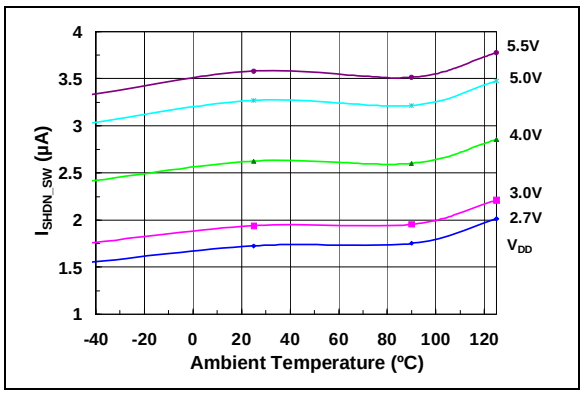


FIGURE 2-18: *Software Shutdown Current vs. Temperature and V_{DD}.*

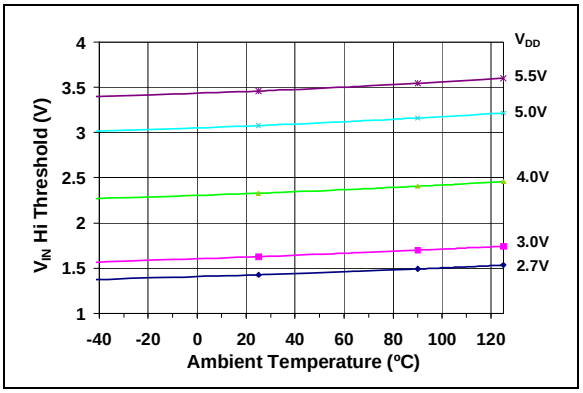


FIGURE 2-21: *V_{IN} High Threshold vs. Temperature and V_{DD}.*

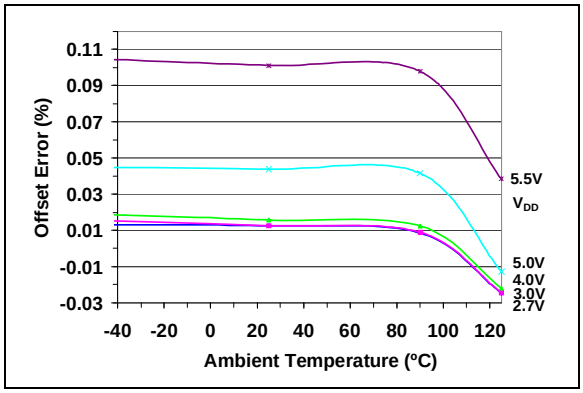


FIGURE 2-19: *Offset Error vs. Temperature and V_{DD}.*

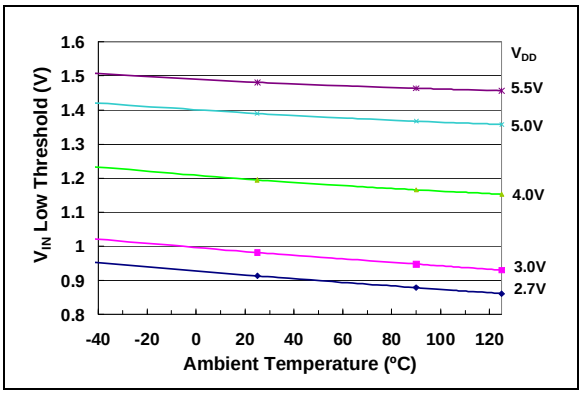


FIGURE 2-22: *V_{IN} Low Threshold vs. Temperature and V_{DD}.*

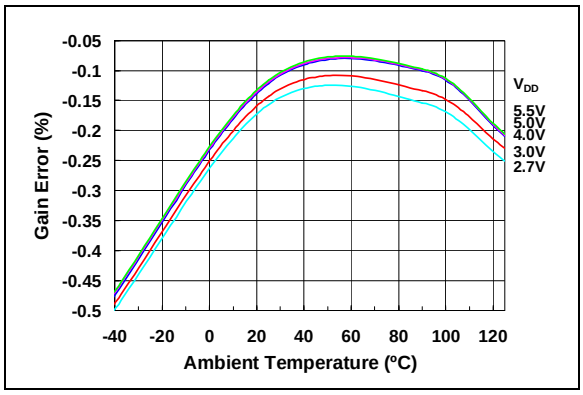


FIGURE 2-20: *Gain Error vs. Temperature and V_{DD}.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Gain = 2x, R_L = 5 kΩ, C_L = 100 pF.

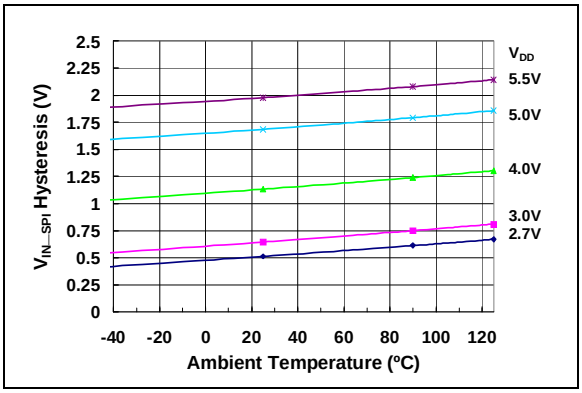


FIGURE 2-23: *Input Hysteresis vs. Temperature and V_{DD}.*

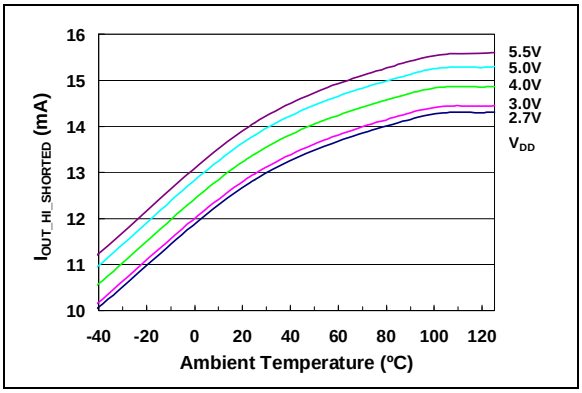


FIGURE 2-26: *I_{OUT} High Short vs. Temperature and V_{DD}.*

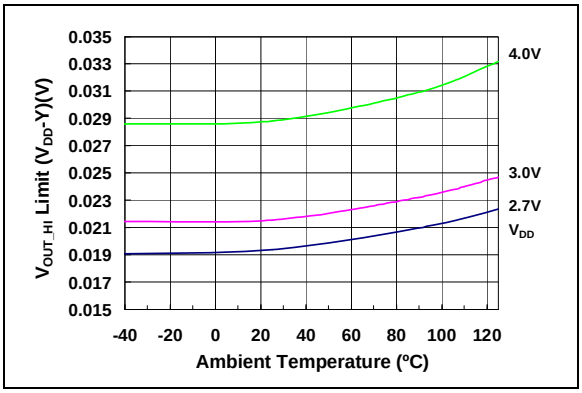


FIGURE 2-24: *V_{OUT} High Limit vs.Temperature and V_{DD}.*

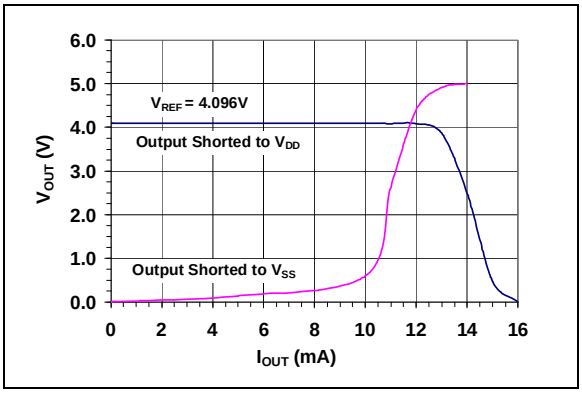


FIGURE 2-27: *I_{OUT} vs. V_{OUT}. Gain = 2x.*

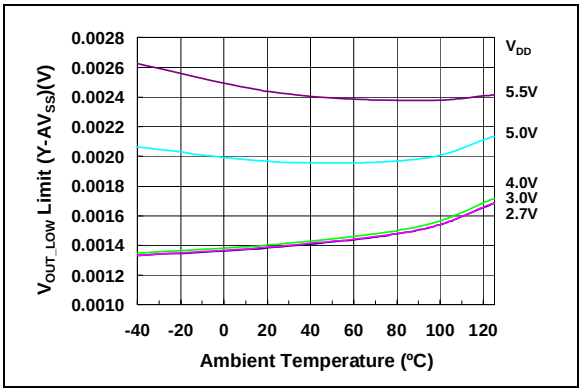


FIGURE 2-25: *V_{OUT} Low Limit vs. Temperature and V_{DD}.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Gain = 2x, R_L = 5 kΩ, C_L = 100 pF.

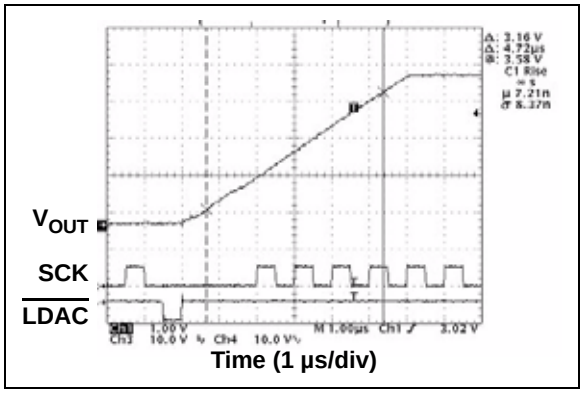


FIGURE 2-28: *V_{OUT} Rise Time.*

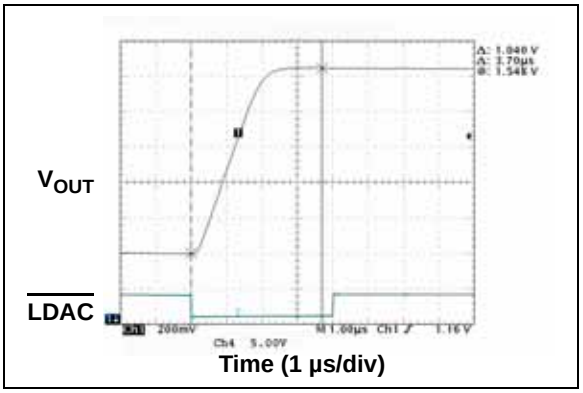


FIGURE 2-31: *V_{OUT} Rise Time.*

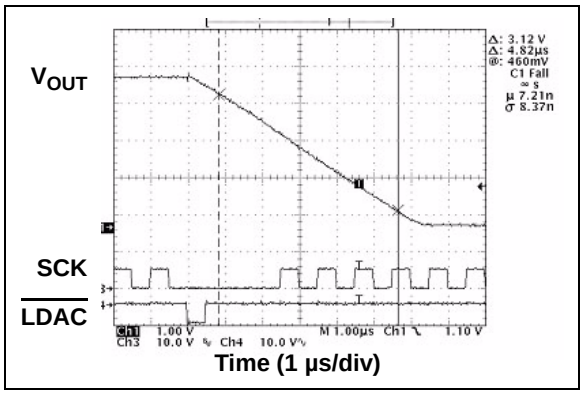


FIGURE 2-29: *V_{OUT} Fall Time.*

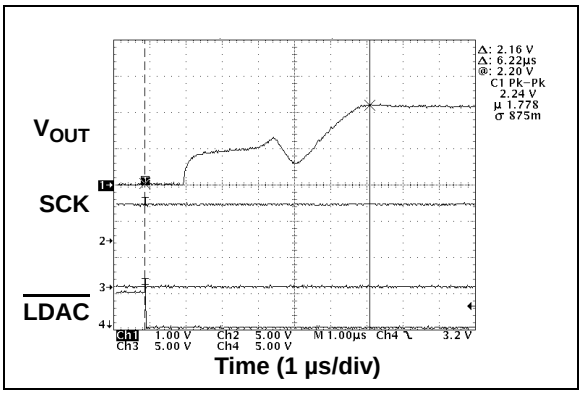


FIGURE 2-32: *V_{OUT} Rise Time Exit Shutdown.*

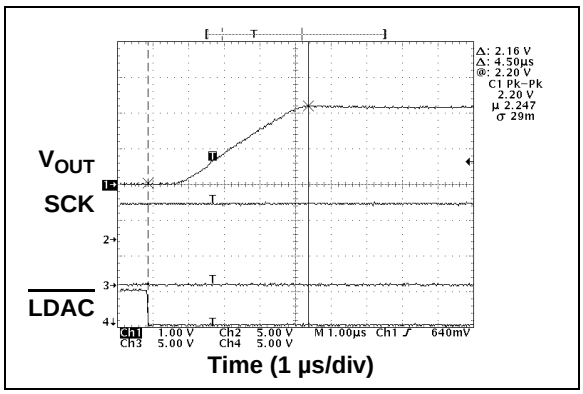


FIGURE 2-30: *V_{OUT} Rise Time.*

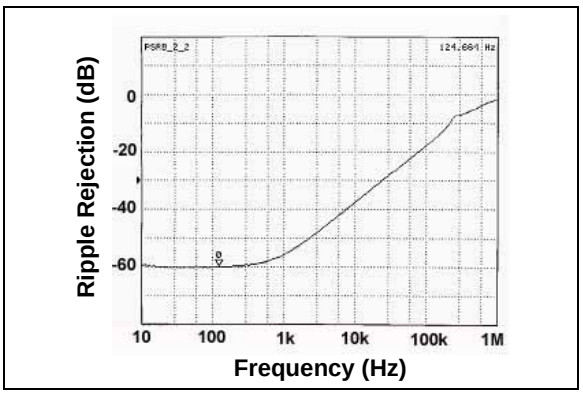


FIGURE 2-33: *PSRR vs. Frequency.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE FOR MCP4802/4812/4822

MCP4802/4812/4822 MSOP, PDIP, SOIC	Symbol	Description
1	V_{DD}	Supply Voltage Input (2.7V to 5.5V)
2	$\overline{CS}$	Chip Select Input
3	SCK	Serial Clock Input
4	SDI	Serial Data Input
5	$\overline{LDAC}$	Synchronization Input. This pin is used to transfer DAC settings (Input Registers) to the output registers (V_{OUT})
6	V_{OUTB}	DAC_B Output
7	V_{SS}	Ground reference point for all circuitry on the device
8	V_{OUTA}	DAC_A Output

3.1 Supply Voltage Pins (V_{DD}, V_{SS})

V_{DD} is the positive supply voltage input pin. The input supply voltage is relative to V_{SS} and can range from 2.7V to 5.5V. The power supply at the V_{DD} pin should be as clean as possible for a good DAC performance. It is recommended to use an appropriate bypass capacitor of about 0.1 µF (ceramic) to ground. An additional 10 µF capacitor (tantalum) in parallel is also recommended to further attenuate high-frequency noise present in application boards.

V_{SS} is the analog ground pin and the current return path of the device. The user must connect the V_{SS} pin to a ground plane through a low-impedance connection. If an analog ground path is available in the application Printed Circuit Board (PCB), it is highly recommended that the V_{SS} pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

3.2 Chip Select ($\overline{CS}$)

$\overline{CS}$ is the Chip Select input pin, which requires an active-low to enable serial clock and data functions.

3.3 Serial Clock Input (SCK)

SCK is the SPI compatible serial clock input pin.

3.4 Serial Data Input (SDI)

SDI is the SPI compatible serial data input pin.

3.5 Latch DAC Input ($\overline{LDAC}$)

$\overline{LDAC}$ (latch DAC synchronization input) pin is used to transfer the input latch registers to their corresponding DAC registers (output latches, V_{OUT}). When this pin is low, both V_{OUTA} and V_{OUTB} are updated at the same time with their input register contents. This pin can be tied to low (V_{SS}) if the V_{OUT} update is desired at the rising edge of the $\overline{CS}$ pin. This pin can be driven by an external control device such as an MCU I/O pin.

3.6 Analog Outputs (V_{OUTA}, V_{OUTB})

V_{OUTA} is the DAC A output pin, and V_{OUTB} is the DAC B output pin. Each output has its own output amplifier. The full-scale range of the DAC output is from V_{SS} to G* V_{REF}, where G is the gain selection option (1x or 2x). The DAC analog output cannot go higher than the supply voltage (V_{DD}).

NOTES:

4.0 GENERAL OVERVIEW

The MCP4802, MCP4812 and MCP4822 are dual voltage output 8-bit, 10-bit and 12-bit DAC devices, respectively. These devices include rail-to-rail output amplifiers, internal voltage reference, shutdown and reset-management circuitry. The devices use an SPI serial communication interface and operate with a single supply voltage from 2.7V to 5.5V.

The DAC input coding of these devices is straight binary. Equation 4-1 shows the DAC analog output voltage calculation.

EQUATION 4-1: ANALOG OUTPUT VOLTAGE (V_{OUT})

$$V_{OUT} = \frac{(2.048V \times D_n)}{2^n} \times G$$

Where:

2.048V	=	Internal voltage reference
D_n	=	DAC input code
G	=	Gain selection
	=	2 for <$\overline{GA}$> bit = 0
	=	1 for <$\overline{GA}$> bit = 1
n	=	DAC Resolution
	=	8 for MCP4802
	=	10 for MCP4812
	=	12 for MCP4822

The ideal output range of each device is:

- **MCP4802 (n = 8)**

(a) 0.0V to 255/256 * 2.048V when gain setting = 1x.

(b) 0.0V to 255/256 * 4.096V when gain setting = 2x.

- **MCP4812 (n = 10)**

(a) 0.0V to 1023/1024 * 2.048V when gain setting = 1x.

(b) 0.0V to 1023/1024 * 4.096V when gain setting = 2x.

- **MCP4822 (n = 12)**

(a) 0.0V to 4095/4096 * 2.048V when gain setting = 1x.

(b) 0.0V to 4095/4096 * 4.096V when gain setting = 2x.

Note: See the output swing voltage specification in **Section 1.0 "Electrical Characteristics"**.

1 LSb is the ideal voltage difference between two successive codes. Table 4-1 illustrates the LSb calculation of each device.

TABLE 4-1: LSb OF EACH DEVICE

Device	Gain Selection	LSb Size
MCP4802 (n = 8)	1x	2.048V/256 = 8 mV
	2x	4.096V/256 = 16 mV
MCP4812 (n = 10)	1x	2.048V/1024 = 2 mV
	2x	4.096V/1024 = 4 mV
MCP4822 (n = 12)	1x	2.048V/4096 = 0.5 mV
	2x	4.096V/4096 = 1 mV

4.0.1 INL ACCURACY

Integral Non-Linearity (INL) error for these devices is the maximum deviation between an actual code transition point and its corresponding ideal transition point once offset and gain errors have been removed. The two end points method (from 0x000 to 0xFFF) is used for the calculation. Figure 4-1 shows the details.

A positive INL error represents transition(s) later than ideal. A negative INL error represents transition(s) earlier than ideal.

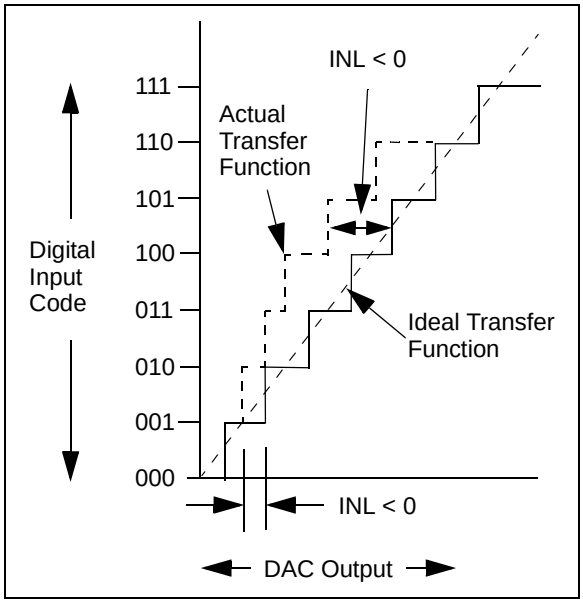


FIGURE 4-1: *Example for INL Error.*

4.0.2 DNL ACCURACY

A Differential Non-Linearity (DNL) error is the measure of variations in code widths from the ideal code width. A DNL error of zero indicates that every code is exactly 1 LSb wide.

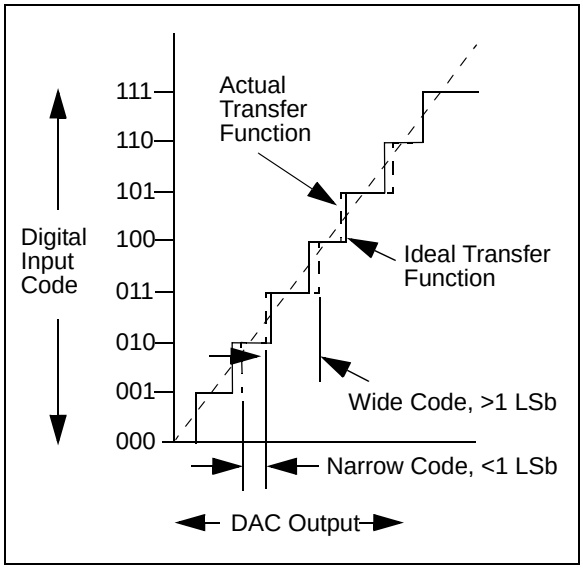


FIGURE 4-2: *Example for DNL Error.*

4.0.3 OFFSET ERROR

An offset error is the deviation from zero voltage output when the digital input code is zero.

4.0.4 GAIN ERROR

A gain error is the deviation from the ideal output, V_{REF} – 1 LSb, excluding the effects of offset error.

4.1 Circuit Descriptions

4.1.1 OUTPUT AMPLIFIERS

The DAC's outputs are buffered with a low-power, precision CMOS amplifier. This amplifier provides low offset voltage and low noise. The output stage enables the device to operate with output voltages close to the power supply rails. Refer to **Section 1.0 "Electrical Characteristics"** for the analog output voltage range and load conditions.

In addition to resistive load-driving capability, the amplifier will also drive high capacitive loads without oscillation. The amplifier's strong outputs allow V_{OUT} to be used as a programmable voltage reference in a system.

4.1.1.1 Programmable Gain Block

The rail-to-rail output amplifier has two configurable gain options: a gain of 1x (<$\overline{GA}$> = 1) or a gain of 2x (<$\overline{GA}$> = 0). The default value for this bit is a gain of 2 (<$\overline{GA}$> = 0). This results in an ideal full-scale output of 0.000V to 4.096V due to the internal reference (V_{REF} = 2.048V).

4.1.2 VOLTAGE REFERENCE

The MCP4802/4812/4822 devices utilize internal 2.048V voltage reference. The voltage reference has a low temperature coefficient and low noise characteristics. Refer to **Section 1.0 "Electrical Characteristics"** for the voltage reference specifications.

4.1.3 POWER-ON RESET CIRCUIT

The internal Power-on Reset (POR) circuit monitors the power supply voltage (V_{DD}) during the device operation. The circuit also ensures that the DAC powers up with high output impedance (<SHDN> = 0, typically 500 kΩ). The devices will continue to have a high-impedance output until a valid write command is received and the LDAC pin meets the input low threshold.

If the power supply voltage is less than the POR threshold (V_{POR} = 2.0V, typical), the DACs will be held in their Reset state. The DACs will remain in that state until $V_{DD} > V_{POR}$ and a subsequent write command is received.

Figure 4-3 shows a typical power supply transient pulse and the duration required to cause a reset to occur, as well as the relationship between the duration and trip voltage. A 0.1 µF decoupling capacitor, mounted as close as possible to the V_{DD} pin, can provide additional transient immunity.

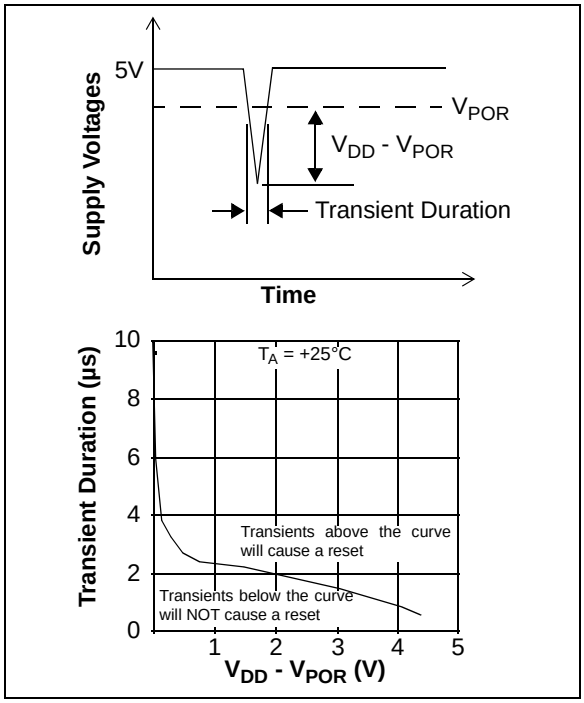


FIGURE 4-3: *Typical Transient Response.*

4.1.4 SHUTDOWN MODE

The user can shut down each DAC channel selectively using a software command (<SHDN> = 0). During Shutdown mode, most of the internal circuits in the channel that was shut down are turned off for power savings. The internal reference is not affected by the shutdown command. The serial interface also remains active, thus allowing a write command to bring the device out of the Shutdown mode. There will be no analog output at the channel that was shut down and the V_{OUT} pin is internally switched to a known resistive load (500 kΩ, typical). Figure 4-4 shows the analog output stage during the Shutdown mode.

The device will remain in Shutdown mode until the <SHDN> bit = 1 is latched into the device. When a DAC channel is changed from Shutdown to Active mode, the output settling time takes < 10 µs, but greater than the standard active mode settling time (4.5 µs).

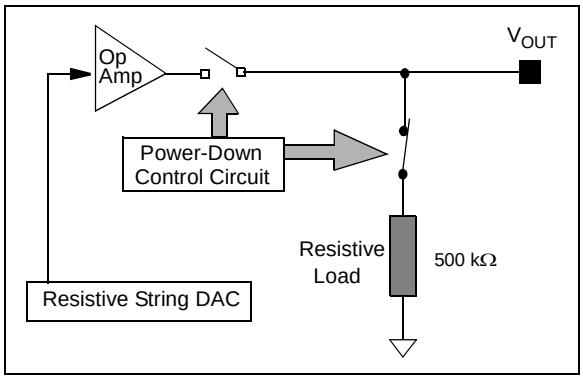


FIGURE 4-4: *Output Stage for Shutdown Mode.*

NOTES:

5.0 SERIAL INTERFACE

5.1 Overview

The MCP4802/4812/4822 devices are designed to interface directly with the Serial Peripheral Interface (SPI) port, available on many microcontrollers, and supports Mode 0,0 and Mode 1,1. Commands and data are sent to the device via the SDI pin, with data being clocked-in on the rising edge of SCK. The communications are unidirectional and, thus, data cannot be read out of the MCP4802/4812/4822 devices. The $\overline{CS}$ pin must be held low for the duration of a write command. The write command consists of 16 bits and is used to configure the DAC's control and data latches. Register 5-1 to Register 5-3 detail the input register that is used to configure and load the DAC_A and DAC_B registers for each device. Figure 5-1 to Figure 5-3 show the write command for each device.

Refer to Figure 1-1 and SPI Timing Specifications Table for detailed input and output timing specifications for both Mode 0,0 and Mode 1,1 operation.

5.2 Write Command

The write command is initiated by driving the $\overline{CS}$ pin low, followed by clocking the four Configuration bits and the 12 data bits into the SDI pin on the rising edge of SCK. The $\overline{CS}$ pin is then raised, causing the data to be latched into the selected DAC's input registers.

The MCP4802/4812/4822 devices utilize a double-buffered latch structure to allow both DAC_A's and DAC_B's outputs to be synchronized with the $\overline{LDAC}$ pin, if desired.

By bringing down the $\overline{LDAC}$ pin to a low state, the contents stored in the DAC's input registers are transferred into the DAC's output registers (V_{OUT}), and both V_{OUTA} and V_{OUTB} are updated at the same time.

All writes to the MCP4802/4812/4822 devices are 16-bit words. Any clocks after the first 16^{th} clock will be ignored. The Most Significant four bits are Configuration bits. The remaining 12 bits are data bits. No data can be transferred into the device with $\overline{CS}$ high. The data transfer will only occur if 16 clocks have been transferred into the device. If the rising edge of $\overline{CS}$ occurs prior, shifting of data into the input registers will be aborted.

REGISTER 5-1: WRITE COMMAND REGISTER FOR MCP4822 (12-BIT DAC)

W-x	W-x	W-x	W-0	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
$\overline{A}$/B	—	$\overline{GA}$	$\overline{SHDN}$	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
bit 15															bit 0

REGISTER 5-2: WRITE COMMAND REGISTER FOR MCP4812 (10-BIT DAC)

W-x	W-x	W-x	W-0	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
$\overline{A}$/B	—	$\overline{GA}$	$\overline{SHDN}$	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	x	x
bit 15															bit 0

REGISTER 5-3: WRITE COMMAND REGISTER FOR MCP4802 (8-BIT DAC)

W-x	W-x	W-x	W-0	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
$\overline{A}$/B	—	$\overline{GA}$	$\overline{SHDN}$	D7	D6	D5	D4	D3	D2	D1	D0	x	x	x	x
bit 15															bit 0

Where:

bit 15 **$\overline{A}$/B:** DAC_A or DAC_B Selection bit
- 1 = Write to DAC_B
- 0 = Write to DAC_A

bit 14 — Don't Care

bit 13 **$\overline{GA}$:** Output Gain Selection bit
- 1 = 1x ($V_{OUT} = V_{REF} * D/4096$)
- 0 = 2x ($V_{OUT} = 2 * V_{REF} * D/4096$), where internal V_{REF} = 2.048V.

bit 12 **$\overline{SHDN}$:** Output Shutdown Control bit
- 1 = Active mode operation. V_{OUT} is available.
- 0 = Shutdown the selected DAC channel. Analog output is not available at the channel that was shut down. V_{OUT} pin is connected to 500 kΩ (typical).

bit 11-0 **D11:D0:** DAC Input Data bits. Bit x is ignored.

Legend			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

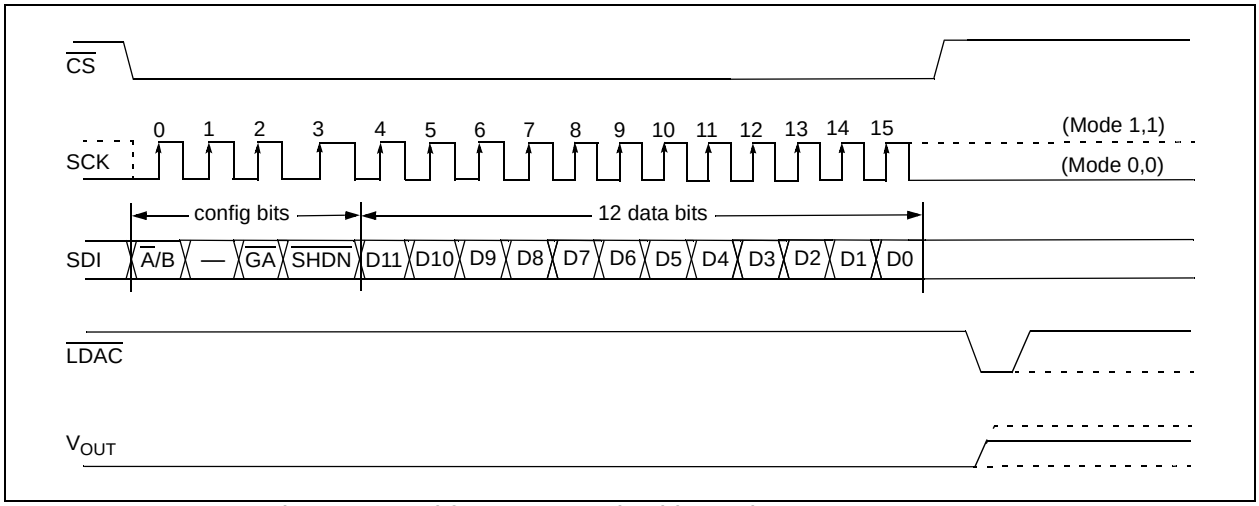
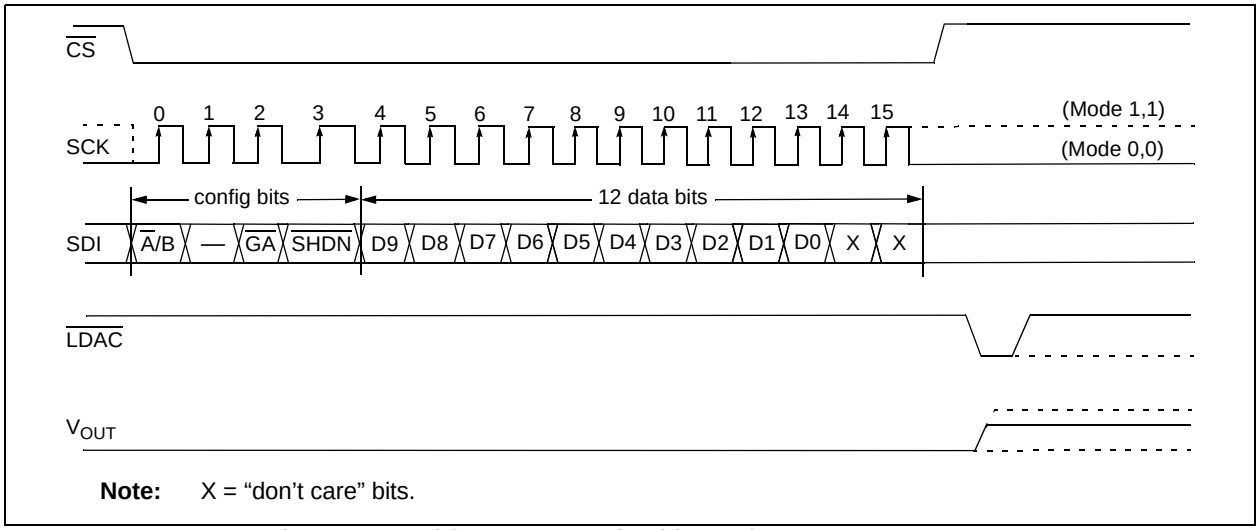
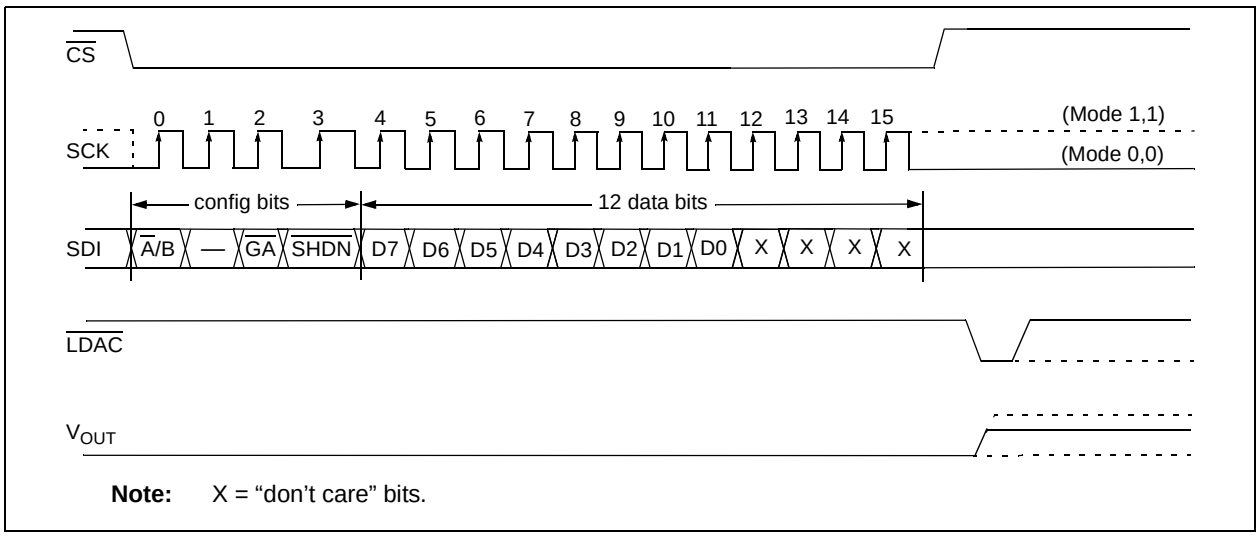


FIGURE 5-1: *Write Command for MCP4822 (12-bit DAC).*



Note: X = “don’t care” bits.

FIGURE 5-2: *Write Command for MCP4812 (10-bit DAC).*



Note: X = “don’t care” bits.

FIGURE 5-3: *Write Command for MCP4802 (8-bit DAC).*

NOTES:

6.0 TYPICAL APPLICATIONS

The MCP4802/4812/4822 family of devices are general purpose DACs for various applications where a precision operation with low-power and internal voltage reference is required.

Applications generally suited for the devices are:

- Set Point or Offset Trimming
- Sensor Calibration
- Precision Selectable Voltage Reference
- Portable Instrumentation (Battery-Powered)
- Calibration of Optical Communication Devices

6.1 Digital Interface

The MCP4802/4812/4822 devices utilize a 3-wire synchronous serial protocol to transfer the DAC's setup and input codes from the digital devices. The serial protocol can be interfaced to SPI or Microwire peripherals that is common on many microcontroller units (MCUs), including Microchip's PIC® MCUs and dsPIC® DSCs.

In addition to the three serial connections ($\overline{CS}$, SCK and SDI), the $\overline{LDAC}$ signal synchronizes the two DAC outputs. By bringing down the $\overline{LDAC}$ pin to "low", all DAC input codes and settings in the two DAC input registers are latched into their DAC output registers at the same time. Therefore, both DAC_A and DAC_B outputs are updated at the same time. Figure 6-1 shows an example of the pin connections. Note that the $\overline{LDAC}$ pin can be tied low (V_{SS}) to reduce the required connections from four to three I/O pins. In this case, the DAC output can be immediately updated when a valid 16 clock transmission has been received and the $\overline{CS}$ pin has been raised.

6.2 Power Supply Considerations

The typical application will require a bypass capacitor in order to filter out the noise in the power supply traces. The noise can be induced onto the power supply's traces from various events such as digital switching or as a result of changes on the DAC's output. The bypass capacitor helps to minimize the effect of these noise sources. Figure 6-1 illustrates an appropriate bypass strategy. In this example, two bypass capacitors are used in parallel: (a) 0.1 µF (ceramic) and (b)10 µF (tantalum). These capacitors should be placed as close to the device power pin (V_{DD}) as possible (within 4 mm).

The power source supplying these devices should be as clean as possible. If the application circuit has separate digital and analog power supplies, V_{DD} and V_{SS} of the device should reside on the analog plane.

6.3 Output Noise Considerations

The voltage noise density (in µV/√Hz) is illustrated in Figure 2-13. This noise appears at V_{OUTX}, and is primarily a result of the internal reference voltage. Its 1/f corner (f_{CORNER}) is approximately 400 Hz.

Figure 2-14 illustrates the voltage noise (in mV_{RMS} or mV_{P-P}). A small bypass capacitor on V_{OUTX} is an effective method to produce a single-pole Low-Pass Filter (LPF) that will reduce this noise. For instance, a bypass capacitor sized to produce a 1 kHz LPF would result in an E_{NREF} of about 100 μV_{RMS}. This would be necessary when trying to achieve the low DNL error performance (at G = 1) that the MCP4802/4812/4822 devices are capable of. The tested range for stability is .001µF through 4.7 µF.

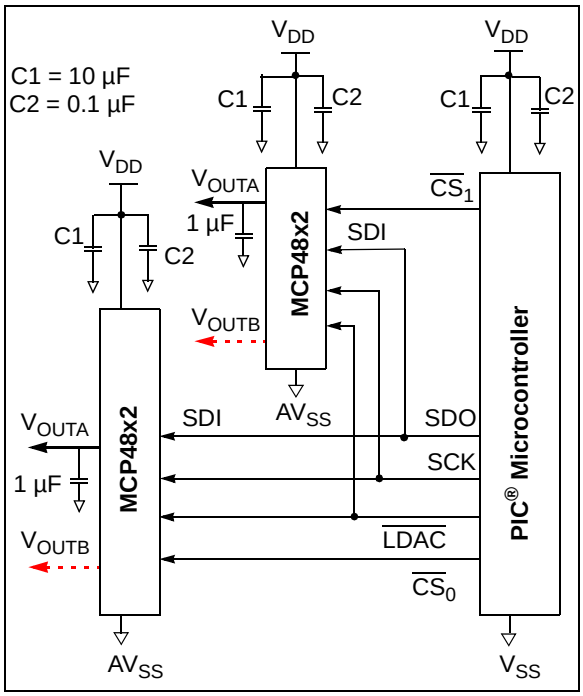


FIGURE 6-1: *Typical Connection Diagram.*

6.4 Layout Considerations

Inductively-coupled AC transients and digital switching noises can degrade the output signal integrity, and potentially reduce the device performance. Careful board layout will minimize these effects and increase the Signal-to-Noise Ratio (SNR). Bench testing has shown that a multi-layer board utilizing a low-inductance ground plane, isolated inputs and isolated outputs with proper decoupling, is critical for the best performance. Particularly harsh environments may require shielding of critical signals.

Breadboards and wire-wrapped boards are not recommended if low noise is desired.

6.5 Single-Supply Operation

The MCP4802/4812/4822 family of devices are rail-to-rail voltage output DAC devices designed to operate with a V_{DD} range of 2.7V to 5.5V. Its output amplifier is robust enough to drive small-signal loads directly. Therefore, it does not require any external output buffer for most applications.

6.5.1 DC SET POINT OR CALIBRATION

A common application for the devices is a digitally-controlled set point and/or calibration of variable parameters, such as sensor offset or slope. For example, the MCP4822 provides 4096 output steps. If G = 1 is selected, the internal 2.048V V_{REF} would produce 500 µV of resolution. If G = 2 is selected, the internal 2.048 V_{REF} would produce 1 mV of resolution.

6.5.1.1 Decreasing Output Step Size

If the application is calibrating the bias voltage of a diode or transistor, a bias voltage range of 0.8V may be desired with about 200 µV resolution per step. Two common methods to achieve a 0.8V range are to either reduce V_{REF} to 0.82V (using the MCP49XX family device that uses external reference) or use a voltage divider on the DAC's output.

Using a V_{REF} is an option if the V_{REF} is available with the desired output voltage range. However, occasionally, when using a low-voltage V_{REF}, the noise floor causes SNR error that is intolerable. Using a voltage divider method is another option and provides some advantages when V_{REF} needs to be very low or when the desired output voltage is not available. In this case, a larger value V_{REF} is used while two resistors scale the output range down to the precise desired level.

Example 6-1 illustrates this concept. Note that the bypass capacitor on the output of the voltage divider plays a critical function in attenuating the output noise of the DAC and the induced noise from the environment.

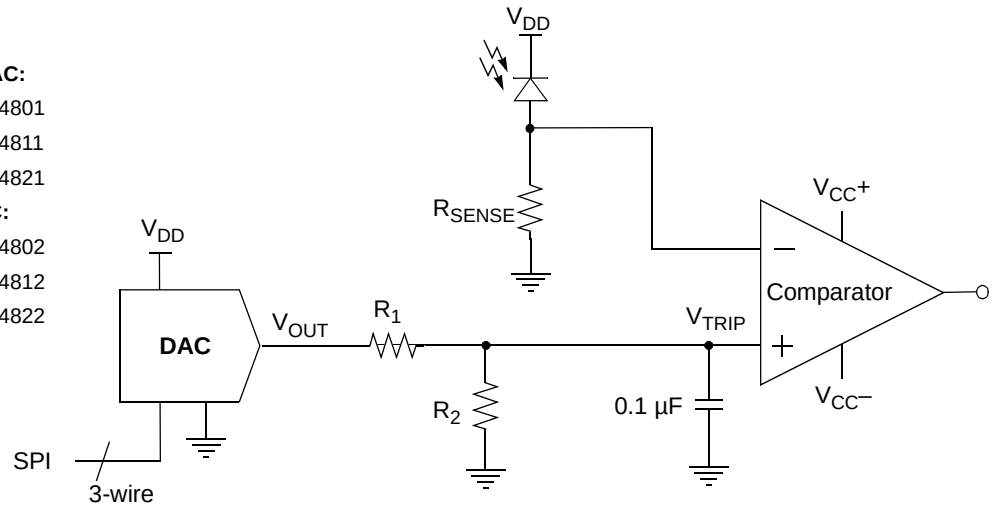
EXAMPLE 6-1: EXAMPLE CIRCUIT OF SET POINT OR THRESHOLD CALIBRATION

(a) Single Output DAC:

MCP4801
MCP4811
MCP4821

(b) Dual Output DAC:

MCP4802
MCP4812
MCP4822



$$V_{OUT} = 2.048 \cdot G \cdot \frac{D_n}{2^N}$$

$$V_{trip} = V_{OUT}\left(\frac{R_2}{R_1 + R_2}\right)$$

G	=	Gain selection (1x or 2x)
D_n	=	Digital value of DAC (0-255) for MCP4801/MCP4802
	=	Digital value of DAC (0-1023) for MCP4811/MCP4812
	=	Digital value of DAC (0-4095) for MCP4821/MCP4822
N	=	DAC bit resolution

6.5.1.2 Building a “Window” DAC

When calibrating a set point or threshold of a sensor, typically only a small portion of the DAC output range is utilized. If the LSb size is adequate enough to meet the application’s accuracy needs, the unused range is sacrificed without consequences. If greater accuracy is needed, then the output range will need to be reduced to increase the resolution around the desired threshold.

If the threshold is not near V_{REF}, $2V_{REF}$ or V_{SS}, then creating a “window” around the threshold has several advantages. One simple method to create this “window” is to use a voltage divider network with a pull-up and pull-down resistor. Example 6-2 shows this concept.

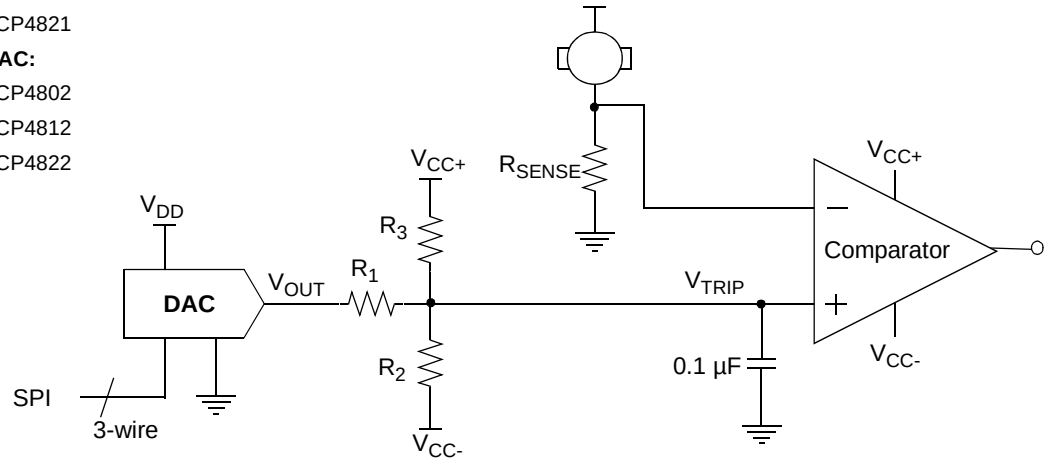
EXAMPLE 6-2: SINGLE-SUPPLY “WINDOW” DAC

(a) Single Output DAC:

MCP4801
MCP4811
MCP4821

(b) Dual Output DAC:

MCP4802
MCP4812
MCP4822



$$V_{OUT} = 2.048 \cdot G \cdot \frac{D_n}{2^N}$$

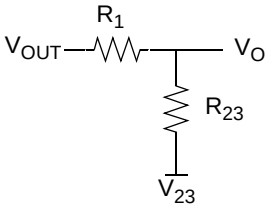
G	=	Gain selection (1x or 2x)
D_n	=	Digital value of DAC (0-255) for MCP4801/MCP4802
	=	Digital value of DAC (0-1023) for MCP4811/MCP4812
	=	Digital value of DAC (0-4095) for MCP4821/MCP4822
N	=	DAC bit resolution

Thevenin Equivalent

$$R_{23} = \frac{R_2 R_3}{R_2 + R_3}$$

$$V_{23} = \frac{(V_{CC+} R_2) + (V_{CC-} R_3)}{R_2 + R_3}$$

$$V_{trip} = \frac{V_{OUT} R_{23} + V_{23} R_1}{R_1 + R_{23}}$$



6.6 Bipolar Operation

Bipolar operation is achievable using the MCP4802/4812/4822 family of devices by utilizing an external operational amplifier (op amp). This configuration is desirable due to the wide variety and availability of op amps. This allows a general purpose DAC, with its cost and availability advantages, to meet almost any desired output voltage range, power and noise performance.

Example 6-3 illustrates a simple bipolar voltage source configuration. R_1 and R_2 allow the gain to be selected, while R_3 and R_4 shift the DAC's output to a selected offset. Note that R4 can be tied to V_{DD}, instead of V_{SS}, if a higher offset is desired. Also note that a pull-up to V_{DD} could be used instead of R_4, or in addition to R_4, if a higher offset is desired.

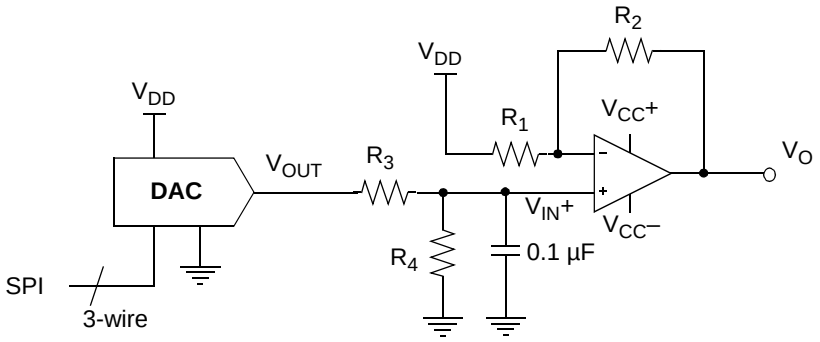
EXAMPLE 6-3: DIGITALLY-CONTROLLED BIPOLAR VOLTAGE SOURCE

(a) Single Output DAC:

MCP4801
MCP4811
MCP4821

(b) Dual Output DAC:

MCP4802
MCP4812
MCP4822



$$V_{OUT} = 2.048 \cdot G \cdot \frac{D_n}{2^N}$$

$$V_{IN+} = \frac{V_{OUT} R_4}{R_3 + R_4}$$

$$V_O = V_{IN+}\left(1 + \frac{R_2}{R_1}\right) - V_{DD}\left(\frac{R_2}{R_1}\right)$$

G	=	Gain selection (1x or 2x)
D_n	=	Digital value of DAC (0-255) for MCP4801/MCP4802
	=	Digital value of DAC (0-1023) for MCP4811/MCP4812
	=	Digital value of DAC (0-4095) for MCP4821/MCP4822
N	=	DAC bit resolution

6.6.1 DESIGN EXAMPLE: DESIGN A BIPOLAR DAC USING Example 6-3 WITH 12-BIT MCP4822 OR MCP4821

An output step magnitude of 1 mV, with an output range of ±2.05V, is desired for a particular application.

Step 1: Calculate the range: +2.05V – (-2.05V) = 4.1V.

Step 2: Calculate the resolution needed:

4.1V/1 mV = 4100

Since 2^{12} = 4096, 12-bit resolution is desired.

Step 3: The amplifier gain (R_2/R_1), multiplied by full-scale V_{OUT} (4.096V), must be equal to the desired minimum output to achieve bipolar operation. Since any gain can be realized by choosing resistor values (R_1+R_2), the V_{REF} value must be selected first. If a V_{REF} of 4.096V is used (G=2), solve for the amplifier's gain by setting the DAC to 0, knowing that the output needs to be -2.05V.

The equation can be simplified to:

$$\frac{-R_2}{R_1} = \frac{-2.05}{4.096V} \qquad \frac{R_2}{R_1} = \frac{1}{2}$$

If R_1 = 20 kΩ and R_2 = 10 kΩ, the gain will be 0.5.

Step 4: Next, solve for R_3 and R_4 by setting the DAC to 4096, knowing that the output needs to be +2.05V.

$$\frac{R_4}{(R_3 + R_4)} = \frac{2.05V + (0.5 \cdot 4.096V)}{1.5 \cdot 4.096V} = \frac{2}{3}$$

If R_4 = 20 kΩ, then R_3 = 10 kΩ

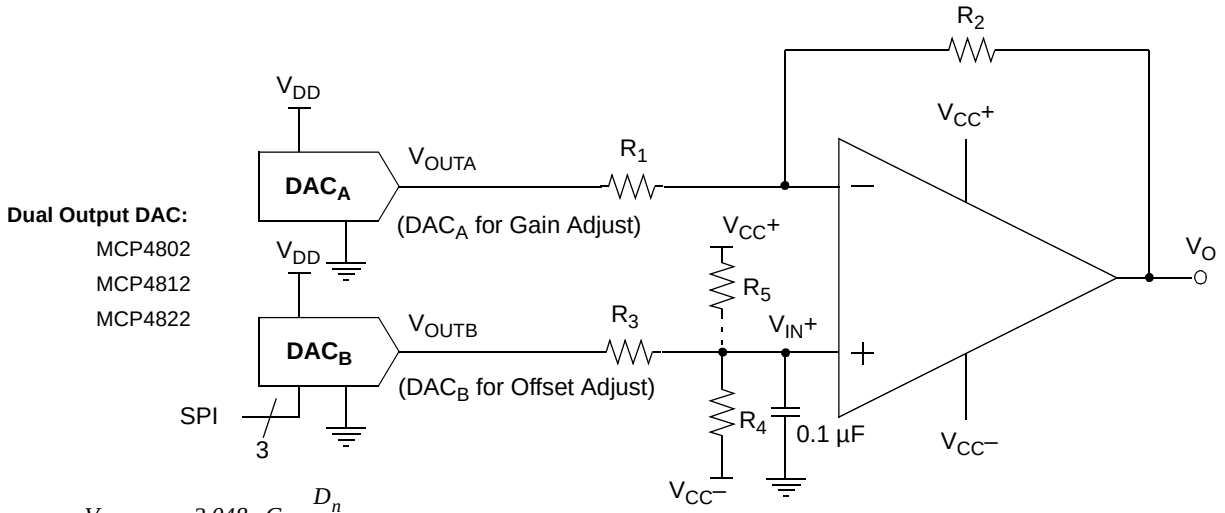
6.7 Selectable Gain and Offset Bipolar Voltage Output Using a Dual Output DAC

In some applications, precision digital control of the output range is desirable. Example 6-4 illustrates how to use the MCP4802/4812/4822 family of devices to achieve this in a bipolar or single-supply application.

This circuit is typically used for linearizing a sensor whose slope and offset varies.

The equation to design a bipolar "window" DAC would be utilized if R_3, R_4 and R_5 are populated.

EXAMPLE 6-4: BIPOLAR VOLTAGE SOURCE WITH SELECTABLE GAIN AND OFFSET



$$V_{OUTA} = 2.048 \cdot G_A \cdot \frac{D_n}{2^N}$$

$$V_{OUTB} = 2.048 \cdot G_B \cdot \frac{D_n}{2^N}$$

$$V_{IN+} = \frac{V_{OUTB}R_4 + V_{CC-}R_3}{R_3 + R_4}$$

$$V_O = \underbrace{V_{IN+}\left(1 + \frac{R_2}{R_1}\right)}_{\text{Offset Adjust}} - \underbrace{V_{OUTA}\left(\frac{R_2}{R_1}\right)}_{\text{Gain Adjust}}$$

G	=	Gain selection (1x or 2x)
N	=	DAC bit resolution
D_A, D_B	=	Digital value of DAC (0-255) for MCP4802
	=	Digital value of DAC (0-1023) for MCP4812
	=	Digital value of DAC (0-4095) for MCP4822

Bipolar "Window" DAC using R_4 and R_5

Thevenin Equivalent

$$V_{45} = \frac{V_{CC+}R_4 + V_{CC-}R_5}{R_4 + R_5} \qquad R_{45} = \frac{R_4R_5}{R_4 + R_5}$$

$$V_{IN+} = \frac{V_{OUTB}R_{45} + V_{45}R_3}{R_3 + R_{45}} \qquad V_O = \underbrace{V_{IN+}\left(1 + \frac{R_2}{R_1}\right)}_{\text{Offset Adjust}} - \underbrace{V_{OUTA}\left(\frac{R_2}{R_1}\right)}_{\text{Gain Adjust}}$$

6.8 Designing a Double-Precision DAC Using a Dual DAC

Example 6-5 illustrates how to design a single-supply voltage output capable of up to 24-bit resolution from a dual 12-bit DAC (MCP4822). This design is simply a voltage divider with a buffered output.

As an example, if an application similar to the one developed in **Section 6.6.1 "Design Example: Design a Bipolar DAC Using Example 6-3 with 12-bit MCP4822 or MCP4821"** required a resolution of 1 µV instead of 1 mV, and a range of 0V to 4.1V, then 12-bit resolution would not be adequate.

Step 1: Calculate the resolution needed:

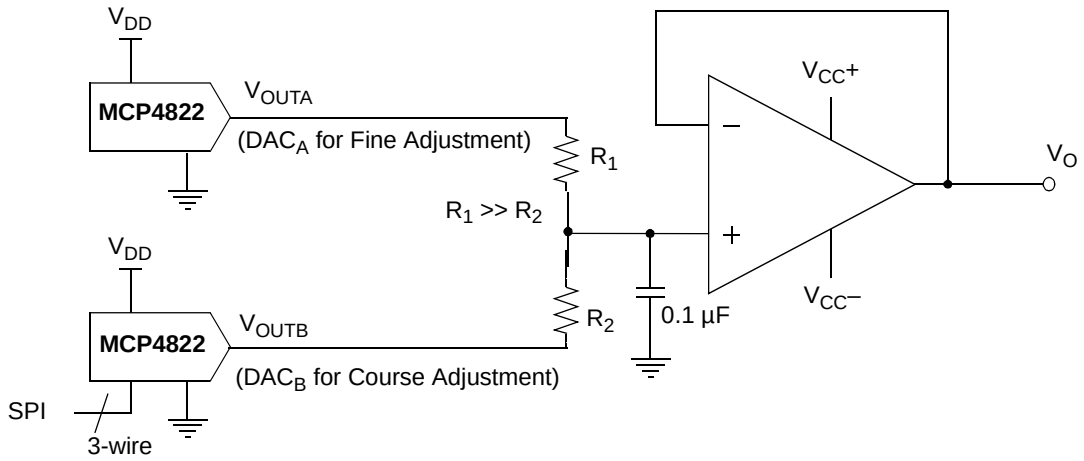
4.1V/1 µV = 4.1 x 10^6. Since 2^{22} = 4.2 x 10^6, 22-bit resolution is desired. Since DNL = ±0.75 LSb, this design can be done with the 12-bit MCP4822 DAC.

Step 2: Since DAC_B's V_{OUTB} has a resolution of 1 mV, its output only needs to be "pulled" 1/1000 to meet the 1 µV target. Dividing V_{OUTA} by 1000 would allow the application to compensate for DAC_B's DNL error.

Step 3: If R_2 is 100Ω, then R_1 needs to be 100 kΩ.

Step 4: The resulting transfer function is shown in the equation of Example 6-5.

EXAMPLE 6-5: SIMPLE, DOUBLE-PRECISION DAC WITH MCP4822



$$V_{OUTA} = 2.048 \cdot G_A \cdot \frac{D_A}{2^{12}}$$

$$V_{OUTB} = 2.048 \cdot G_B \cdot \frac{D_B}{2^{12}}$$

$$V_O = \frac{V_{OUTA}R_2 + V_{OUTB}R_1}{R_1 + R_2}$$

G_x	=	Gain selection (1x or 2x)
D_n	=	Digital value of DAC (0-4096)

6.9 Building Programmable Current Source

Example 6-6 shows an example of building a programmable current source using a voltage follower. The current sensor (sensor resistor) is used to convert the DAC voltage output into a digitally-selectable current source.

Adding the resistor network from Example 6-2 would be advantageous in this application. The smaller R_{SENSE} is, the less power dissipated across it. However, this also reduces the resolution that the current can be controlled with. The voltage divider, or "window", DAC configuration would allow the range to be reduced, thus increasing resolution around the range of interest. When working with very small sensor voltages, plan on eliminating the amplifier's offset error by storing the DAC's setting under known sensor conditions.

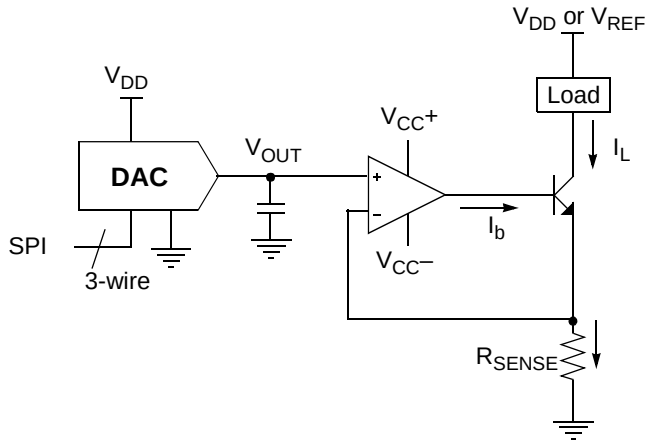
EXAMPLE 6-6: DIGITALLY-CONTROLLED CURRENT SOURCE

(a) Single Output DAC:

MCP4801
MCP4811
MCP4821

(b) Dual Output DAC:

MCP4802
MCP4812
MCP4822



$$I_b = \frac{I_L}{\beta}$$

$$I_L = \frac{V_{OUT}}{R_{sense}} \times \frac{\beta}{\beta + 1}$$

where β = Common-Emitter Current Gain.

G	=	Gain selection (1x or 2x)
D_n	=	Digital value of DAC (0-255) for MCP4801/MCP4802
	=	Digital value of DAC (0-1023) for MCP4811/MCP4812
	=	Digital value of DAC (0-4095) for MCP4821/MCP4822
N	=	DAC bit resolution

NOTES:

7.0 DEVELOPMENT SUPPORT

7.1 Evaluation and Demonstration Boards

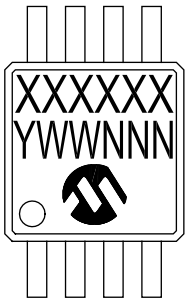
The Mixed Signal PICtail™ Demo Board supports the MCP4802/4812/4822 family of devices. Refer to www.microchip.com for further information on this product's capabilities and availability.

NOTES:

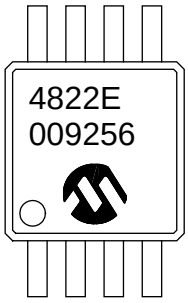
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

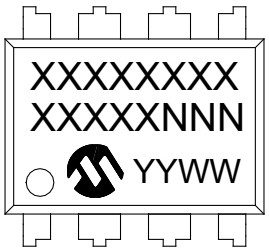
8-Lead MSOP (3x3 mm)



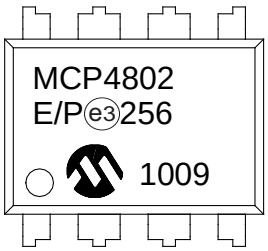
Example



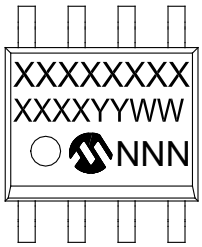
8-Lead PDIP (300 mil)



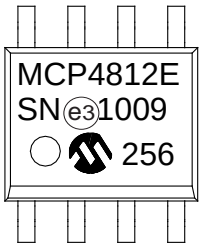
Example



8-Lead SOIC (3.90 mm)



Example

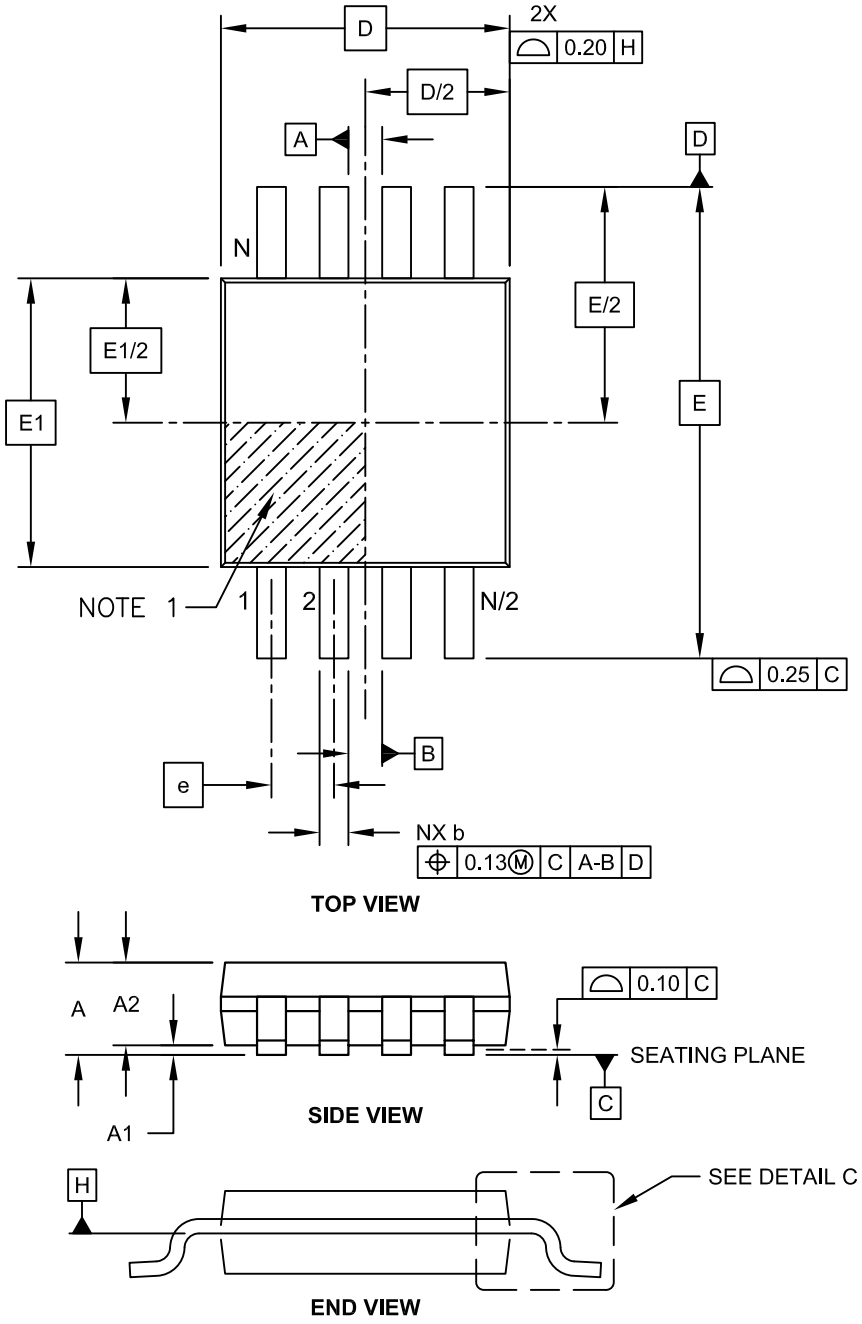


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

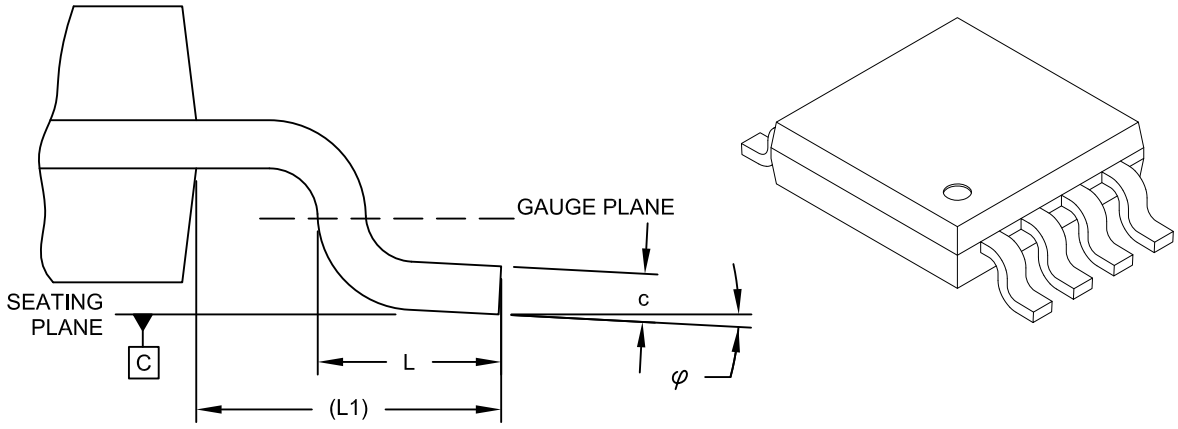
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

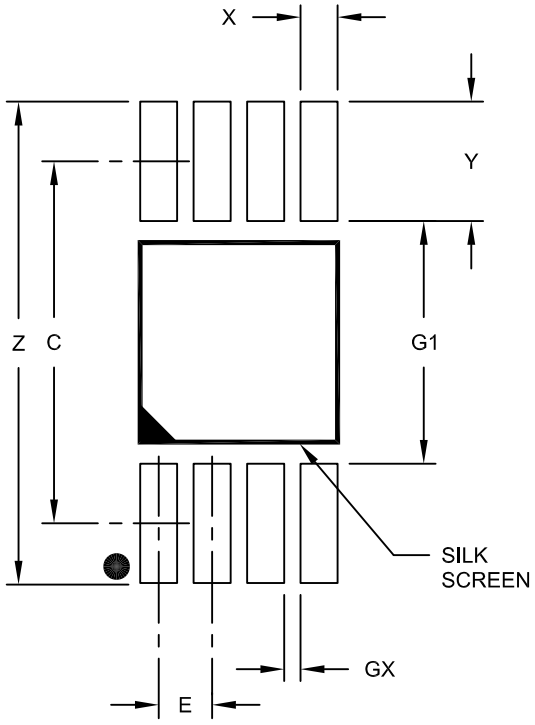
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

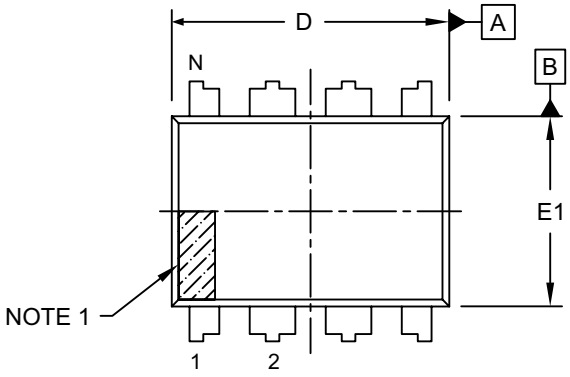
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

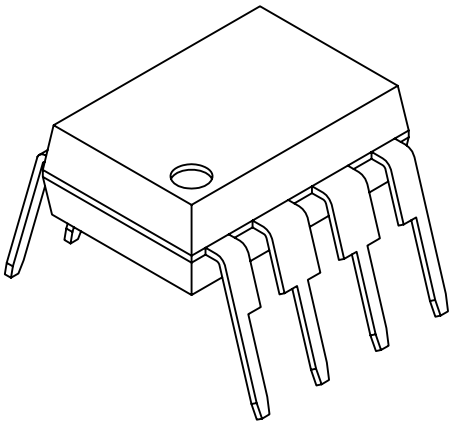
Microchip Technology Drawing No. C04-2111A

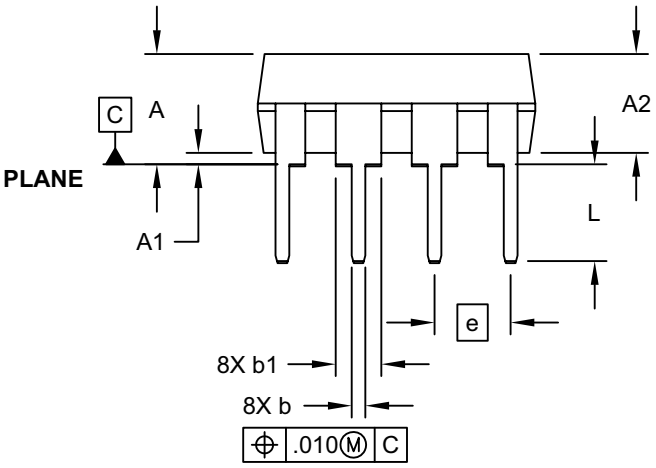
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

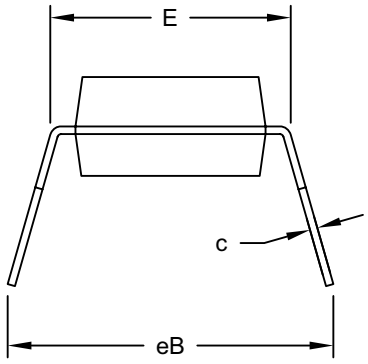


TOP VIEW





SIDE VIEW

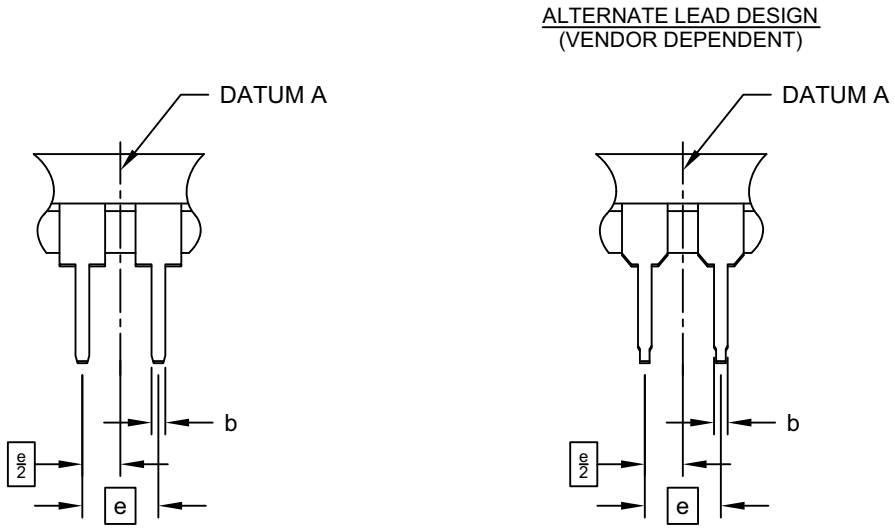


END VIEW

Microchip Technology Drawing No. C04-018D Sheet 1 of 2

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

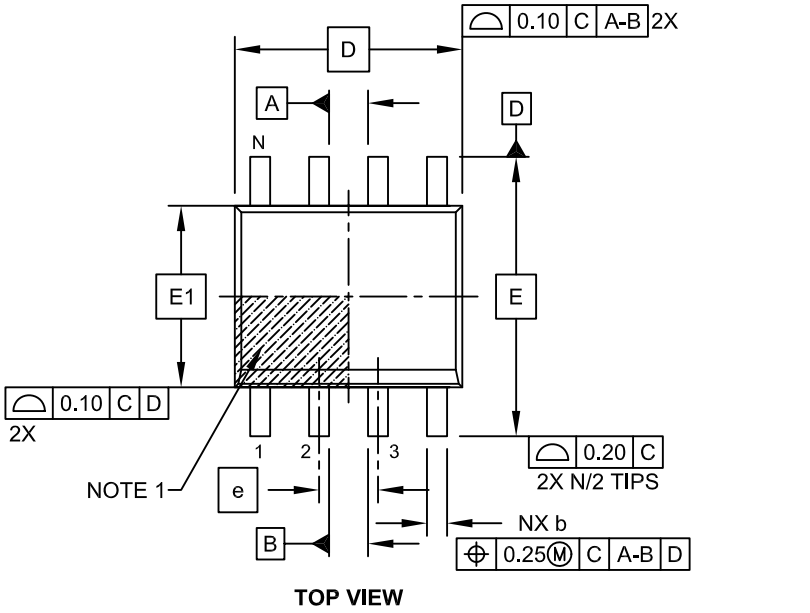
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

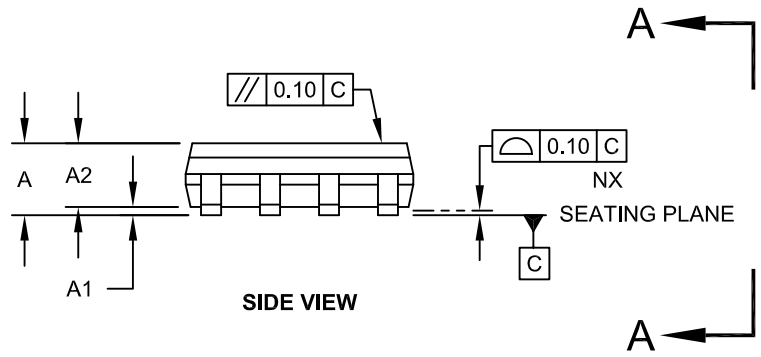
Microchip Technology Drawing No. C04-018D Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

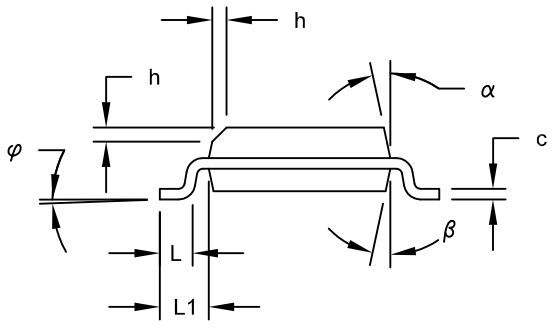
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

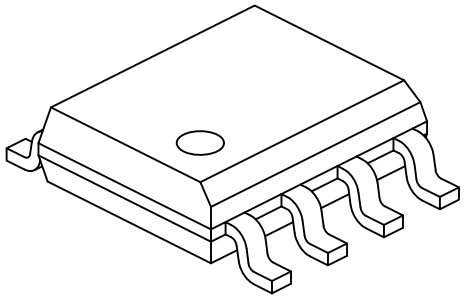


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

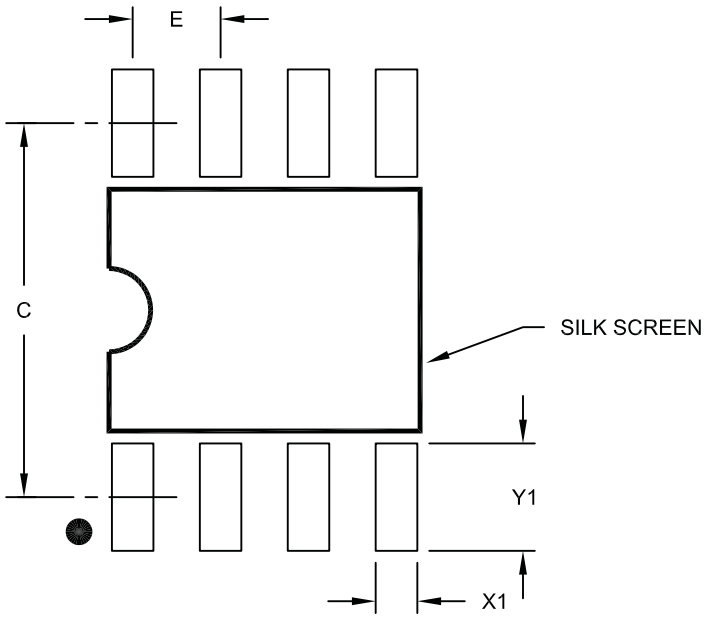
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (May 2015)

- Updated MSOP package marking drawing to correctly display the part's orientation.

Revision A (April 2010)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP4802:	Dual 8-Bit Voltage Output DAC
	MCP4802T:	Dual 8-Bit Voltage Output DAC (Tape and Reel, MSOP and SOIC only)
	MCP4812:	Dual 10-Bit Voltage Output DAC
	MCP4812T:	Dual 10-Bit Voltage Output DAC (Tape and Reel, MSOP and SOIC only)
	MCP4822:	Dual 12-Bit Voltage Output DAC
	MCP4822T:	Dual 12-Bit Voltage Output DAC (Tape and Reel, MSOP and SOIC only)
Temperature Range:	E =	-40°C to +125°C (Extended)
Package:	MS =	8-Lead Plastic Micro Small Outline (MSOP)
	P =	8-Lead Plastic Dual In-Line (PDIP)
	SN =	8-Lead Plastic Small Outline - Narrow, 150 mil (SOIC)

Examples:

a)	MCP4802-E/MS:	Extended temperature, MSOP package.
b)	MCP4802T-E/MS:	Extended temperature, MSOP package, Tape and Reel.
c)	MCP4802-E/P:	Extended temperature, PDIP package.
d)	MCP4802-E/SN:	Extended temperature, SOIC package.
e)	MCP4802T-E/SN:	Extended temperature, SOIC package, Tape and Reel.
a)	MCP4812-E/MS:	Extended temperature, MSOP package.
b)	MCP4812T-E/MS:	Extended temperature, MSOP package, Tape and Reel.
c)	MCP4812-E/P:	Extended temperature, PDIP package.
d)	MCP4812-E/SN:	Extended temperature, SOIC package.
e)	MCP4812T-E/SN:	Extended temperature, SOIC package, Tape and Reel.
a)	MCP4822-E/MS:	Extended temperature, MSOP package.
b)	MCP4822T-E/MS:	Extended temperature, MSOP package, Tape and Reel.
c)	MCP4822-E/P:	Extended temperature, PDIP package.
d)	MCP4822-E/SN:	Extended temperature, SOIC package.
e)	MCP4822T-E/SN:	Extended temperature, SOIC package, Tape and Reel.

NOTES:

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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