# 6-Pin µP Reset Circuit with Power-Fail Comparator

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$ to GND .....-0.3V to +6V
RESET, $\overline{RESET}$
(MAX6342/MAX6344/MAX6345) ..... -0.3V to ($V_{CC}$ + 0.3V)
$\overline{RESET}$ (MAX6343)..... -0.3V to +6V
$\overline{MR}$, PFI, $\overline{PFO}$ .....-0.3V to ($V_{CC}$ + 0.3V)
Input Current, $V_{CC}$ .....50mA
Output Current, RESET, $\overline{RESET}$ .....50mA

Continuous Power Dissipation ($T_A$ = +70°C)
6-Pin SOT23 (derate 4mW/°C above +70°C).....320mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature Range (soldering, 10s)..... +300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{CC}$ = +1.0V to +5.5V, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = +25°C and $V_{CC}$ = +3V.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Supply Voltage Range | $V_{CC}$ | $T_A$ = 0°C to +70°C | | 1.0 | | 5.5 | V |
| | | $T_A$ = -40°C to +125°C | | 1.2 | | 5.5 | |
| Supply Current | $I_{CC}$ | No load | $V_{CC}$ = 3V, TA = -40° to +85°C | | 25 | 40 | µA |
| | | | $V_{CC}$ = 5.5V, TA = -40° to +85°C | | 30 | 50 | |
| | | | $V_{CC}$ = 3V, TA = -40° to +125°C | | 25 | 50 | |
| | | | $V_{CC}$ = 5.5V, TA = -40° to +125°C | | 30 | 60 | |
| Reset Threshold | $V_{TH}$ | MAX634_L | $T_A$ = +25°C | 4.56 | 4.63 | 4.70 | V |
| | | | $T_A$ = -40°C to +85°C | 4.50 | | 4.75 | |
| | | | $T_A$ = -40°C to +125°C | 4.40 | | 4.86 | |
| | | MAX634_M | $T_A$ = +25°C | 4.31 | 4.38 | 4.45 | |
| | | | $T_A$ = -40°C to +85°C | 4.25 | | 4.50 | |
| | | | $T_A$ = -40°C to +125°C | 4.16 | | 4.56 | |
| | | MAX634_T | $T_A$ = +25°C | 3.03 | 3.08 | 3.13 | |
| | | | $T_A$ = -40°C to +85°C | 3.00 | | 3.15 | |
| | | | $T_A$ = -40°C to +125°C | 2.92 | | 3.23 | |
| | | MAX634_S | $T_A$ = +25°C | 2.89 | 2.93 | 2.97 | |
| | | | $T_A$ = -40°C to +85°C | 2.85 | | 3.00 | |
| | | | $T_A$ = -40°C to +125°C | 2.78 | | 3.08 | |
| | | MAX634_R | $T_A$ = +25°C | 2.59 | 2.63 | 2.67 | |
| | | | $T_A$ = -40°C to +85°C | 2.55 | | 2.70 | |
| | | | $T_A$ = -40°C to +125°C | 2.50 | | 2.76 | |
| | | MAX634_Z | $T_A$ = +25°C | 2.30 | 2.33 | 2.36 | |
| | | | $T_A$ = -40°C to +85°C | 2.25 | | 2.38 | |
| | | | $T_A$ = -40°C to +125°C | 2.21 | | 2.45 | |
| $V_{CC}$ to Reset Delay | | $V_{CC}$ = $V_{TH}$ to ($V_{TH}$ - 100mV) | | | 20 | | µs |
| $\overline{RESET}$ and RESET Outputs Drive Capability (Note 2) | $V_{OL}$ | $V_{CC}$ > 1.2V, $I_{SINK}$ = 100µA | | | | 0.4 | V |
| | | $V_{CC}$ > 2.7V, $I_{SINK}$ = 1.2mA | | | | 0.3 | |
| | | $V_{CC}$ > 4.5V, $I_{SINK}$ = 3.2mA | | | | 0.4 | |
| | $V_{OH}$ | $V_{CC}$ > 1.2V, $I_{SOURCE}$ = 50µA | | 0.8 × $V_{CC}$ | | | V |
| | | $V_{CC}$ > 2.7V, $I_{SOURCE}$ = 500µA (MAX6342/MAX6345 only) | | 0.8 × $V_{CC}$ | | | |
| | | $V_{CC}$ > 4.5V, $I_{SOURCE}$ = 800µA (MAX6342/MAX6345 only) | | 0.8 × $V_{CC}$ | | | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = +1.0V to +5.5V, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = +25°C and $V_{CC}$ = +3V.) (Note 1)

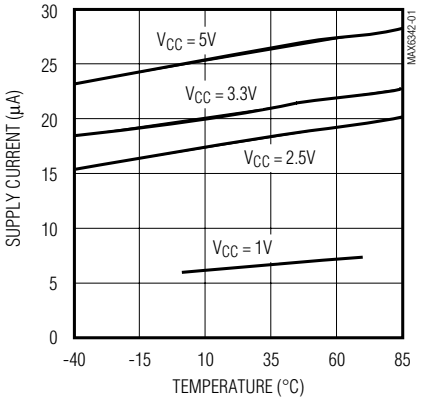
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Reset Timeout Period | $t_{RP}$ | $T_A$ = -40°C to +85°C | 100 | 180 | 280 | ms |
| | | $T_A$ = -40°C to +125°C | 80 | | 360 | |
| Open-Drain $\overline{RESET}$ Output Leakage Current (Note 3) | $I_{LKG}$ | MAX6343 only, $V_{CC} > V_{TH(MAX)}$ | | | 1 | µA |
| $\overline{MR}$ Input Low | $V_{IL}$ | | | | 0.3 × VCC | V |
| $\overline{MR}$ Input High | $V_{IH}$ | | 0.7 × VCC | | | V |
| $\overline{MR}$ Pull-Up Resistance | | | 60 | | | kΩ |
| $\overline{MR}$ Minimum Pulse Width | | | 1 | | | µs |
| $\overline{MR}$ Glitch Rejection | | | | 0.1 | | µs |
| $\overline{MR}$ to Reset Delay | | | | 0.2 | | µs |
| PFI Input Threshold | | $T_A$ = -40°C to +85°C | 1.2 | 1.25 | 1.3 | V |
| | | $T_A$ = -40°C to +125°C | 1.15 | | 1.35 | |
| PFI Leakage Current (Note 3) | | $T_A$ = -40°C to +85°C | | ±0.01 | ±25 | nA |
| | | $T_A$ = -85°C to +125°C | | | ±100 | |
| $\overline{PFO}$ Output Voltage | $V_{OL}$ | $V_{CC}$ = 4.5V, $I_{SINK}$ = 3.2mA | | | 0.4 | V |
| $\overline{PFO}$ Output Voltage | $V_{OH}$ | $V_{CC}$ = 4.5V, $I_{SOURCE}$ = 800µA | 0.8 × VCC | | | V |
| $\overline{PFO}$ Output Short-Circuit Current | | Output sink current | | 20 | | mA |
| | | Output source current | | 5 | | |
| PFI to $\overline{PFO}$ Delay | | $V_{OVERDRIVE}$ = 15mV | | 3 | | µs |

**Note 1:** Overtemperature limits are guaranteed by design and not production tested.
**Note 2:** Apply to each part in accordance with threshold voltage, output configuration, and manual reset status selected.
**Note 3:** Leakage parameters are guaranteed by design and not production tested.

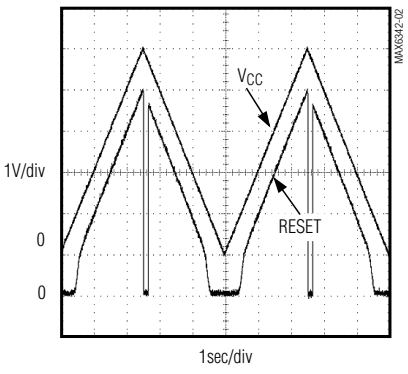
## Typical Operating Characteristics

($V_{PFI}$ = $V_{CC}$ = +5V, $T_A$ = +25°C, unless otherwise noted.)

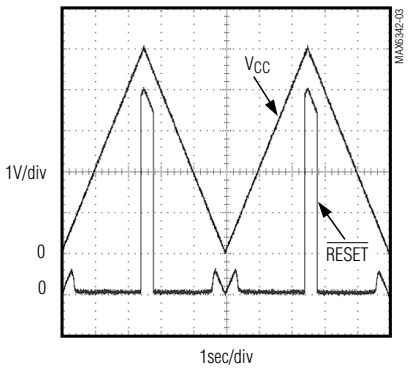
**SUPPLY CURRENT vs. SUPPLY VOLTAGE AND TEMPERATURE**




**MAX6344L/MAX6345L RESET OUTPUT VOLTAGE vs. SUPPLY VOLTAGE**




**MAX6342M/MAX6345M RESET OUTPUT VOLTAGE vs. SUPPLY VOLTAGE**

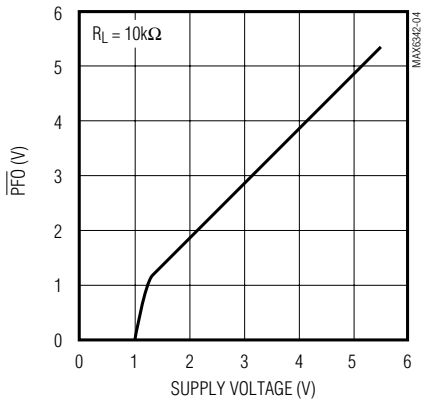


# 6-Pin µP Reset Circuit with Power-Fail Comparator

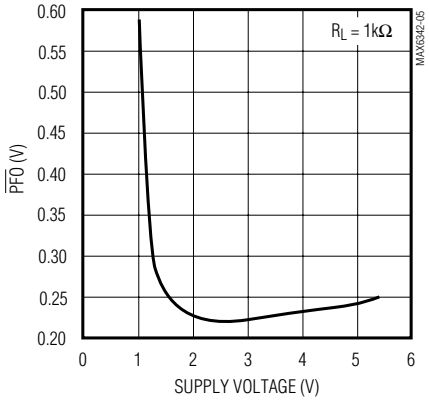
## Typical Operating Characteristics (continued)

($V_{PFI}$ = $V_{CC}$ = +5V, $T_A$ = +25°C, unless otherwise noted.)

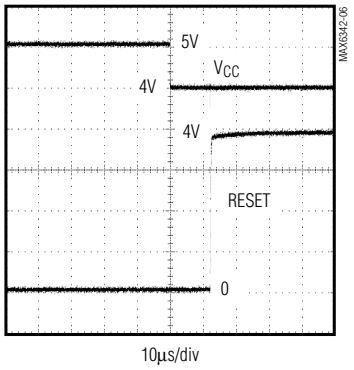
**$\overline{PFO}$ OUTPUT-VOLTAGE HIGH vs. SUPPLY VOLTAGE**



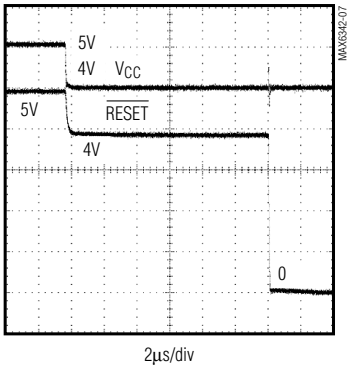

**$\overline{PFO}$ OUTPUT-VOLTAGE LOW vs. SUPPLY VOLTAGE**




**MAX6344/MAX6345 RESET RESPONSE TIME**




**MAX6342/MAX6345 $\overline{RESET}$ RESPONSE TIME**




## Pin Description

| PIN | | | | NAME | FUNCTION |
|---|---|---|---|---|---|
| MAX6342 | MAX6343 | MAX6344 | MAX6345 | | |
| 1 | 1 | 1 | 1 | $V_{CC}$ | Supply Voltage |
| 2 | 2 | 2 | 2 | GND | Ground |
| 3 | 3 | 3 | 3 | PFI | Power-Fail Voltage Monitor Input. When PFI is < 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or $V_{CC}$ when not used. |
| 4 | 4 | 4 | 4 | $\overline{PFO}$ | Power-Fail Voltage Monitor Output |

# 6-Pin µP Reset Circuit with Power-Fail Comparator

## Pin Description (continued)

| PIN | | | | NAME | FUNCTION |
|---|---|---|---|---|---|
| MAX6342 | MAX6343 | MAX6344 | MAX6345 | | |
| 5 | 5 | 5 | — | $\overline{MR}$ | Manual-Reset Input. Pull low to force a reset. $\overline{RESET}$ or RESET remains active as long as $\overline{MR}$ is low and for the reset timeout period after $\overline{MR}$ goes high. Leave unconnected or connect to $V_{CC}$ if unused. |
| 6 | 6 | — | 5 | $\overline{RESET}$ | Active-Low Reset Output. Push-pull for MAX6342/MAX6345. Open-drain for MAX6343. It remains low for 180ms after $V_{CC}$ rises above the reset threshold or $\overline{MR}$ goes from low to high. |
| — | — | 6 | 6 | RESET | Active-High Push-Pull Reset Output. It remains high for 180ms after $V_{CC}$ rises above the reset threshold or $\overline{MR}$ goes from low to high. |

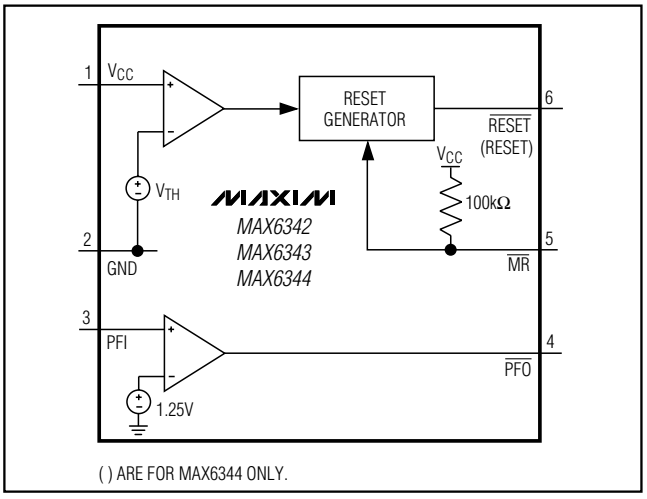



*Figure 1. MAX6342/MAX6343/MAX6344 Functional Diagram*

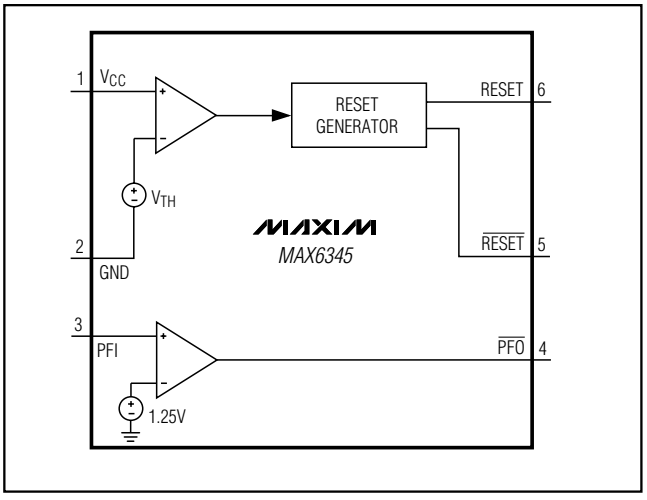



*Figure 2. MAX6345 Functional Diagram*

## Detailed Description

### Reset Output

A µP's reset input starts the µP in a known state. These µP supervisory circuits assert reset to prevent code-execution errors during power-up, power-down, or brownout conditions.

$\overline{RESET}$ and RESET are guaranteed to be asserted at a valid logic level for $V_{CC}$ > +1V (see the *Electrical Characteristics* table). Once RESET asserts, it remains asserted for at least 100ms ($t_{RP}$) after $V_{CC}$ rises above its threshold value or after $\overline{MR}$ returns high (Figures 1 and 2).

### Open-Drain $\overline{RESET}$ Output

The MAX6343 has an active-low, open-drain reset output. This output sinks current when $\overline{RESET}$ is asserted. Connect a pull-up resistor from $\overline{RESET}$ to any positive supply voltage up to +5.5V (Figure 3). Select a resistor value large enough to register a logic low (see the *Electrical Characteristics* table), and small enough to register a logic high while supplying all input current and leakage paths connected to the $\overline{RESET}$ line. A 10kΩ pull-up is sufficient in most applications.

### Manual Reset

The MAX6342/MAX6343/MAX6344s' manual-reset input ($\overline{MR}$) allows reset to be triggered by a pushbutton switch. The switch is effectively debounced by the 1µs min reset pulse width. $\overline{MR}$ is CMOS-logic compatible.

# 6-Pin µP Reset Circuit with Power-Fail Comparator

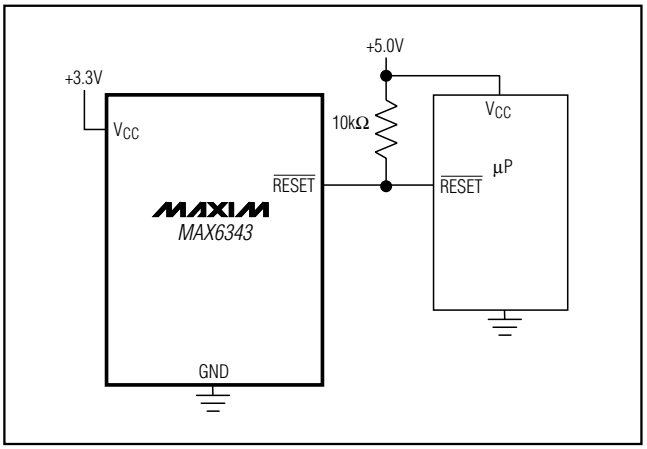



*Figure 3. Open-Drain $\overline{RESET}$ Output Allows Use with Multiple Supplies*

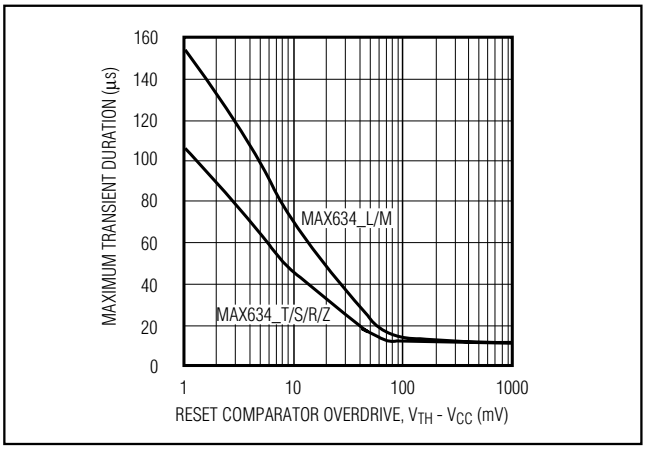



*Figure 4. Maximum Transient Duration Magnitude Rejection*

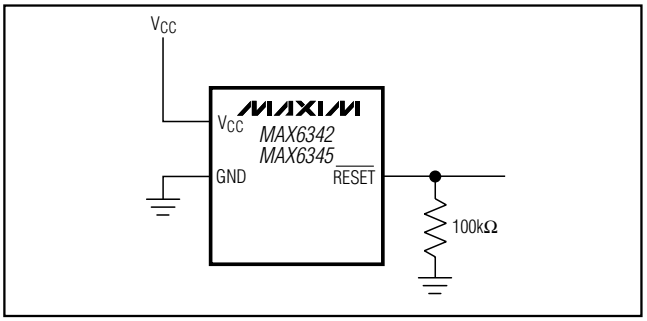



*Figure 5. Ensuring $\overline{RESET}$ Valid to $V_{CC}$ = 0 on Active-Low Push-Pull Outputs*

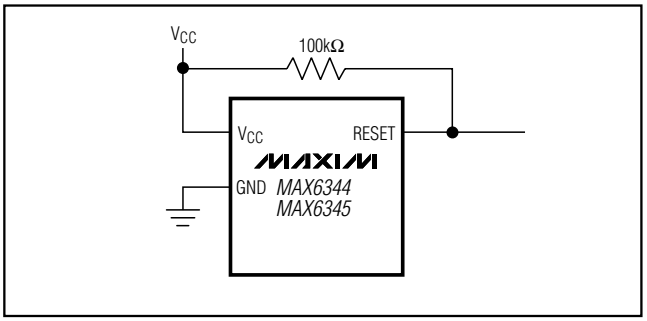



*Figure 6. Ensuring $\overline{RESET}$ Valid to $V_{CC}$ = 0 on Active-High Push-Pull Outputs*

### Power-Fail Comparator

The power-fail comparator is useful for various purposes because the power-fail output ($\overline{PFO}$) is independent of the reset output. The inverting input is internally connected to a +1.25V reference.

To build an early-warning circuit for power failure, connect the PFI pin to a voltage divider (see the *Typical Oper-ating Circuit*). Choose the voltage-divider ratio so that the voltage at PFI falls below +1.25V just before the +5V regulator drops out. Use $\overline{PFO}$ to interrupt the µP to prepare for an orderly shutdown.

## Applications Information

### Negative-Going $V_{CC}$ Transients

The MAX6342–MAX6345 supervisors are immune to short-duration, negative-going $V_{CC}$ transients (glitches) that usually do not require the entire system to shut down.

Figure 4 shows typical transient duration vs. reset comparator overdrive, for which the MAX6342–MAX6345 do not generate a reset pulse. The graph was generated using a negative-going pulse applied to $V_{CC}$, starting 0.5V above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the maximum pulse width a negative-going $V_{CC}$ transient can have without causing a reset pulse. As the magnitude of the transient increases (goes further below the reset threshold), the maximum allowable pulse width decreases.

Typically, a $V_{CC}$ transient that goes 100mV below the reset threshold and lasts 12µs or less will not cause a reset pulse. A 1µF bypass capacitor mounted as close as possible to the $V_{CC}$ pin provides additional transient immunity.

### Ensuring a Valid Reset Output Down to $V_{CC}$ = 0

The MAX6342–MAX6345 are guaranteed to operate properly down to $V_{CC}$ = +1V. In applications that require valid reset levels down to $V_{CC}$ = 0, a pulldown resistor to active-low outputs (MAX6342/MAX6345) and a pullup resistor to active-high outputs (MAX6344/MAX6345) ensure that the reset line is valid when the reset output is no longer sinking or sourcing current (Figures 5 and 6).

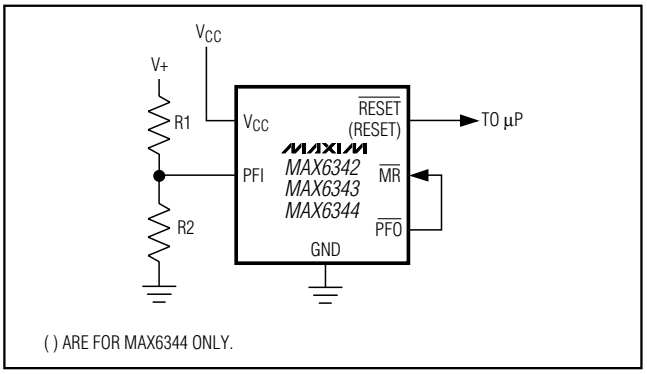



*Figure 7. Monitoring Two Supplies*

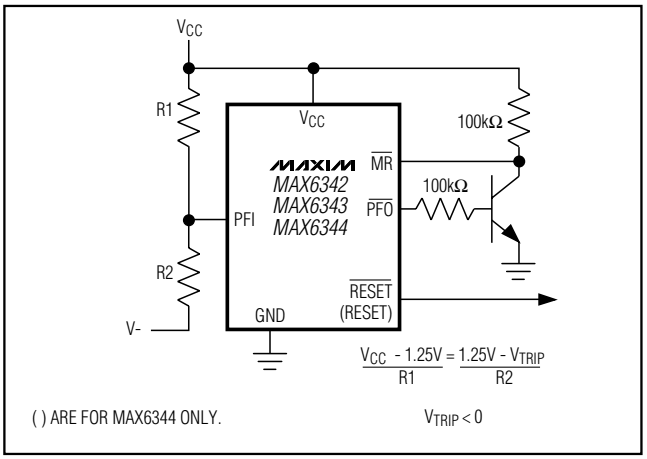



*Figure 8. Monitoring a Negative Voltage*

Note that this method does not work with the open-drain output of the MAX6343. The resistor value used is not critical, but it must be large enough not to load the reset output when $V_{CC}$ is above the reset threshold. For most applications, 100kΩ is adequate.

### Monitoring Two Supplies

Monitor another voltage by connecting a resistor-divider to PFI as shown in Figure 7. The threshold voltage will then be given by:

$$V_{TH(PFI)} = 1.25[(R1 + R2) / R2]$$

where $V_{TH(PFI)}$ is the threshold at which the monitored voltage will trip $\overline{PFO}$.

A good rule of thumb for selecting the resistors is to choose R2 between 250kΩ and 500kΩ and solve for R1. Connect $\overline{PFO}$ to $\overline{MR}$ in applications that require reset to assert when the second voltage falls below its threshold.

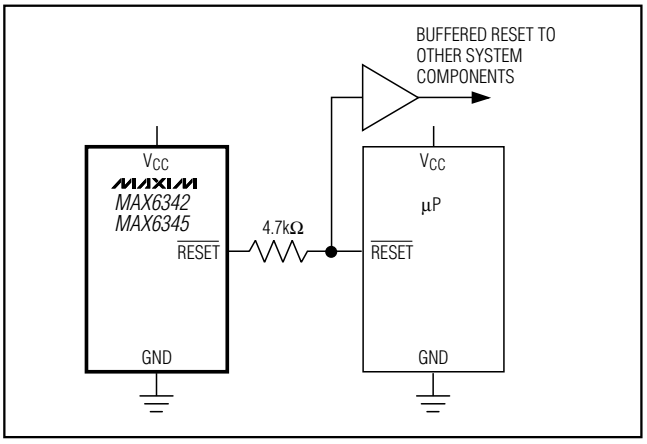



*Figure 9. Interfacing to µPs with Bidirectional Reset I/O*

### Monitoring a Negative Voltage

Connect the circuit as shown in Figure 8 to use the power-fail comparator to monitor a negative supply rail. $\overline{PFO}$ stays low when V- is good. When V- rises to cause PFI to be above +1.25V, $\overline{PFO}$ goes high. By adding the resistors and transistor as shown, a high $\overline{PFO}$ triggers reset. As long as $\overline{PFO}$ remains high, the MAX6342/MAX6343/MAX6344 will keep reset asserted. Note that the accuracy of this circuit depends on the PFI threshold tolerance, the $V_{CC}$ line voltage, and the resistors. Also, ensure that the voltage at PFI remains above GND.

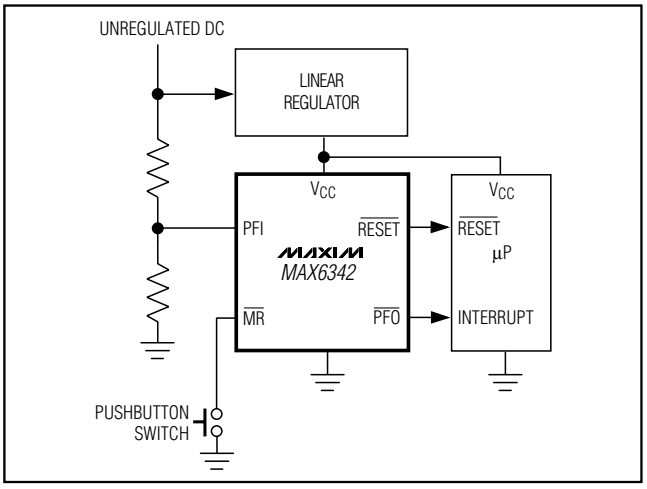
### Interfacing to µPs with Bidirectional Reset Pins

## SOT Top Marks

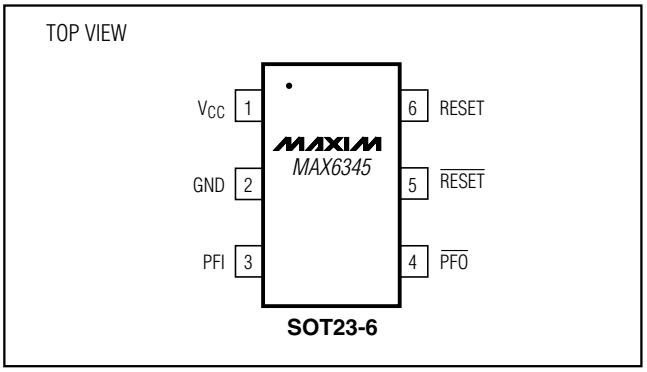
| PART | SOT TOP MARK | PART | SOT TOP MARK |
|---|---|---|---|
| MAX6342LUT-T | AACP | MAX6344LUT-T | AADQ |
| MAX6342MUT-T | AACQ | MAX6344MUT-T | AADR |
| MAX6342TUT-T | AACR | MAX6344TUT-T | AADS |
| MAX6342SUT-T | AACS | MAX6344SUT-T | AADT |
| MAX6342RUT-T | AACT | MAX6344RUT-T | AADU |
| MAX6342ZUT-T | AACU | MAX6344ZUT-T | AADV |
| MAX6343LUT-T | AACV | MAX6345LUT-T | AADW |
| MAX6343MUT-T | AACW | MAX6345MUT-T | AADX |
| MAX6343TUT-T | AACX | MAX6345TUT-T | AADY |
| MAX6343SUT-T | AACY | MAX6345SUT-T | AADZ |
| MAX6343RUT-T | AACZ | MAX6345RUT-T | AAEA |
| MAX6343ZUT-T | AADA | MAX6345ZUT-T | AAEB |

# 6-Pin µP Reset Circuit with Power-Fail Comparator

## Typical Operating Circuit




## Pin Configurations (continued)

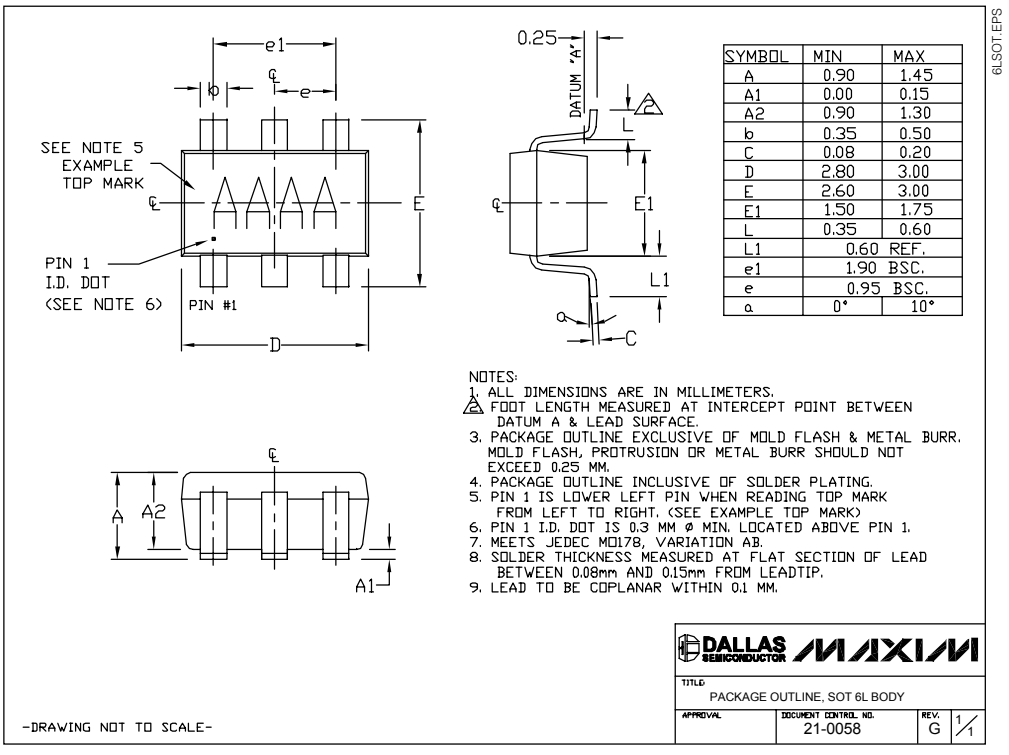



## Chip Information

TRANSISTOR COUNT: 403

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)




| SYMBOL | MIN | MAX |
|---|---|---|
| A | 0.90 | 1.45 |
| A1 | 0.00 | 0.15 |
| A2 | 0.90 | 1.30 |
| b | 0.35 | 0.50 |
| C | 0.08 | 0.20 |
| D | 2.80 | 3.00 |
| E | 2.60 | 3.00 |
| E1 | 1.50 | 1.75 |
| L | 0.35 | 0.60 |
| L1 | 0.60 REF. | |
| e1 | 1.90 BSC. | |
| e | 0.95 BSC. | |
| α | 0° | 10° |