ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND)

V+ .....-0.3V to +44V
V- .....-25V to +0.3V
V+ to V-.....-0.3V to +44V
All Other Pins (Note 1).....(V- - 0.3V) to (V+ + 0.3V)
Continuous Current into Any Terminal.....±20mA
Peak Current into Any Terminal
(pulsed at 1ms, 10% duty cycle).....±30mA
ESD per Method 3015.7 .....>2000V

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C).....471mW
µMAX (derate 4.1mW/°C above +70°C) 330mW
Operating Temperature Ranges
MAX452_C_A.....0°C to +70°C
MAX452_E_A.....-40°C to +85°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Signals on IN, A, B, X, or Y exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—±15V Supplies

(V+ = +15V, V- = -15V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog-Signal Range	V_A, V_B, V_X , V_Y	(Note 3)	C, E	-V		V+	V
A-X, A-Y, B-X, B-Y On-Resistance	R_{ON}	V_A = V_B = ±10V, I_A = I_B = 1mA	+25°C		105	175	Ω
			C, E			200	
A-X, A-Y, B-X, B-Y On-Resistance Match (Note 4)	ΔR_{ON}	V_A = V_B = ±10V, I_A = I_B = 1mA	+25°C		0.5	8	Ω
			C, E			10	
A-X, A-Y, B-X, B-Y On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	V_A = V_B = -5V, 0V, +5V; I_A = I_B = 1mA	+25°C		12	18	Ω
			C, E			30	
A, B, X, Y Leakage Current (Note 6)	$I_{A(OFF)}$, $I_{B(OFF)}$, $I_{X(OFF)}$, $I_{Y(OFF)}$	V+ = 16.5V, V- = -16.5V; V_{IN} = 0V, 3V; V_A = ±15.5V, V_B = ±15.5V	+25°C	-0.5	0.01	0.5	nA
			C, E	-10		10	
LOGIC INPUT							
IN Input Logic Threshold High	V_{INH}		C, E		1.6	2.4	V
IN Input Logic Threshold Low	V_{INL}		C, E	0.8	1.6		V
IN Input Current Logic High or Low	I_{INH}, I_{INL}	$V_{IN\_}$ = 0.8V or 2.4V	C, E	1	0.03	1	µA

ELECTRICAL CHARACTERISTICS—±15V Supplies (continued)

(V+ = +15V, V- = -15V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		T_A	MIN	TYP (Note 2)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS								
Transition Time	t_{TRANS}	$V_A = V_B = \pm10V$, V+ = 15V, V- = -15V, Figure 3	MAX4526	+25°C		65	100	ns
				C, E			125	
			MAX4527	+25°C		95	200	
				C, E			250	
Break-Before-Make Time Delay	t_{BBM}	$V_A = V_B = \pm10V$, V+ = 15V, V- = -15V, Figure 4		+25°C	1	5		ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_A or V_B = 0V, R_S = 0Ω, Figure 5		+25°C		1	10	pC
A-X, A-Y, B-X, B-Y Capacitance	C_{OFF}	$V_A = V_B$ = GND, f = 1MHz, Figure 6		+25°C		13		pF
A-X, A-Y, B-X, B-Y Isolation (Note 7)	V_{ISO}	R_L = 50Ω, C_L = 15pF, $V_A = V_B = 1V_{RMS}$, f = 1MHz, Figure 7		+25°C		-65		dB
POWER SUPPLY								
Power-Supply Range	V+, V-			C, E	±4.5		±20	V
V+ Supply Current	I+	V+ = 16.5V, V_{IN} = 0V or V+	MAX4526	+25°C		0.7	1	mA
				C, E			1.5	
			MAX4527	+25°C		0.05	1	µA
				C, E			10	
V- Supply Current	I-	V- = -16.5V	MAX4526	+25°C	-400			µA
				C, E	-500			
			MAX4527	+25°C	-1	0.05		
				C, E	-1			

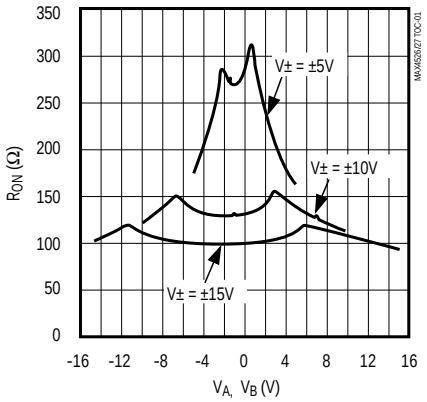
Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 3: Guaranteed by design.
Note 4: $\Delta R_{ON} = \Delta R_{ON(MAX)} - \Delta R_{ON(MIN)}$.
Note 5: Resistance flatness is defined as the difference between the maximum and minimum values of on-resistance as measured over the specified analog-signal range.
Note 6: Leakage current is 100% tested at maximum rated hot temperature, and is guaranteed by correlation at T_A = +25°C and minimum rated cold temperature.
Note 7: Off-isolation = 20log10 [(V_X or V_Y) / (V_A or V_B)], V_X or V_Y = output, V_A or V_B = input to off switch.

Phase-Reversal Analog Switches

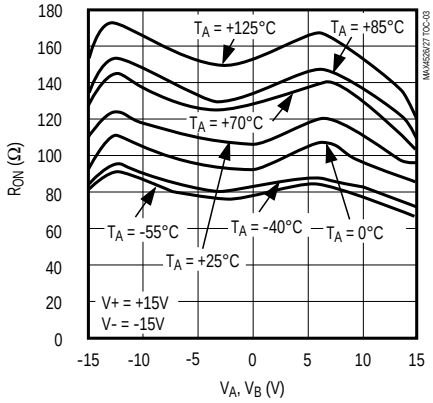
Typical Operating Characteristics

(V+ = +15V, V- = -15V, GND = 0V, T_A = +25°C, unless otherwise noted.)

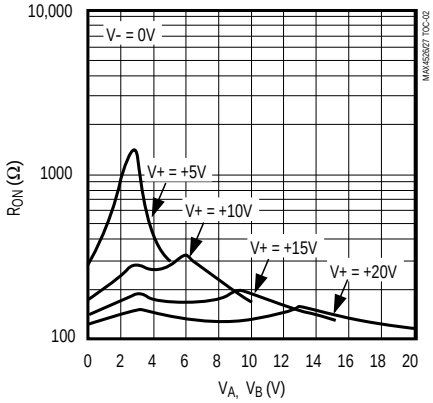
ON-RESISTANCE vs. V_A, V_B (DUAL SUPPLIES)



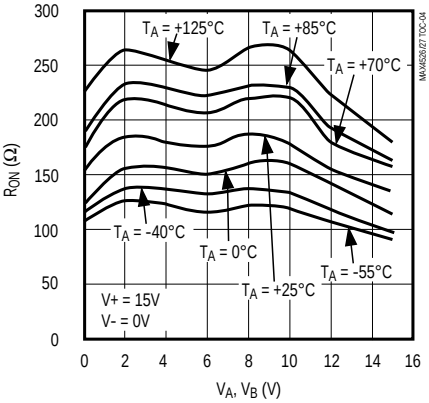
ON-RESISTANCE vs. V_A, V_B, AND TEMPERATURE (DUAL SUPPLIES)



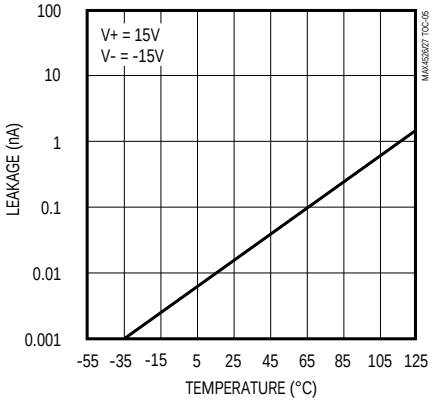
ON-RESISTANCE vs. V_A, V_B (SINGLE SUPPLY)



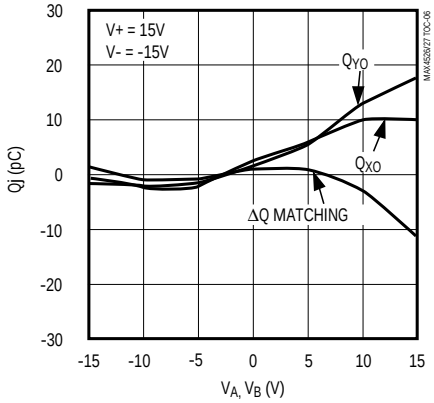
ON-RESISTANCE vs. V_A, V_B, AND TEMPERATURE (SINGLE SUPPLY)



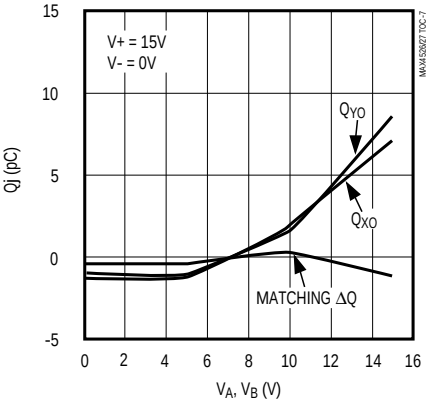
LEAKAGE vs. TEMPERATURE



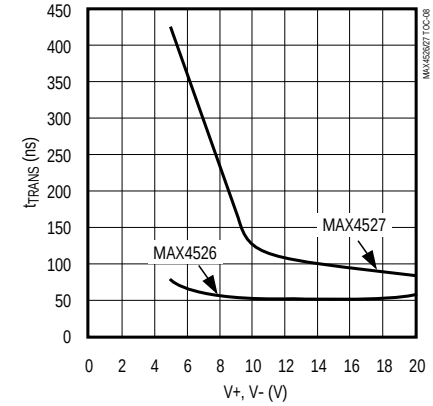
CHARGE INJECTION, CHARGE-INJECTION MATCHING vs. V_A, V_B



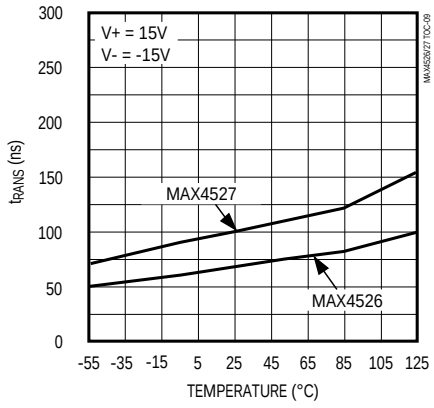
CHARGE INJECTION, CHARGE-INJECTION MATCHING vs. V_A, V_B (SINGLE SUPPLY)



TRANSITION TIME vs. SUPPLY VOLTAGE



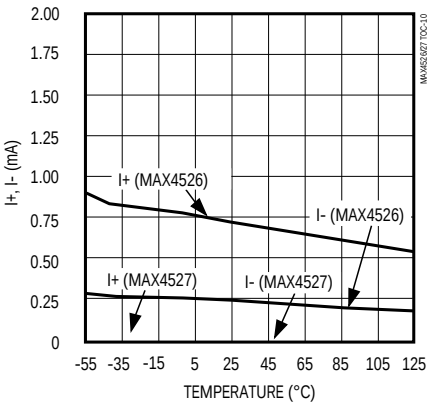
TRANSITION TIME vs. TEMPERATURE



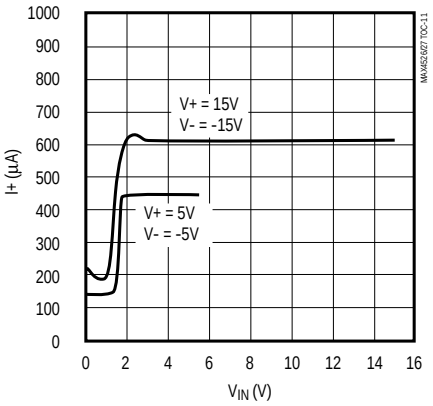
Typical Operating Characteristics (continued)

(V+ = +15V, V- = -15V, GND = 0V, T_A = +25°C, unless otherwise noted.)

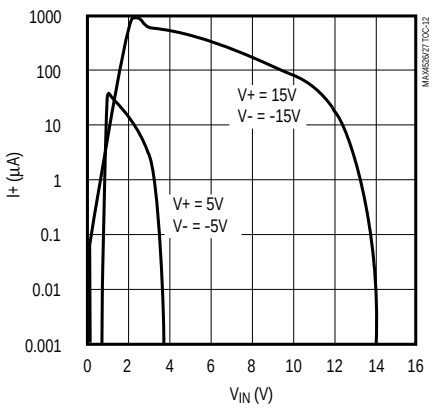
SUPPLY CURRENT vs. TEMPERATURE



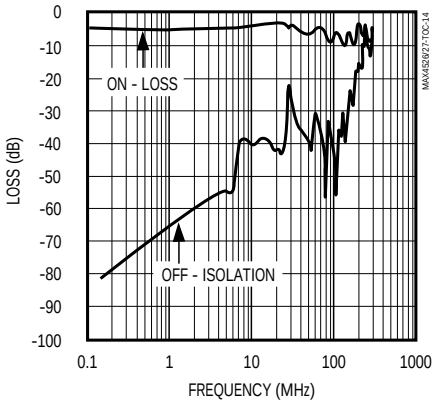
MAX4526
POSITIVE SUPPLY CURRENT vs. V_{IN}



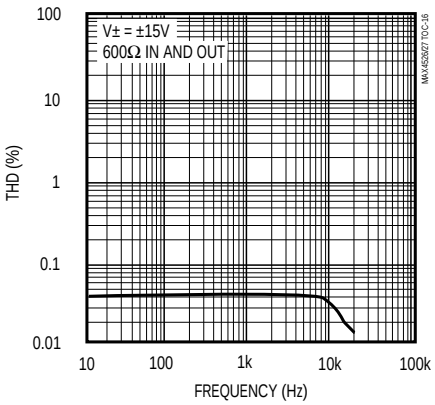
MAX4527
POSITIVE SUPPLY CURRENT vs. V_{IN}



MAX4526
FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION
vs. FREQUENCY



Phase-Reversal Analog Switches

Pin Configuration

PIN	NAME	FUNCTION
1	A	Analog-Switch Input Terminal A. Connected to Y when IN is low; connected to X when IN is high.
2	B	Analog-Switch Input Terminal B. Connected to X when IN is low; connected to Y when IN is high.
3	GND	Ground. Connect GND to digital ground. (Analog signals have no ground reference; they are limited to V+ and V-.)
4	IN	Logic-Level Control Inputs (see *Truth Table*).
5	V-	Negative Analog Supply-Voltage Input. Connect V- to GND for single-supply operation.
6	Y	Analog-Switch Output Terminal Y.
7	X	Analog-Switch Output Terminal X.
8	V+	Positive Analog/Digital Supply-Voltage Input. Internally connected to substrate.

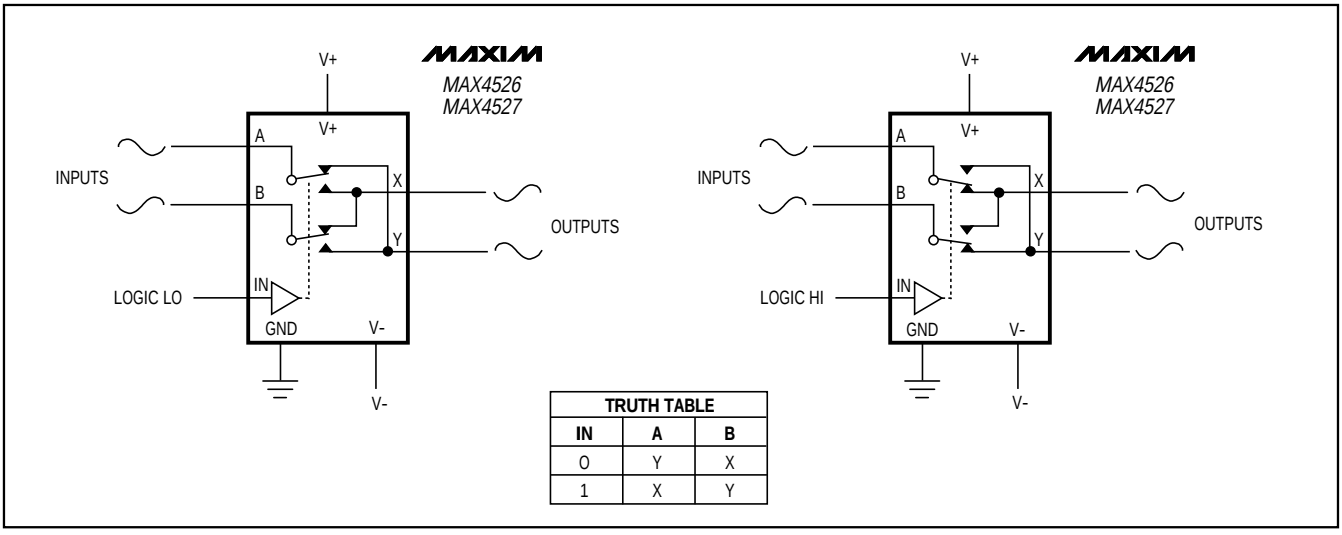
Note: A, B, X and Y pins are identical and interchangeable. Either may be considered as an input or output; signals pass equally well in either direction. However, AC symmetry is best when A and B are the input, and X and Y are the output. Reduce AC balance in critical applications by using A and X or A and Y as the input, and B and Y or B and X as the output.

Detailed Description

The MAX4526/MAX4527 are phase-reversal analog switches, consisting of two normally open and two normally closed CMOS analog switches arranged in a bridge configuration. Analog signals are put into two input pins and taken out of two output pins. A logic-level signal controls whether the input signal is routed through normally or inverted. A low-resistance DC path goes from inputs to outputs at all times, yet isolation between the two signal paths is excellent. Analog signals range from V- to V+.

These parts are characterized and optimized with ±15V supplies, and they can operate from a single supply. The MAX4526 is optimized for high-frequency operation, and has a higher-speed logic-level translator and switch driver. The MAX4527 has identical analog switch characteristics, but has a slower logic-level translator and switch driver for lower current consumption.

The MAX4526/MAX4527 are designed for DC and low-frequency-signal phase-reversal applications, such as chopper amplifiers, modulator/demodulators, and self-zeroing or self-calibrating circuits. Unlike conventional CMOS switches externally wired in a bridge configuration, both DC and AC symmetry are optimized with a small 8-pin configuration that allows simple board layout and isolation of logic signals from analog signals.



TRUTH TABLE		
IN	A	B
0	Y	X
1	X	Y

Figure 1. Typical Application Circuits

Power-Supply Considerations

Overview

The MAX4526/MAX4527 construction is typical of most CMOS analog switches. It has three supply pins: V+, V-, and GND. V+ and V- drive the internal CMOS switches and set the analog-voltage limits on any switch. Reverse ESD-protection diodes are internally connected between each analog signal pin, and both V+ and V-. One of these diodes conducts if any analog signal exceeds V+ or V-.

Virtually all of the analog leakage current is through the ESD diodes to V+ or V-. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The *difference* in the two diode leakages from the signal path to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows to the supply terminals, not to the other switch terminal. This explains how both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog-signal paths and GND. The analog-signal paths consist of an N-channel and P-channel MOSFET with their sources and drains paralleled and their gates driven out-of-phase to V+ and V- by the logic-level translators.

V+ and GND power the internal logic and logic-level translator and set the input logic threshold. The logic-level translator converts the logic levels to switched V+ and V- signals to drive the analog switches' gates. This drive signal is the only connection between GND and the analog supplies. V+ and V- have ESD-protection diodes to GND. The logic-level input has ESD protection to V+ and to V- but not to GND, so the logic signal can go below GND (as low as V-) when bipolar supplies are used.

Increasing V- has no effect on the logic-level thresholds, but it does increase the drive to the internal P-channel switches, reducing the overall switch on-resistance. V- also sets the negative limit of the analog-signal voltage.

The logic-level input pin, IN, has ESD-protection diodes to V+ and V- but not to GND, so it can be safely driven to V+ and V-. The logic-level threshold, V_{IN}, is CMOS/TTL compatible when V+ is between 4.5V and 36V (see *Typical Operating Characteristics*).

Bipolar Supplies

The MAX4526/MAX4527 operate with bipolar supplies between ±4.5V and ±18V. However, since all factory characterization is done with ±15V supplies, specifications at other supplies are not guaranteed. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of 44V (see *Absolute Maximum Ratings*).

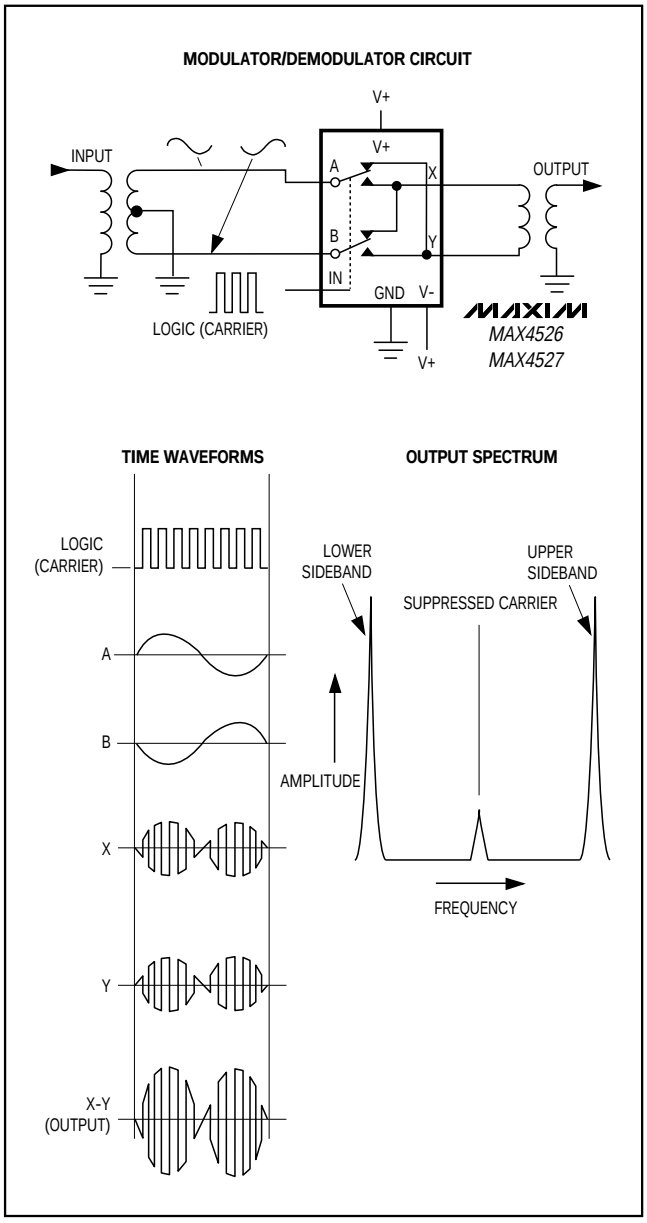


Figure 2. Balanced Modulator/Demodulator

Single Supply

The MAX4526/MAX4527 operate from a single supply between +4.5V and +36V when V- is connected to GND. Observe all of the bipolar precautions when operating from a single supply.

Applications Information

The MAX4526/MAX4527 are designed for DC and low-frequency-signal phase-reversal applications. Both DC and AC symmetry are optimized for use with ±15V supplies.

Signal Phase/Polarity Reversal

The MAX4526/MAX4527 can reverse the phase or polarity of a pair of signals that are out-of-phase and balanced to ground. This is done by routing signals through the MAX4526/MAX4527 and under control of the IN pin, reversing the two signals paths inside the switch before sending out to a balanced output. Figure 1 shows a typical example. **The MAX4526/MAX4527 cannot reverse the phase or polarity of a single-grounded signal, as can be done with an inverting op amp or transformer.**

Balanced Modulators/Demodulators

The MAX4526/MAX4527 can be used as a balanced modulator/demodulator at carrier frequencies up to 100kHz (Figure 2). Higher frequencies are possible, but as frequency increases, small imbalances in the MAX4526/MAX4527's internal capacitance and resistance gradually impair performance. Similarly, imbalances in external circuit capacitance and resistance to GND reduce overall carrier suppression.

The carrier is applied as a logic-level square wave to IN. (Note that this voltage can go as negative as V-.) For best carrier suppression, the power-supply voltages should be equal, the square wave should have a precise 50% duty cycle, and both the input and output signals should be symmetrical about ground. Bypass V+ and V- to GND with 0.1µF ceramic capacitors, as close to the IC pins as possible. Since the logic-level translator/driver in the MAX4526 is faster than the one in the MAX4527, it gives better results at higher frequencies. In critical applications, carrier suppression can be optimized by trimming duty cycle, DC bias around GND, or external source and load capacitance.

In signal lines, balancing both capacitance and resistance to GND produces the best carrier suppression.

Transformer coupling of input and output signals provides the best isolation and carrier suppression. Transformers can also provide signal filtering, impedance matching, or low-noise voltage gain. Use a center-tapped transformer or high-resistance voltage divider to provide a DC path to GND on either the input signal or output signal. This ensures a DC path to GND and symmetrical operation of the internal switches.

Test Circuits/Timing Diagrams

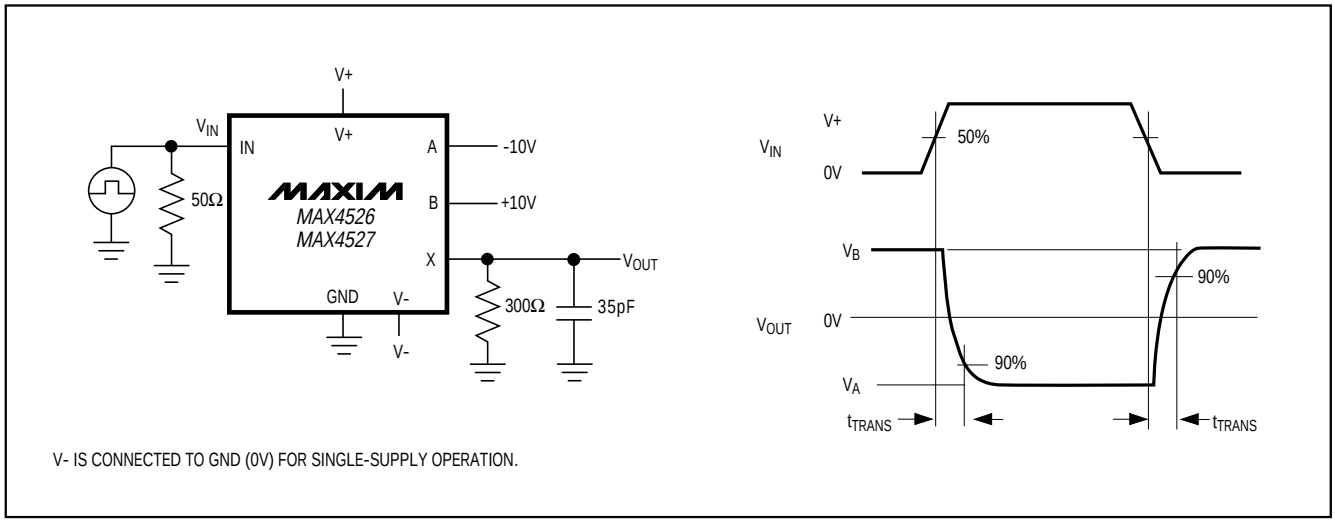


Figure 3. Address Transition Time

Test Circuits/Timing Diagrams (continued)

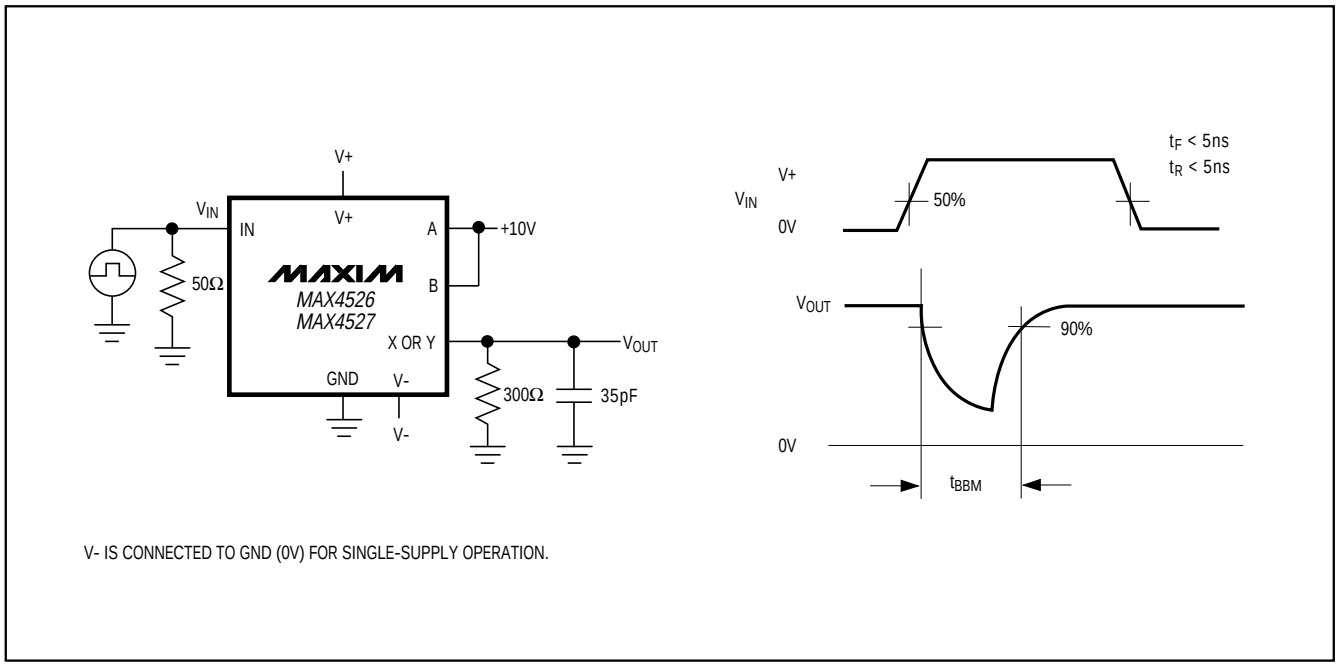


Figure 4. Break-Before-Make Interval

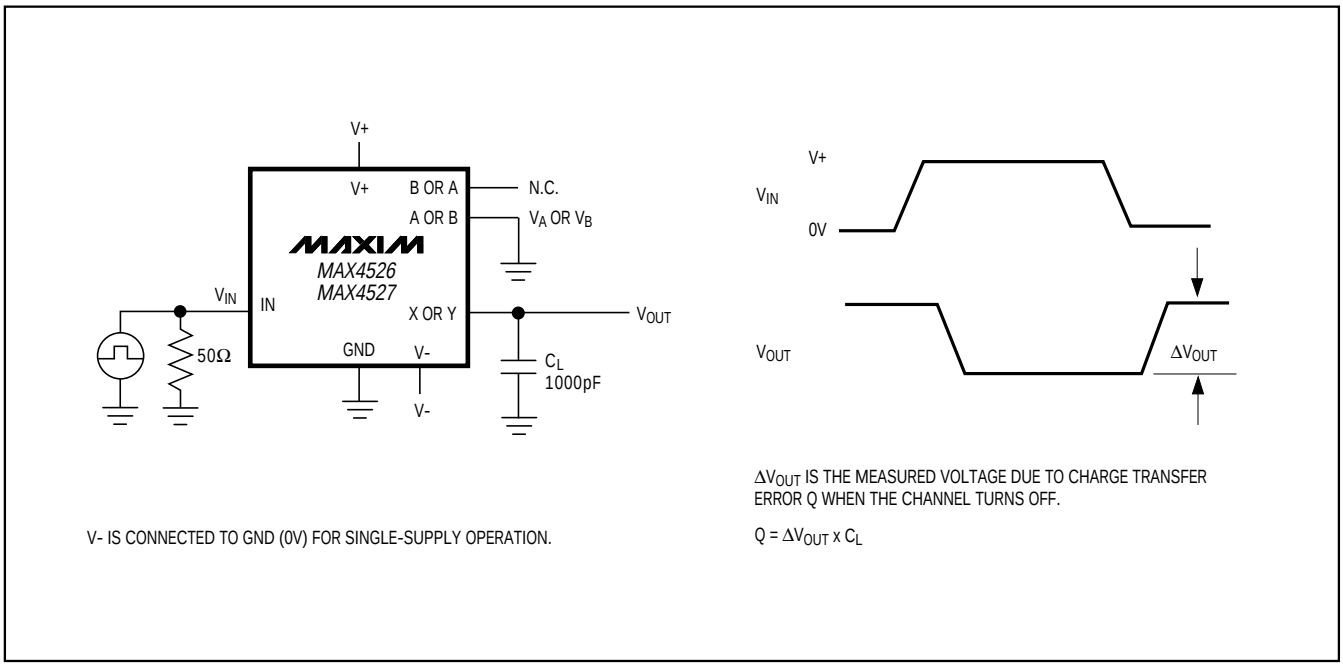


Figure 5. Charge Injection

Test Circuits/Timing Diagrams (continued)

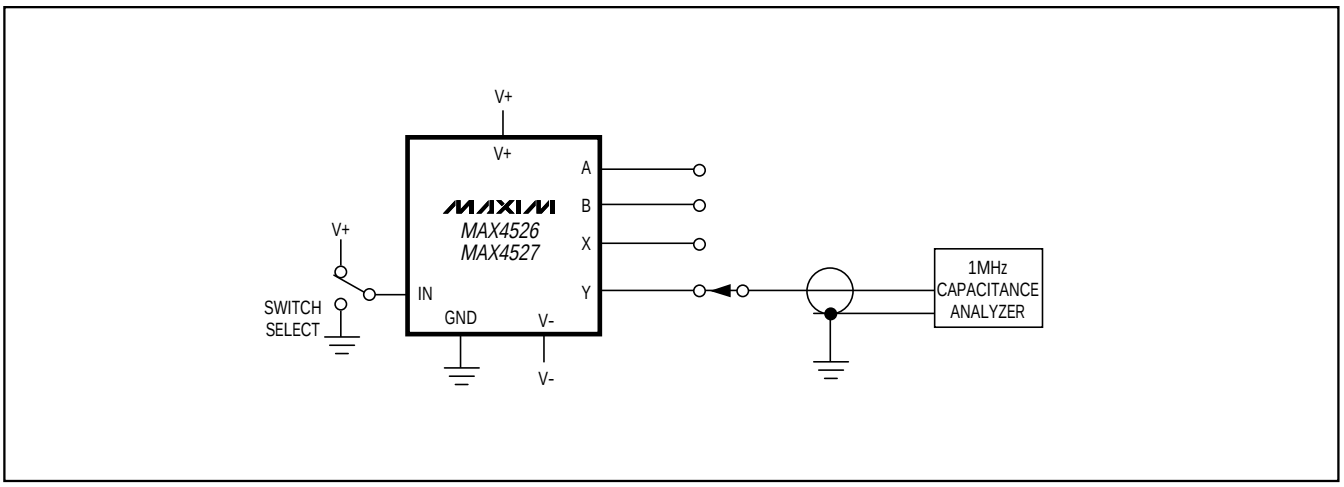


Figure 6. A, B, X, Y Capacitance

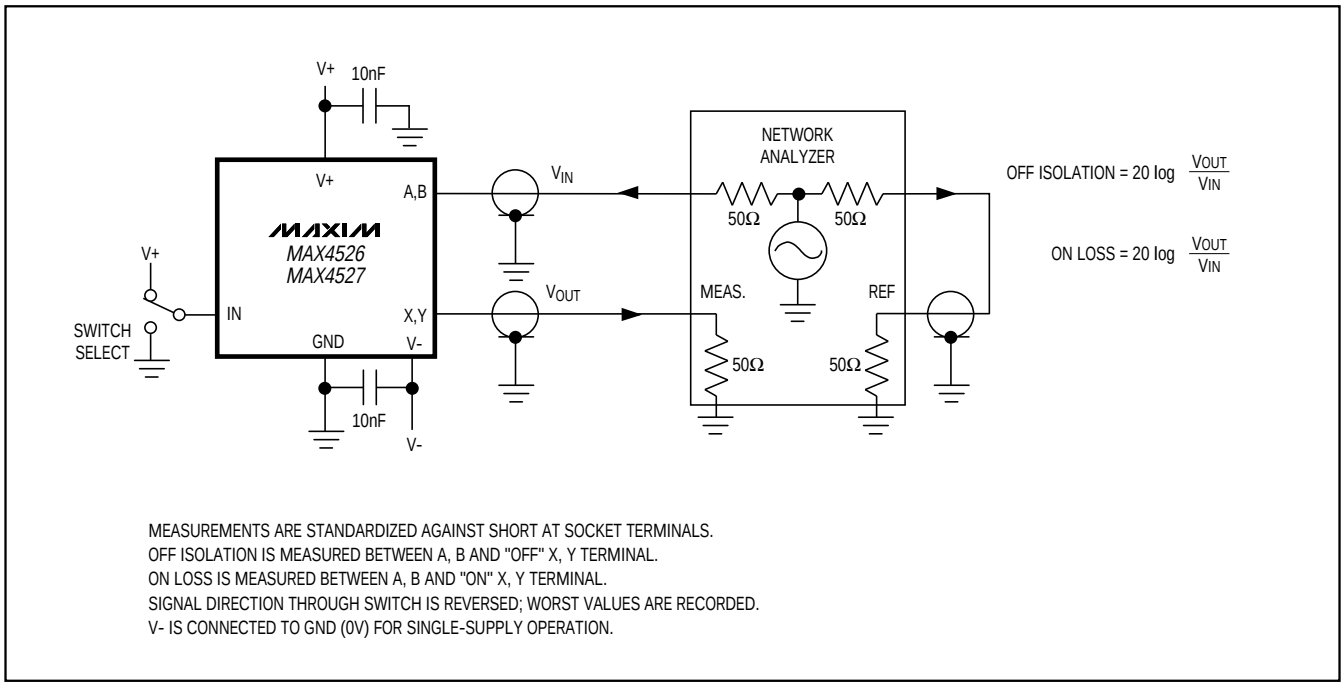


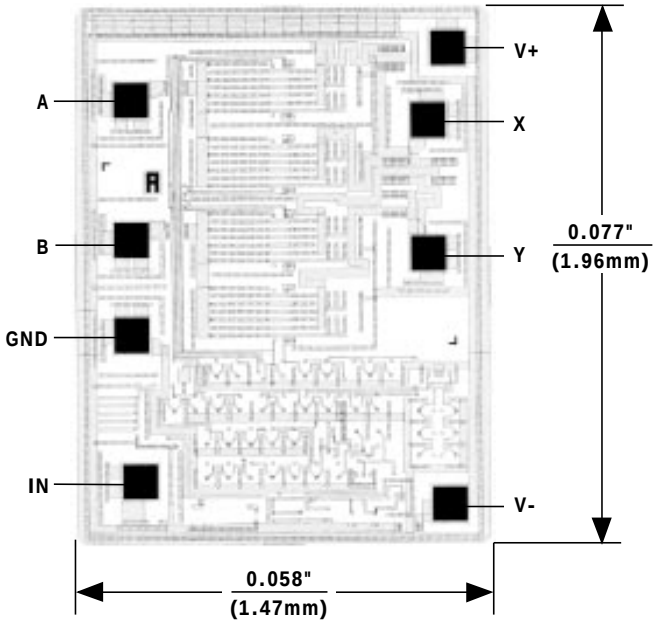
Figure 7. Off Isolation and On Loss

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4527CPA	0°C to +70°C	8 Plastic DIP
MAX4527CSA	0°C to +70°C	8 SO
MAX4527CUA	0°C to +70°C	8 µMAX
MAX4527C/D	0°C to +70°C	Dice*
MAX4527EPA	-40°C to +85°C	8 Plastic DIP
MAX4527ESA	-40°C to +85°C	8 SO
MAX4527EUA	-40°C to +85°C	8 µMAX

**Contact factory for availability.*

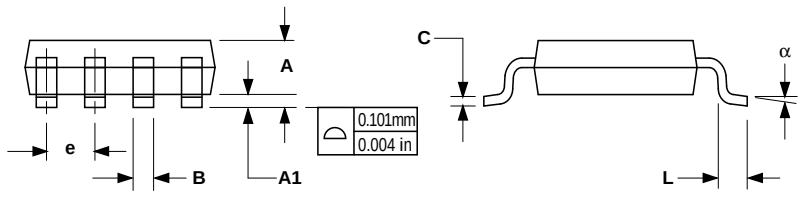
_____Chip Topography

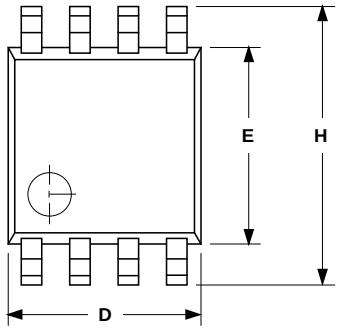


TRANSISTOR COUNT: 50

SUBSTRATE IS INTERNALLY CONNECTED TO V+

_____Package Information





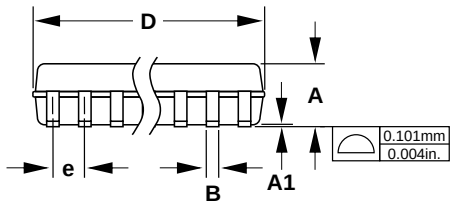
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
E	0.116	0.120	2.95	3.05
e	0.0256		0.65	
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°

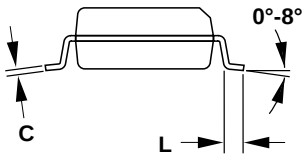
21-0036D

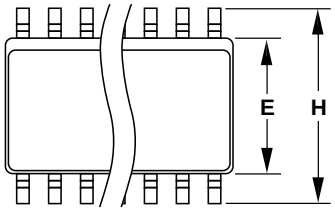
8-PIN µMAX
MICROMAX SMALL-OUTLINE
PACKAGE

Phase-Reversal Analog Switches

Package Information (continued)





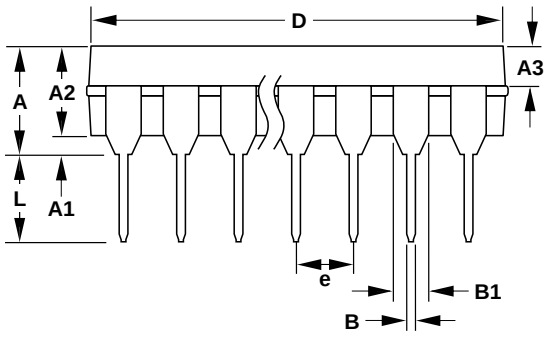


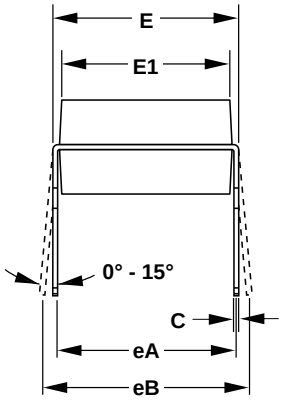
Narrow SO SMALL-OUTLINE PACKAGE (0.150 in.)

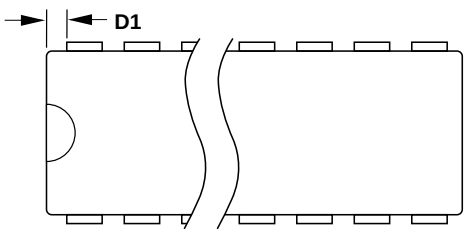
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.189	0.197	4.80	5.00
D	14	0.337	0.344	8.55	8.75
D	16	0.386	0.394	9.80	10.00

21-0041A







Plastic DIP PLASTIC DUAL-IN-LINE PACKAGE (0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043A