

LV5856MX

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V _{IN} pin voltage	V _{IN}		8 to 18	V
BOOT pin voltage	V _{BT}		-0.3 to 23	V
SW pin voltage	V _{SW}		-0.4 to V _{IN}	V
BOOT pin-SW pin voltage	V _{BS-SW}		6.5	V
EN voltage	V _{EN}		18	V
FB, COMP, SS pin voltage	V _{FSO}		6	V

Electrical Characteristics at Ta = 25°C, V_{IN} = 12V, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
IC current drain at standby	I _{CC1}	EN=0V		60		μA
IC current drain in operation	I _{CC2}	EN=5V, FB=1V		2.5		mA
Efficiency	Effcy	V _{IN} =12V, I _{OUT} =1A, V _o =5V, Design target *2		93		%
Reference voltage	V _{ref}	V _{IN} =8V to 28V (±2%)	-2%	0.923	+2%	V
FB pin bias current	I _{ref}	FB=0.923V		10	100	nA
High-side ON resistance	R _{onH}	BOOT=5V, I _{OUT} =1A		0.13		Ω
Low-side ON resistance	R _{onL}			0.13		Ω
Oscillation frequency	f _{OSC}			340		kHz
Oscillation frequency during short-circuit protection	f _{OSCS}			100		kHz
EN high-threshold voltage	V _{enth}			1.5		V
Maximum ON DUTY	D max		80			%
Minimum ON DUTY	D min				8	%
SW Peak Current limit	I _{cl1}	V _{IN} =12V, V _{OUT} =5V, L=10μH	4			A
Thermal shutdown temperature	T _{sd}	*Design guarantee *3		160		°C
Thermal shutdown temperature hysteresis	D _{tsd}	*Design guarantee *3		40		°C
Soft start current	I _{SS}	SS=0V		6		μA
Discharge On-Resistance	V _{SWON}			35		Ω
V _{IN} UVLO lock voltage	V _{UVLO^L}			6.0		V
V _{IN} UVLO lock release voltage	V _{UVLO^H}			6.9		V

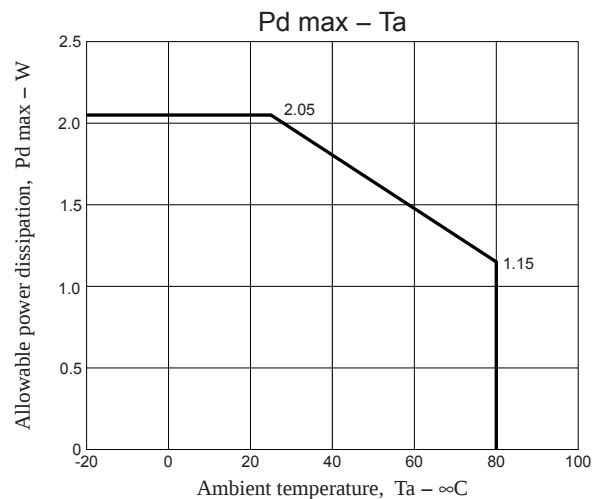
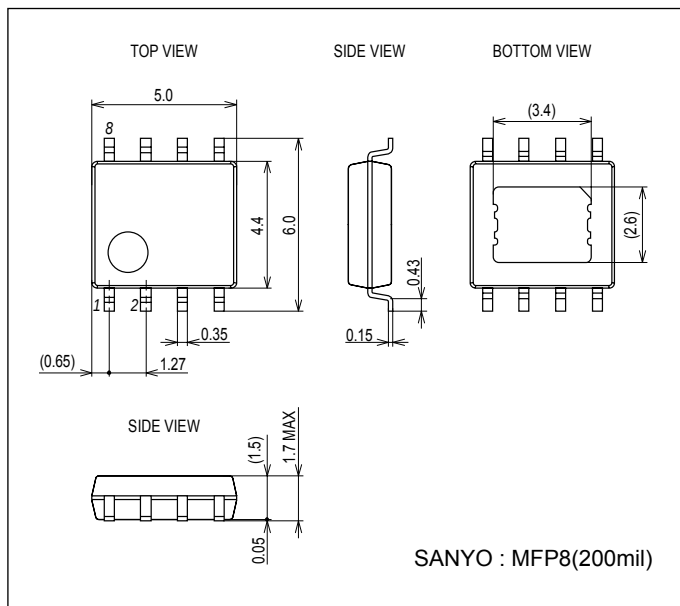
*2: Reference value (not tested before shipment)

*2: Design guarantee (value guaranteed by design and not tested before shipment)

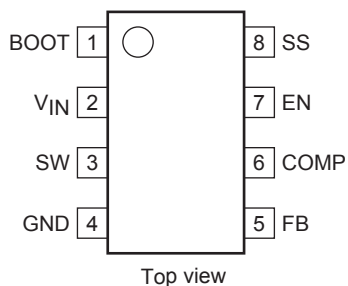
Package Dimensions

unit : mm (typ)

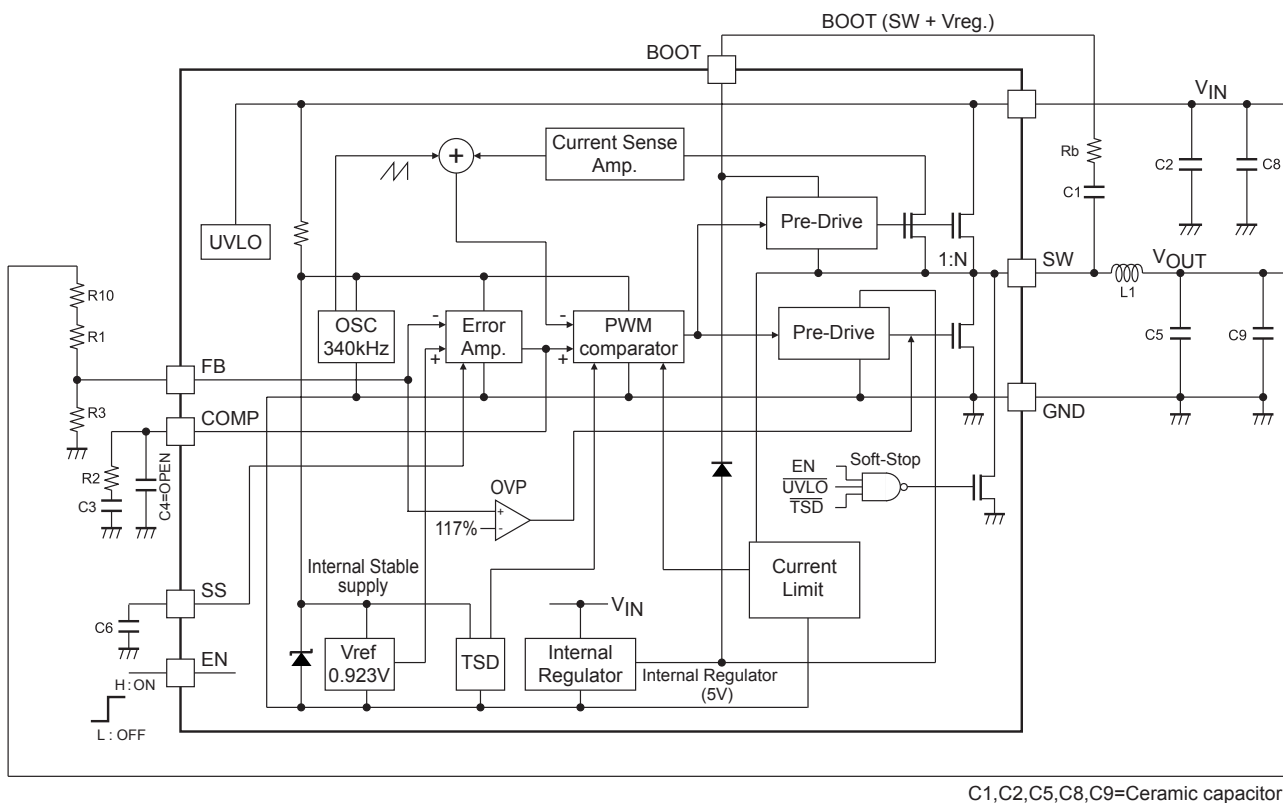
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Pin Assignment



Block Diagram and Sample Application Circuit



Pin Function

Pin No.	Pin name	Function	Equivalent circuit
1	BOOT	Upper MOS transistor boot strap capacitance connection pin. Connect the boot capacitance of about 0.1uF between SW pins. To protect the SW pin's absolute maximum rating , to ensure stable operation, and to eliminate noise , the boot capacitance serial resistance (about 15Ω) Rb proves effective.	
2	V _{IN}	Input Voltage Pin. Connect substantially large (10uF 2 parallel or more) capacitance between this pin and GND.	
3	SW	Power Switch pin. Connect the output LC filter. Connect the above capacitance between this pin and BOOT pin. The discharge transistor for a Soft-Stop is connected with this terminal (typical 35Ω). It turns it on by either EN=L, UVLO or a thermal shutdown.	
4	GND	Ground pin.	
5	FB	Feedback pin. Set the output voltage by means of split resistor in the section of the output voltage V _{OUT} -FB-GND. V _{OUT} setting is made as calculated below. $V_{OUT} = V_{ref} \times \left\{ 1 + \frac{(R1 + R10)}{R3} \right\}$ $V_{ref} = 0.923V$ Example: 3.3V output voltage (See, Block Diagram and Application example) $V_{OUT} = 0.923 \times \left\{ 1 + \frac{(22k + 3.9k)}{10k} \right\}$ $= 3.314V$	
8	SS	Soft start pin. Sets the soft start time by means of the built-in 6μA source voltage and external soft start capacity. The soft start capacity C6 can be set as follows: $C6 = 6\mu A \times \frac{T_{ss}}{V_{ref}}$ Where, T _{ss} is the soft start time and V _{ref} is the reference voltage. Example: 2.3ms soft start time achieved $C6 = 6\mu A \times \frac{2.3ms}{0.923V} = 0.015\mu F$	
6	COMP	Phase compensation pin. Connects with the phase compensation external capacitance and resistance of DC/DC converter close loop.	
7	EN	Enable pin. Converter enabled when set to the HIGH voltage and disabled when LOW voltage or OPEN state.	

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