Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V_{IN} pin voltage	V_{IN}		8 to 18	V
BOOT pin voltage	V_{BT}		-0.3 to 23	V
SW pin voltage	V_{SW}		-0.4 to V_{IN}	V
BOOT pin-SW pin voltage	V_{BS-SW}		6.5	V
EN voltage	V_{EN}		18	V
FB, COMP, SS pin voltage	V_{FSO}		6	V

Electrical Characteristics at Ta = 25°C, V_{IN} = 12V, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
IC current drain at standby	$I_{CC}1$	EN=0V		60		μA
IC current drain in operation	$I_{CC}2$	EN=5v, FB=1V		2.5		mA
Efficiency	Effcy	V_{IN}=12V, I_{OUT}=1A, Vo=5V, Design target *2		93		%
Reference voltage	Vref	V_{IN}=8V to 28V (±2%)	-2%	0.923	+2%	V
FB pin bias current	Iref	FB=0.923V		10	100	nA
High-side ON resistance	RonH	BOOT=5V, I_{OUT}=1A		0.13		Ω
Low-side ON resistance	RonL			0.13		Ω
Oscillation frequency	f_{OSC}			340		kHz
Oscillation frequency during short-circuit protection	f_{OSCS}			100		kHz
EN high-threshold voltage	Venth			1.5		V
Maximum ON DUTY	D max		80			%
Minimum ON DUTY	D min				8	%
SW Peak Current limit	Icl1	V_{IN}=12V, V_{OUT}=5V, L=10μH	4			A
Thermal shutdown temperature	Ttsd	*Design guarantee *3		160		°C
Thermal shutdown temperature hysteresis	Dtsd	*Design guarantee *3		40		°C
Soft start current	I_{SS}	SS=0V		6		μA
Discharge On-Resistance	V_{SW}ON			35		Ω
V_{IN} UVLO lock voltage	V_{UVLO}L			6.0		V
V_{IN} UVLO lock release voltage	V_{UVLO}H			6.9		V

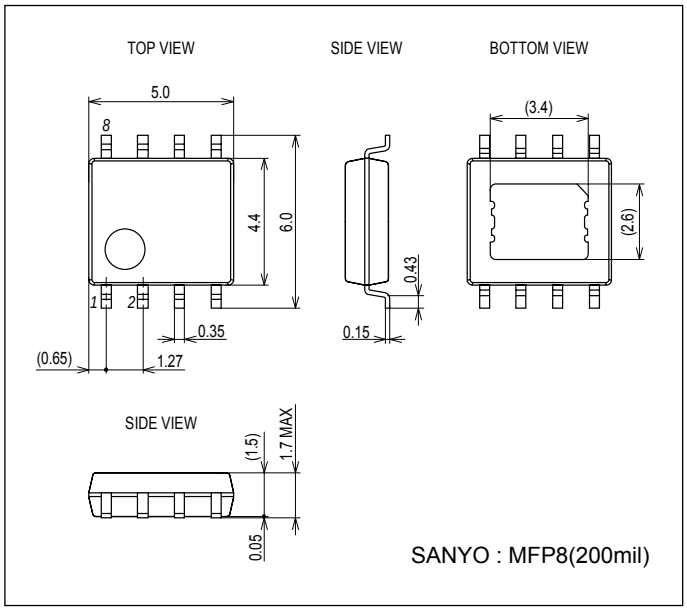
*2: Reference value (not tested before shipment)

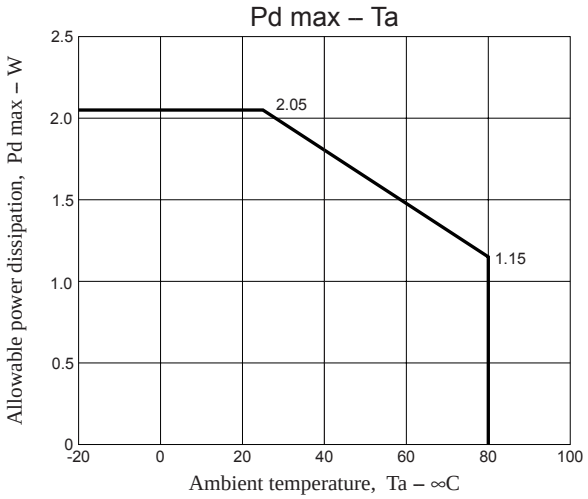
*2: Design guarantee (value guaranteed by design and not tested before shipment)

Package Dimensions

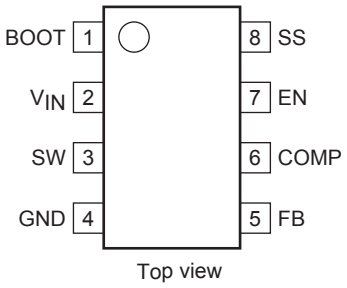
unit : mm (typ)

3372

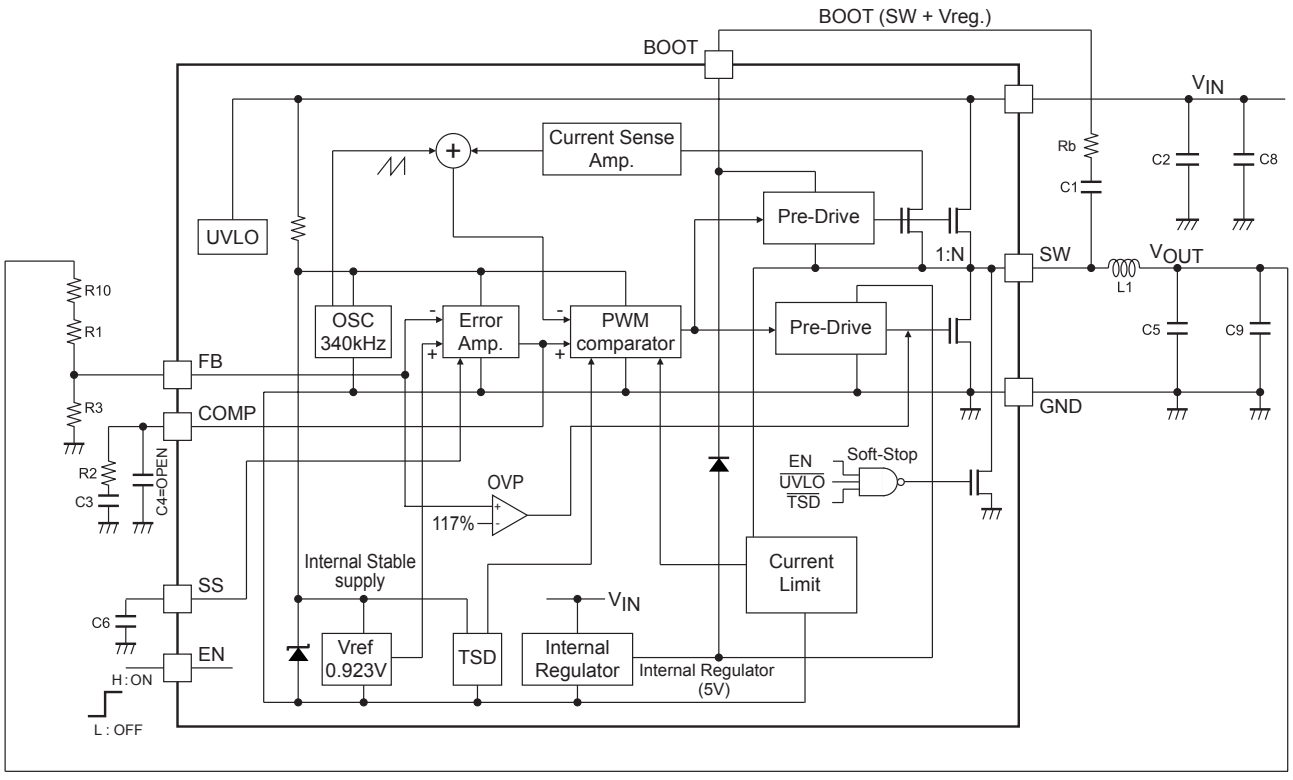




Pin Assignment

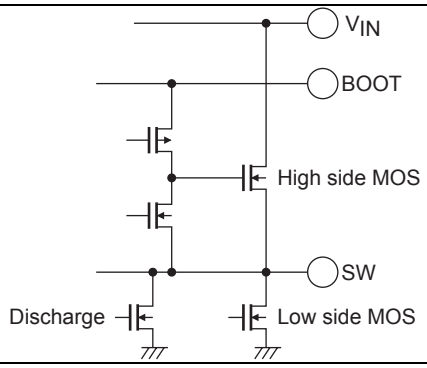
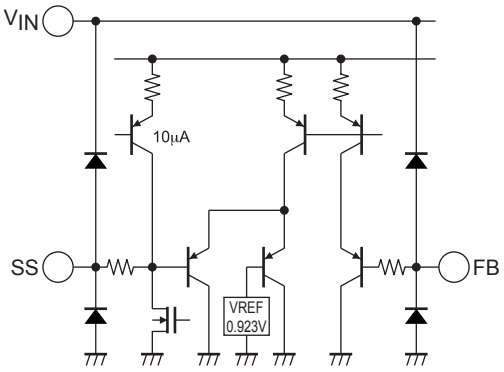
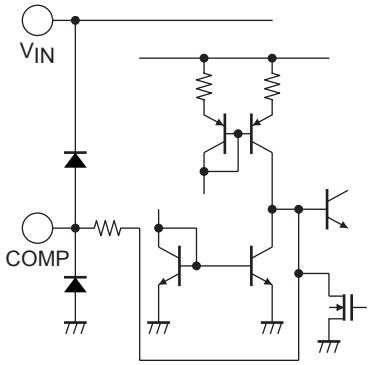


Block Diagram and Sample Application Circuit



C1,C2,C5,C8,C9=Ceramic capacitor

Pin Function

Pin No.	Pin name	Function	Equivalent circuit
1	BOOT	Upper MOS transistor boot strap capacitance connection pin. Connect the boot capacitance of about 0.1uF between SW pins. To protect the SW pin's absolute maximum rating , to ensure stable operation, and to eliminate noise , the boot capacitance serial resistance (about 15Ω) Rb proves effective.	
2	V_{IN}	Input Voltage Pin. Connect substantially large (10uF 2 parallel or more) capacitance between this pin and GND.	
3	SW	Power Switch pin. Connect the output LC filter. Connect the above capacitance between this pin and BOOT pin. The discharge transistor for a Soft-Stop is connected with this terminal (typcal 35Ω). It turns it on by either EN=L, UVLO or a thermal shutdown.	
4	GND	Ground pin.	
5	FB	Feedback pin. Set the output voltage by means of split resistor in the section of the output voltage VOUT-FB-GND. VOUT setting is made as calculated below. $V_{OUT} = Vref \times \{ 1 + \frac{(R1 + R10)}{R3} \}$ Vref = 0.923V Example: 3.3V output voltage (See, Block Diagram and Application example) $V_{OUT} = 0.923 \times \{ 1 + \frac{(22k + 3.9k)}{10k} \}$ =3.314V	
8	SS	Soft start pin. Sets the soft start time by means of the built-in 6μA source voltage and external soft start capacity. The soft start capacity C6 can be set as follows: $C6 = 6\mu A \times \frac{Tss}{Vref}$ Where, Tss is the soft start time and Vref is the reference voltage. Example:2.3ms soft start time achieved $C6 = 6\mu A \times \frac{2.3ms}{0.923V} = 0.015\mu F$	
6	COMP	Phase compensation pin. Connects with the phase compensation external capacitance and resistance of DC/DC converter close loop.	
7	EN	Enable pin. Converter enabled when set to the HIGH voltage and disabled when LOW voltage or OPEN state.