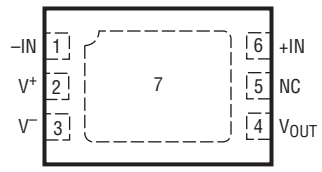
ABSOLUTE MAXIMUM RATINGS

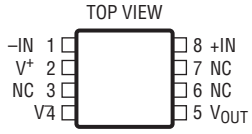
(Notes 1, 2)

Differential Input Voltage (+IN – –IN) ..... ±44V
Input Voltage V(+IN, –IN) to V^- ..... –9.5V to 44V
Total V^+ Supply Voltage from V^- 36V
Output Voltage ..... V^- to (V^- + 36V)
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4)
LT6105C ..... –40°C to 85°C
LT6105I ..... –40°C to 85°C
LT6105H ..... –40°C to 125°C
Specified Temperature Range (Note 5)
LT6105C ..... 0°C to 70°C
LT6105I ..... –40°C to 85°C
LT6105H ..... –40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSOP ..... 300°C

PIN CONFIGURATION



DCB PACKAGE
6-LEAD (2mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 64°C/W
EXPOSED PAD (PIN 7) CONNECTED TO V^- (PIN 3)



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 250°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT6105CDCB#TRMPBF	LT6105CDCB#TRPBF	LCTF	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LT6105IDCB#TRMPBF	LT6105IDCB#TRPBF	LCTF	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LT6105HDCB#TRMPBF	LT6105HDCB#TRPBF	LCTF	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LT6105CMS8#PBF	LT6105CMS8#TRPBF	LTCTD	8-Lead Plastic MS8	0°C to 70°C
LT6105IMS8#PBF	LT6105IMS8#TRPBF	LTCTD	8-Lead Plastic MS8	–40°C to 85°C
LT6105HMS8#PBF	LT6105HMS8#TRPBF	LTCTD	8-Lead Plastic MS8	–40°C to 125°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range 0°C < T_A < 70°C (LT6105C), otherwise specifications are at T_A = 25°C. V^+ = 12V, V^- = 0V, V_S^+ = 12V (see Figure 1), R_{IN1} = R_{IN2} = 100Ω, R_{OUT} = 5k (A_V = 50), V_{SENSE} = V_S^+ – V_S^-, unless otherwise specified. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_S^+, V_S^-	Input Voltage Range	Guaranteed by CMRR	 ●	–0.3 –0.1		44 44	V V
A_V Error	Voltage Gain Error (Note 6)	V_{SENSE} = 25mV to 75mV, V_S^+ = 12V	 ●	–1 –1.3	0.1	1 1.3	% %
		V_{SENSE} = 25mV to 75mV, V_S^+ = 0V	●	–2.5		2.5	%
V_{OS}	Input Offset Voltage MS8 Package	V_{SENSE} = 5mV	 ●	–0.3 –0.6	–0.1	0.3 0.6	mV mV
	Input Offset Voltage DCB Package	V_{SENSE} = 5mV	 ●	–0.4 –0.7	–0.1	0.4 0.7	mV mV
	Input Offset Voltage	V_{SENSE} = 5mV, V_S^+ = 0V	 ●	–1 –1.3	–0.3	1 1.3	mV mV
$\Delta V_{OS}/\Delta T$	Temperature Coefficient of V_{OS}		●		0.5		µV/°C
CMRR	Input Common Mode Rejection Ratio	V_{SENSE} = 5mV, V_S^+ = 2.8V to 44V	 ●	100 95	120		dB dB
		V_{SENSE} = 5mV, V_S^+ = –0.3V to 44V V_{SENSE} = 5mV, V_S^+ = –0.1V to 44V	 ●	94 90			dB dB
V^+	Power Supply Voltage Range	Guaranteed by PSRR	●	2.85		36	V
PSRR	Power Supply Rejection Ratio	V_{SENSE} = 5mV, V_S^+ = 12V, V^+ = 2.85V to 36V	 ●	98 94	120		dB dB
		V_{SENSE} = 5mV, V_S^+ = 0V, V^+ = 2.85V to 36V	 ●	98 94	120		dB dB
$I_{(+IN)}$, $I_{(–IN)}$	Input Current	V_{SENSE} = 0V, V_S^+ = 3V V_{SENSE} = 0V, V_S^+ = 0V	● ●		15 –0.05	25	µA µA
$I_{(+IN)} – I_{(–IN)}$	Input Offset Current	V_{SENSE} = 0V, V_S^+ = 3V V_{SENSE} = 0V, V_S^+ = 0V	● ●		0.05 0.005	0.5	µA µA
$I_{(+IN)} + I_{(–IN)}$	Input Current (Power-Down)	V^+ = 0V, V_S^+ = 44V, V_{SENSE} = 0V	●		0.03	1	µA
I_S	V^+ Supply Current	V_{SENSE} = 0V, V_S^+ = 3V, V^+ = 2.85V V_{SENSE} = 0V, V_S^+ = 3V, V^+ = 36V	● ●		200 240	300 350	µA µA
$V_{O(MIN)}$	Minimum Output Voltage	V_{SENSE} = 0mV, V_S^+ = 44V, V^+ = 36V	●			35	mV
$V_{O(MAX)}$	Output High (Referred to V^+)	V_{SENSE} = 120mV, A_V = 100, R_{OUT} = 10k	●		1.25	1.5	V
I_{OUT}	Maximum Output Current	Guaranteed by $V_{O(MAX)}$	●	1			mA
I_{SC}	Short-Circuit Output Current	V_S^+ = 44V, V_S^- = 0V, R_{OUT} = 0Ω	●	1.5			mA
BW	–3dB Bandwidth	V_{SENSE} = 50mV, A_V = 10V/V			100		kHz
t_S	Output Settling to 1% of Final Value	V_{SENSE} = 5mV to 100mV			5		µs
t_r	Input Step Response (Note 7)	V_{SENSE} = 5mV to 100mV			3		µs
SR	Slew Rate (Note 8)	V_{SENSE} = 5mV to 150mV, A_V = 50V/V, R_{IN} = 400Ω		1.75	2		V/µs
V_{REV}	Reverse Input Voltage (Referred to V^-)	$I_{(+IN)} + I_{(–IN)}$ = –5mA	●	–9.5	–12		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range –40°C < T_A < 85°C (LT6105I), otherwise specifications are at T_A = 25°C. V^+ = 12V, V^- = 0V, V_S^+ = 12V (see Figure 1), R_{IN1} = R_{IN2} = 100Ω, R_{OUT} = 5k (A_V = 50), V_{SENSE} = V_S^+ – V_S^-, unless otherwise specified. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_S^+, V_S^-	Input Voltage Range	Guaranteed by CMRR	 ●	–0.3 –0.3		44 44	V V
A_V Error	Voltage Gain Error (Note 6)	V_{SENSE} = 25mV to 75mV, V_S^+ = 12V	 ●	–1 –1.4	0.1	1 1.4	% %
		V_{SENSE} = 25mV to 75mV, V_S^+ = 0V	●	–3		3	%
V_{OS}	Input Offset Voltage MS8 Package	V_{SENSE} = 5mV	 ●	–0.3 –0.65	–0.1	0.3 0.65	mV mV
	Input Offset Voltage DCB Package	V_{SENSE} = 5mV	 ●	–0.4 –0.75	–0.1	0.4 0.75	mV mV
	Input Offset Voltage	V_{SENSE} = 5mV, V_S^+ = 0V	 ●	–1 –1.4	–0.3	1 1.4	mV mV
$\Delta V_{OS}/\Delta T$	Temperature Coefficient of V_{OS}		●		0.5		µV/°C
CMRR	Input Common Mode Rejection Ratio	V_{SENSE} = 5mV, V_S^+ = 2.8V to 44V	 ●	100 95	120		dB dB
		V_{SENSE} = 5mV, V_S^+ = –0.3V to 44V V_{SENSE} = 5mV, V_S^+ = –0.1V to 44V	 ●	94 90			dB dB
V^+	Power Supply Voltage Range	Guaranteed by PSRR	●	2.85		36	V
PSRR	Power Supply Rejection Ratio	V_{SENSE} = 5mV, V_S^+ = 12V, V^+ = 2.85V to 36V	 ●	98 94	120		dB dB
		V_{SENSE} = 5mV, V_S^+ = 0V, V^+ = 2.85V to 36V	 ●	98 94	120		dB dB
$I_{(+IN)}$, $I_{(–IN)}$	Input Current	V_{SENSE} = 0V, V_S^+ = 3V V_{SENSE} = 0V, V_S^+ = 0V	● ●		16 –0.05	27	µA µA
$I_{(+IN)} – I_{(–IN)}$	Input Offset Current	V_{SENSE} = 0V, V_S^+ = 3V V_{SENSE} = 0V, V_S^+ = 0V	● ●		0.08 0.01	0.6	µA µA
$I_{(+IN)} + I_{(–IN)}$	Input Current (Power-Down)	V^+ = 0V, V_S^+ = 44V, V_{SENSE} = 0V	●		0.035	1	µA
I_S	V^+ Supply Current	V_{SENSE} = 0V, V_S^+ = 3V, V^+ = 2.85V V_{SENSE} = 0V, V_S^+ = 3V, V^+ = 36V	● ●		200 250	325 375	µA µA
$V_{O(MIN)}$	Minimum Output Voltage	V_{SENSE} = 0mV, V_S^+ = 44V, V^+ = 36V	●			40	mV
$V_{O(MAX)}$	Output High (Referred to V^+)	V_{SENSE} = 120mV, A_V = 100, R_{OUT} = 10k	●		1.27	1.6	V
I_{OUT}	Maximum Output Current	Guaranteed by $V_{O(MAX)}$	●	1			mA
I_{SC}	Short-Circuit Output Current	V_S^+ = 44V, V_S^- = 0V, R_{OUT} = 0Ω	●	1.5			mA
BW	–3dB Bandwidth	V_{SENSE} = 50mV, A_V = 10V/V			100		kHz
t_S	Output Settling to 1% of Final Value	V_{SENSE} = 5mV to 100mV			5		µs
t_r	Input Step Response (Note 7)	V_{SENSE} = 5mV to 100mV			3		µs
SR	Slew Rate (Note 8)	V_{SENSE} = 5mV to 150mV, A_V = 50V/V, R_{IN} = 400Ω		1.75	2		V/µs
V_{REV}	Reverse Input Voltage (Referred to V^-)	$I_{(+IN)} + I_{(–IN)}$ = –5mA	●	–9.5	–12		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range –40°C < T_A < 125°C (LT6105H), otherwise specifications are at T_A = 25°C. V^+ = 12V, V^- = 0V, V_S^+ = 12V (see Figure 1), R_{IN1} = R_{IN2} = 100Ω, R_{OUT} = 5k (A_V = 50), V_{SENSE} = V_S^+ – V_S^-, unless otherwise specified. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_S^+, V_S^-	Input Voltage Range	Guaranteed by CMRR	 ●	–0.3 –0.1		44 44	V V
A_V Error	Voltage Gain Error (Note 6)	V_{SENSE} = 25mV to 75mV, V_S^+ = 12V	 ●	–1 –1.5	0.1	1 1.5	% %
		V_{SENSE} = 25mV to 75mV, V_S^+ = 0V	●	–3.25		3.25	%
V_{OS}	Input Offset Voltage MS8 Package	V_{SENSE} = 5mV	 ●	–0.3 –0.8	–0.1	0.3 0.8	mV mV
	Input Offset Voltage DCB Package	V_{SENSE} = 5mV	 ●	–0.4 –0.9	–0.1	0.4 0.9	mV mV
	Input Offset Voltage	V_{SENSE} = 5mV, V_S^+ = 0V	 ●	–1 –1.6	–0.3	1 1.6	mV mV
$\Delta V_{OS}/\Delta T$	Temperature Coefficient of V_{OS}		●		0.5		µV/°C
CMRR	Input Common Mode Rejection Ratio	V_{SENSE} = 5mV, V_S^+ = 2.8V to 44V	 ●	100 95	120		dB dB
		V_{SENSE} = 5mV, V_S^+ = –0.3V to 44V V_{SENSE} = 5mV, V_S^+ = –0.1V to 44V	 ●	94 80			dB dB
V^+	Power Supply Voltage Range	Guaranteed by PSRR	●	2.85		36	V
PSRR	Power Supply Rejection Ratio	V_{SENSE} = 5mV, V_S^+ = 12V, V^+ = 2.85V to 36V	 ●	98 94	120		dB dB
		V_{SENSE} = 5mV, V_S^+ = 0V, V^+ = 2.85V to 36V	 ●	98 94	120		dB dB
$I_{(+IN)}$, $I_{(–IN)}$	Input Current	V_{SENSE} = 0V, V_S^+ = 3V V_{SENSE} = 0V, V_S^+ = 0V	● ●		18 –0.05	30	µA µA
$I_{(+IN)} – I_{(–IN)}$	Input Offset Current	V_{SENSE} = 0V, V_S^+ = 3V V_{SENSE} = 0V, V_S^+ = 0V	● ●		0.35 0.1	0.8	µA µA
$I_{(+IN)} + I_{(–IN)}$	Input Current (Power-Down)	V^+ = 0V, V_S^+ = 44V, V_{SENSE} = 0V	●		0.5	2.5	µA
I_S	V^+ Supply Current	V_{SENSE} = 0V, V_S^+ = 3V, V^+ = 2.85V V_{SENSE} = 0V, V_S^+ = 3V, V^+ = 36V	● ●		240 300	350 450	µA µA
$V_{O(MIN)}$	Minimum Output Voltage	V_{SENSE} = 0mV, V_S^+ = 44V, V^+ = 36V	●			45	mV
$V_{O(MAX)}$	Output High (Referred to V^+)	V_{SENSE} = 120mV, A_V = 100, R_{OUT} = 10k	●		1.3	1.7	V
I_{OUT}	Maximum Output Current	Guaranteed by $V_{O(MAX)}$	●	1			mA
I_{SC}	Short-Circuit Output Current	V_S^+ = 44V, V_S^- = 0V, R_{OUT} = 0Ω	●	1.5			mA
BW	–3dB Bandwidth	V_{SENSE} = 50mV, A_V = 10V/V			100		kHz
t_S	Output Settling to 1% of Final Value	V_{SENSE} = 5mV to 100mV			5		µs
t_r	Input Step Response (Note 7)	V_{SENSE} = 5mV to 100mV			3		µs
SR	Slew Rate (Note 8)	V_{SENSE} = 5mV to 150mV, A_V = 50V/V, R_{IN} = 400Ω		1.75	2		V/µs
V_{REV}	Reverse Input Voltage (Referred to V^-)	$I_{(+IN)} + I_{(–IN)}$ = –5mA	●	–9.5	–12		V

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: ESD (Electrostatic Discharge) sensitive devices. Extensive use of ESD protection devices are used internal to the LT6105, however, high electrostatic discharge can damage or degrade the device. Use proper ESD handling precautions.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum ratings.

Note 4: The LT6105C/LT6105I are guaranteed functional over the operating temperature range of –40°C to 85°C. The LT6105H is guaranteed functional over the operating temperature range of –40°C to 125°C.

Note 5: The LT6105C is guaranteed to meet specified performance from 0°C to 70°C. The LT6105C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LT6105I is guaranteed to meet specified performance from –40°C to 85°C. The LT6105H is guaranteed to meet specified performance from –40°C to 125°C.

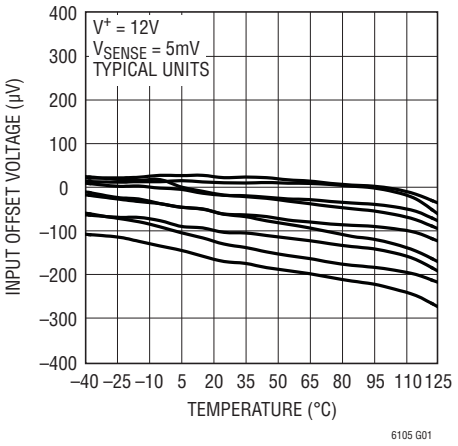
Note 6: 0.01% tolerance external resistors are used.

Note 7: t_r is measured from the input to the 2.5V point on the 5V output.

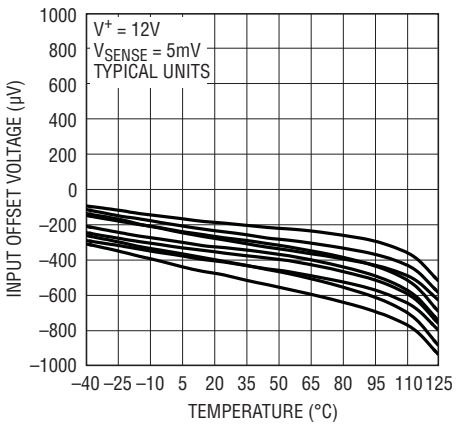
Note 8: Slew rate is measured on the output between 1V and 5V.

TYPICAL PERFORMANCE CHARACTERISTICS

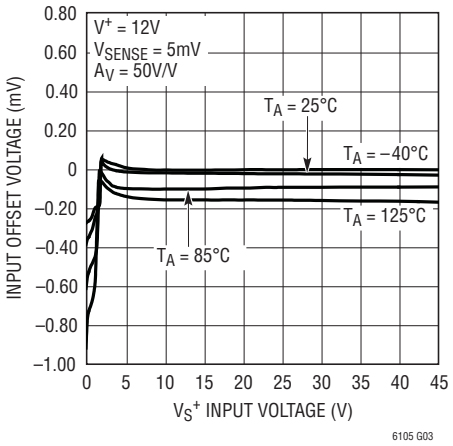
Input Offset Voltage vs Temperature, V_S^+ = 12V



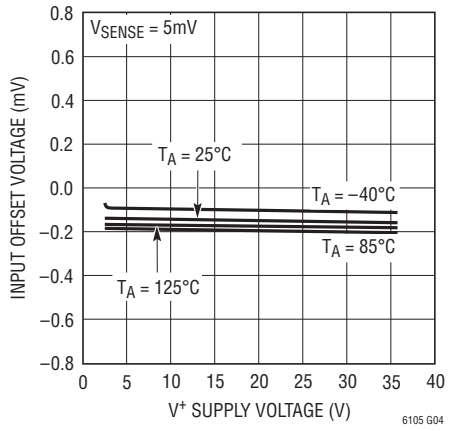
Input Offset Voltage vs Temperature, V_S^+ = 0V



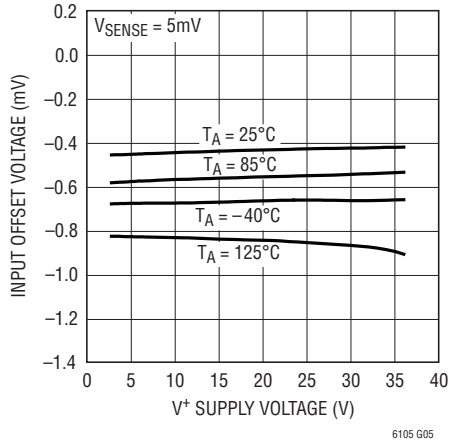
Input Offset Voltage vs Input Voltage



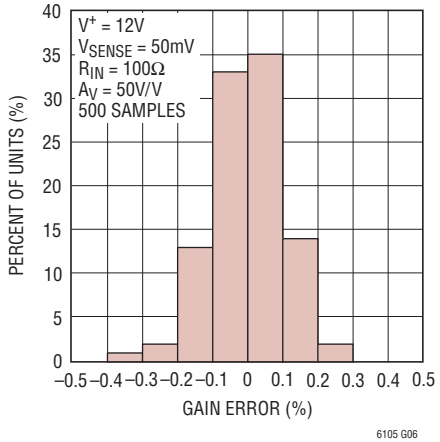
Input Offset Voltage vs Supply Voltage, V_S^+ = 12V



Input Offset Voltage vs Supply Voltage, V_S^+ = 0V

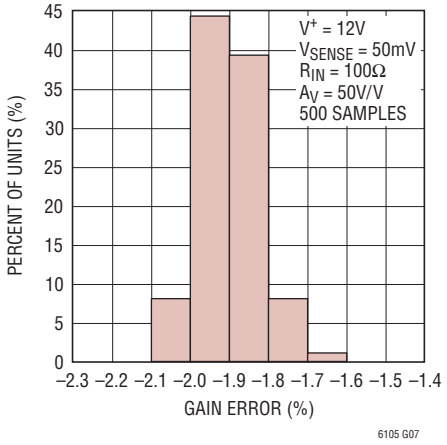


Gain Error Distribution, V_S^+ = 12V

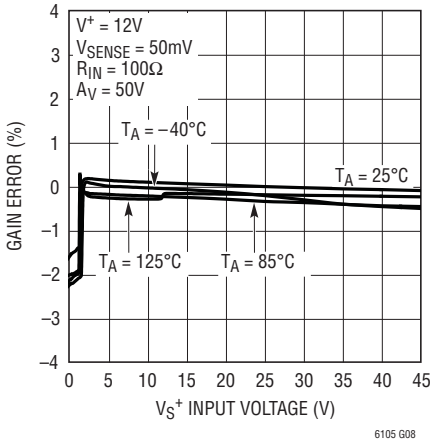


TYPICAL PERFORMANCE CHARACTERISTICS

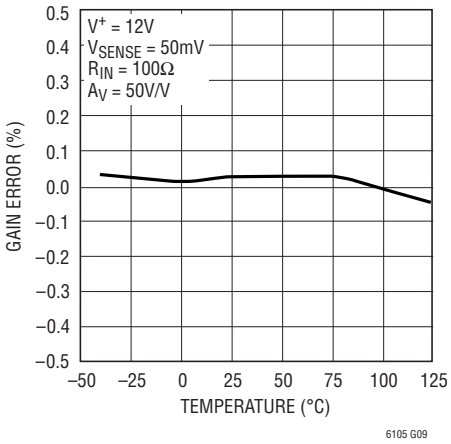
Gain Error Distribution, $V_S^+ = 0V$



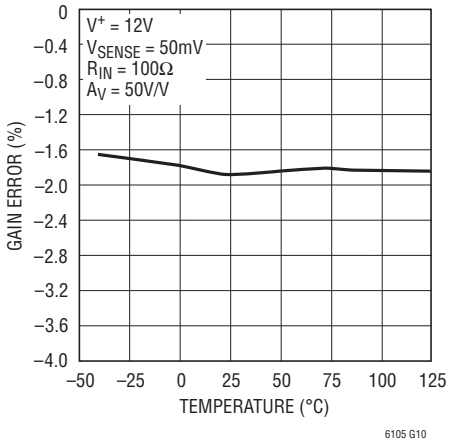
Gain Error vs Input Voltage



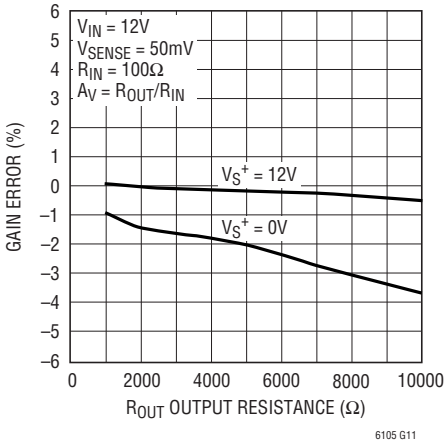
Gain Error vs Temperature, $V_S^+ = 12V$



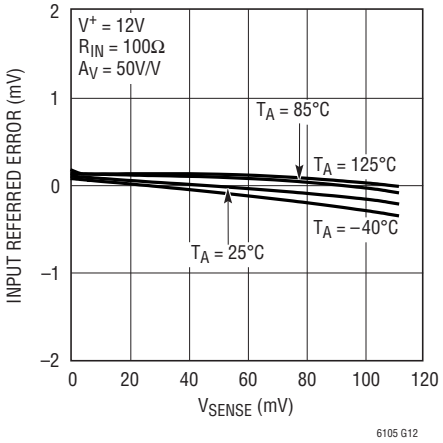
Gain Error vs Temperature, $V_S^+ = 0V$



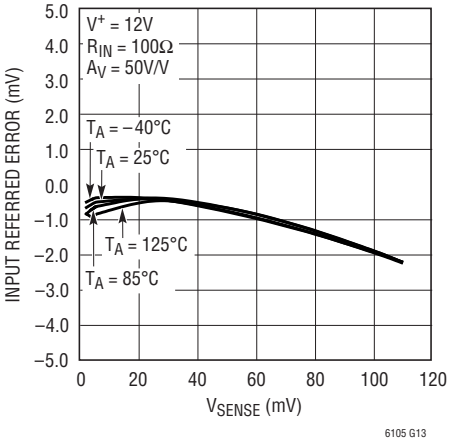
Gain Error vs Output Resistance



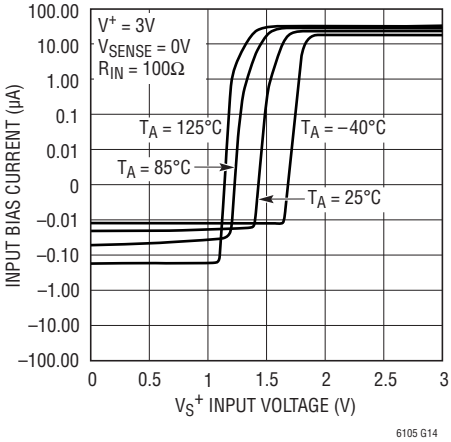
Input Referred Voltage Error vs V_{SENSE}, $V_S^+ = 12V$



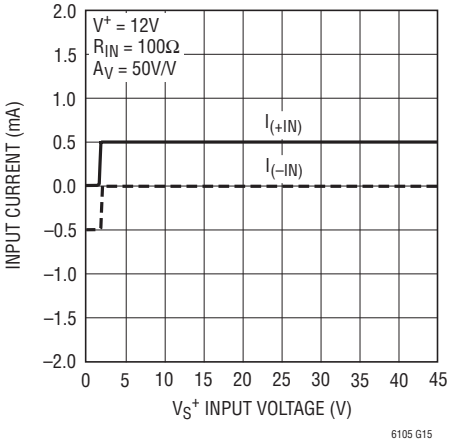
Input Referred Voltage Error vs V_{SENSE}, $V_S^+ = 0V$



Input Bias Current vs Input Voltage

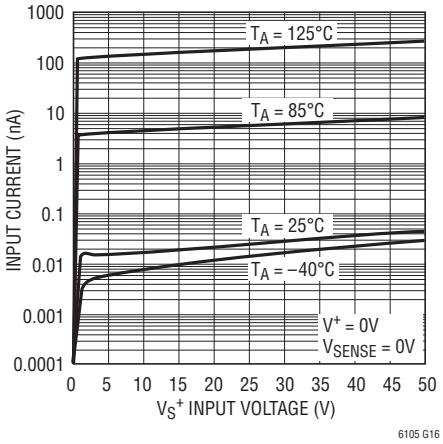


Input Current vs Input Voltage, $V_{SENSE} = 50mV$

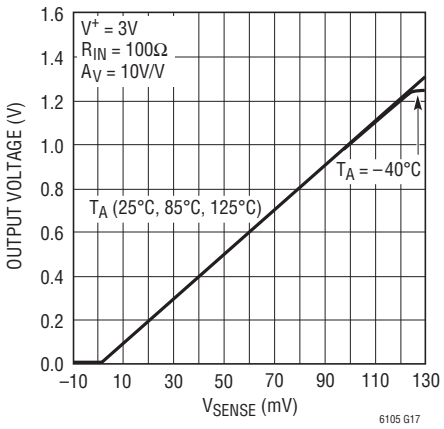


TYPICAL PERFORMANCE CHARACTERISTICS

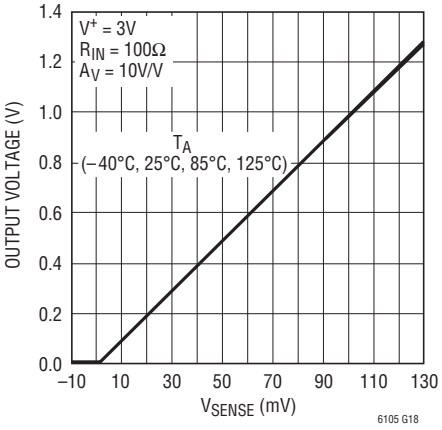
Input Current (V^+ Powered Down) vs Input Voltage



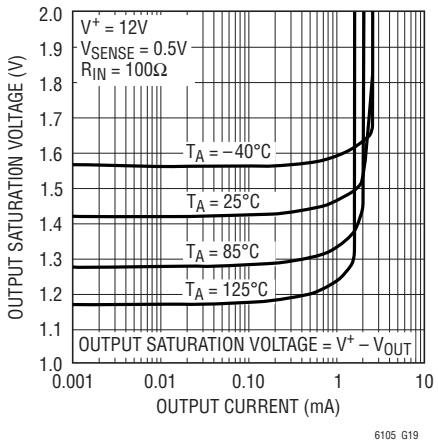
Output Voltage vs V_{SENSE} Voltage, V_S^+ = 12V



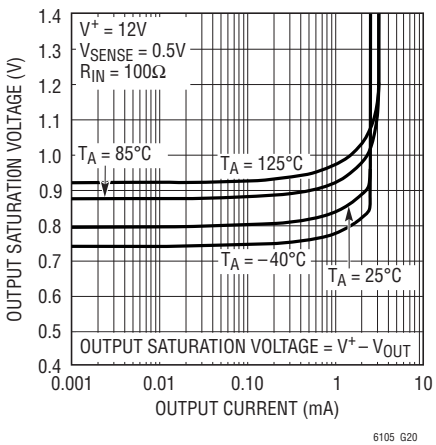
Output Voltage vs V_{SENSE} Voltage, V_S^+ = 0V



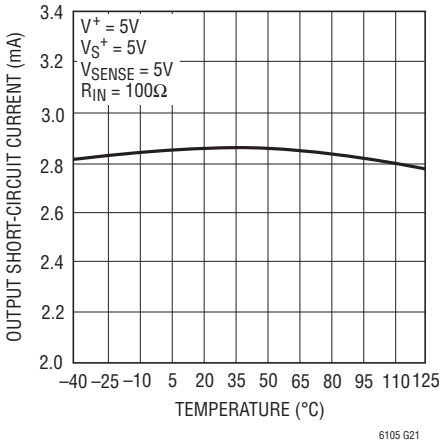
Output Saturation Voltage vs Output Current, V_S^+ = 12V



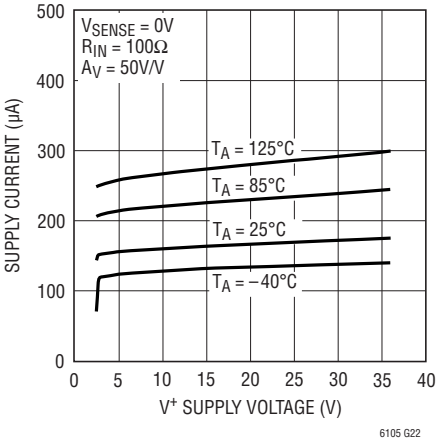
Output Saturation Voltage vs Output Current, V_S^+ = 0.5V



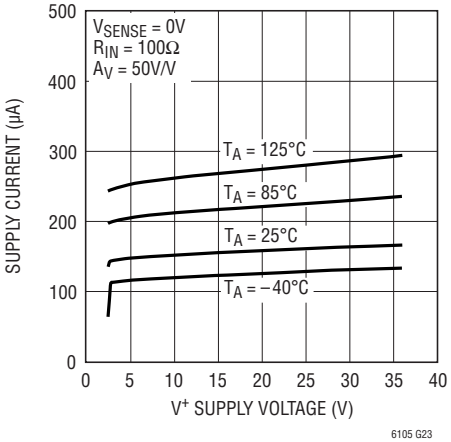
Output Short-Circuit Current vs Temperature



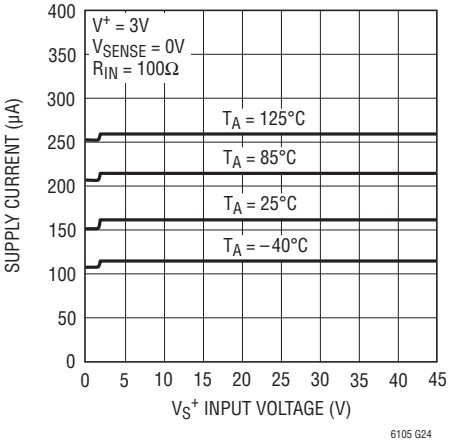
Supply Current vs Supply Voltage, V_S^+ = 12V



Supply Current vs Supply Voltage, V_S^+ = 0V

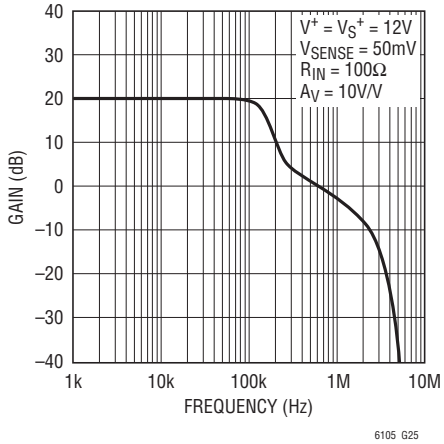


Supply Current vs Input Voltage

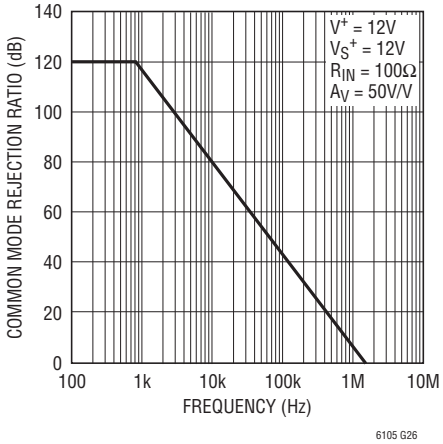


TYPICAL PERFORMANCE CHARACTERISTICS

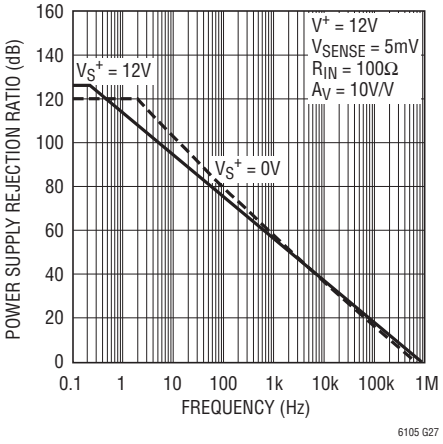
Gain vs Frequency



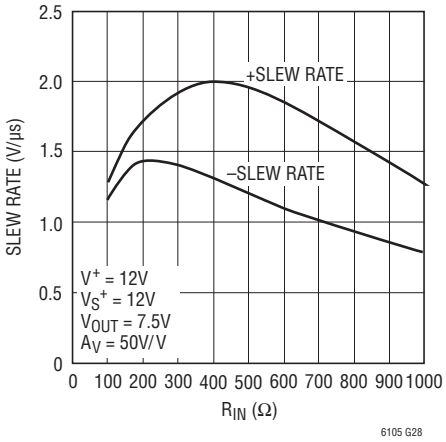
Common Mode Rejection Ratio vs Frequency



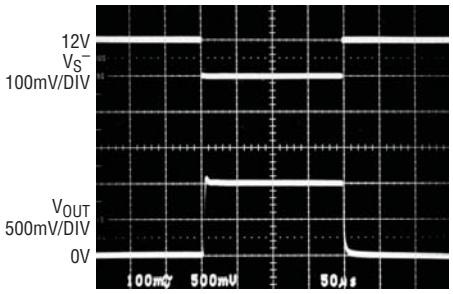
Power Supply Rejection Ratio vs Frequency



Slew Rate vs R_{IN}



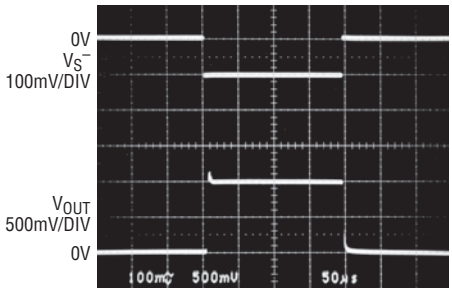
Step Response V_{SENSE} = 0V to 100mV, V_S^+ = 12V



50µs/DIV

V+ = 12V R_{OUT} = 10k
R_{IN} = 1k A_V = 10V/V

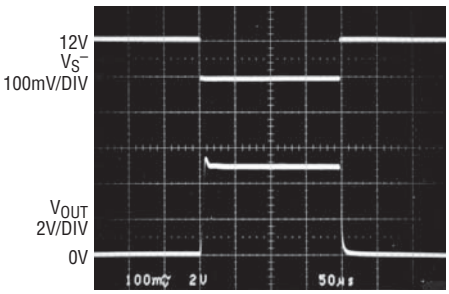
Step Response V_{SENSE} = 0V to 100mV, V_S^+ = 0V



50µs/DIV

V+ = 12V R_{OUT} = 10k
R_{IN} = 1k A_V = 10V/V

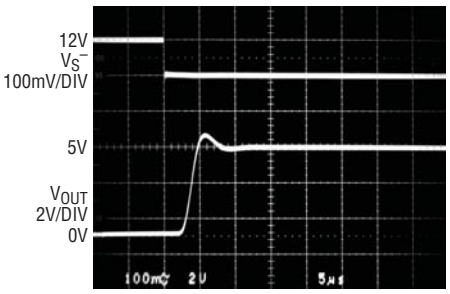
Step Response V_{SENSE} = 0V to 100mV, R_{IN} = 100Ω



50µs/DIV

V+ = 12V
VS+ = 12V
A_V = 50V/V

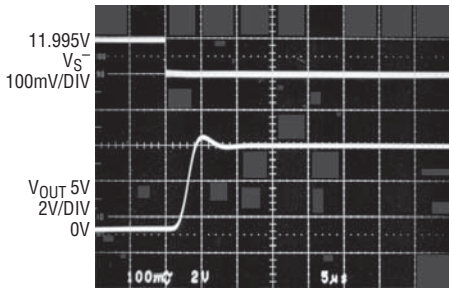
Step Response V_{SENSE} = 0V to 100mV



5µs/DIV

V+ = 12V R_{OUT} = 50k
VS+ = 12V A_V = 50V/V
R_{IN} = 1k

Step Response V_{SENSE} = 5mV to 100mV

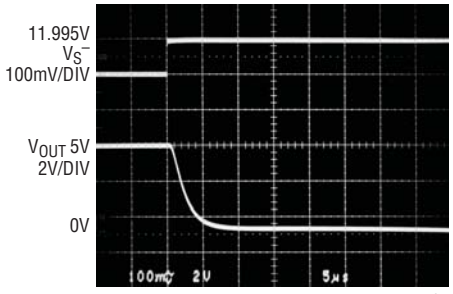


5µs/DIV

V+ = 12V R_{OUT} = 50k
VS+ = 12V A_V = 50V/V
R_{IN} = 1k

TYPICAL PERFORMANCE CHARACTERISTICS

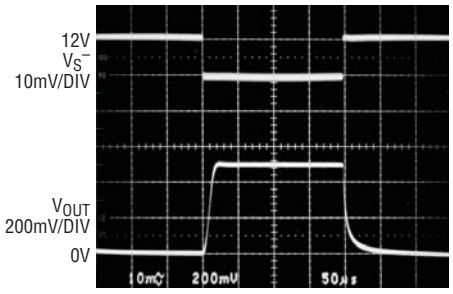
Step Response
V_{SENSE} = 100mV to 5mV



5µs/DIV

V^+ = 12V
V_S^+ = 12V
R_{IN} = 1k
R_{OUT} = 50k
A_V = 50V/V

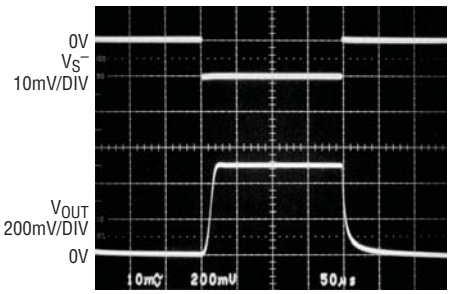
Step Response
V_{SENSE} = 0V to 10mV, V_S^+ = 12V



50µs/DIV

V^+ = 12V
R_{IN} = 100Ω
R_{OUT} = 5k
A_V = 50V/V

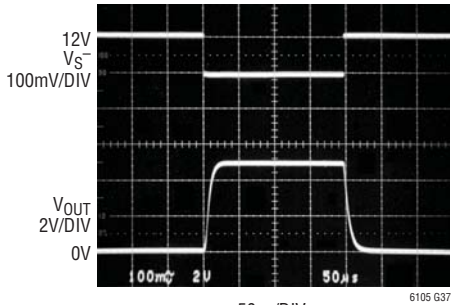
Step Response
V_{SENSE} = 0V to 10mV, V_S^+ = 0V



50µs/DIV

V^+ = 12V
R_{IN} = 100Ω
R_{OUT} = 5k
A_V = 50V/V

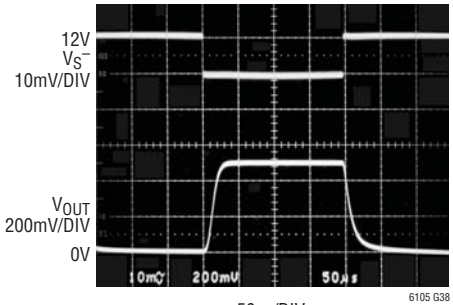
Step Response
V_{SENSE} = 0V to 100mV, C_L = 1000pF, V_S^+ = 12V



50µs/DIV

V^+ = 12V
R_{IN} = 100Ω
R_{OUT} = 5k
A_V = 50V/V
C_L = 1000pF

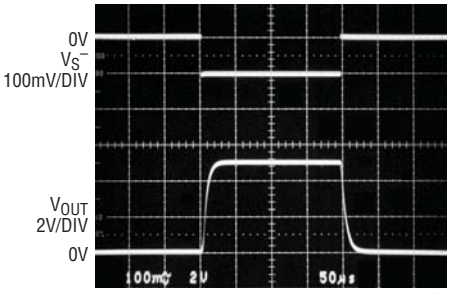
Step Response
V_{SENSE} = 0V to 10mV, C_L = 1000pF, V_S^+ = 12V



50µs/DIV

V^+ = 12V
R_{IN} = 100Ω
R_{OUT} = 5k
A_V = 50V/V
C_L = 1000pF

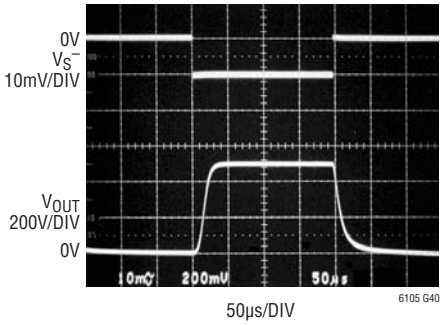
Step Response
V_{SENSE} = 0V to 100mV, C_L = 1000pF, V_S^+ = 0V



50µs/DIV

V^+ = 12V
R_{IN} = 100Ω
R_{OUT} = 5k
A_V = 50V/V
C_L = 1000pF

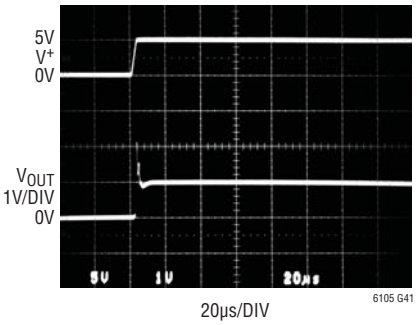
Step Response
V_{SENSE} = 0V to 10mV, C_L = 1000pF, V_S^+ = 0V



50µs/DIV

V^+ = 12V
R_{IN} = 100Ω
R_{OUT} = 5k
A_V = 50V/V
C_L = 1000pF

Power Supply Start-Up Response



20µs/DIV

V_S^+ = 12V
V_{SENSE} = 100mV
R_{IN} = 1k
A_V = 10V/V

PIN FUNCTIONS (DCB/MS8)

–IN (Pin 1/Pin 1): Negative Sense Input Terminal. Negative sense voltage input will remain functional for voltages up to 44V, referred to V^-. Connect –IN to an external gain-setting resistor R_{IN1} ($R_{IN1} = R_{IN2}$) to set the gain.

V^+ (Pin 2/Pin 2): Power Supply Voltage. This pin supplies current to the amplifier and can operate from 2.85V to 36V, independent of the voltages on the –IN or +IN pins.

V^- (Pin 3/Pin 4): Negative Power Supply Voltage or Ground for Single Supply Operation.

V_{OUT} (Pin 4/Pin 5): Voltage Output:

$$V_{OUT} = A_V \bullet (V_{SENSE} \pm V_{OS})$$

V_{OS} is the input offset voltage. A_V is the gain set by external R_{IN1}, R_{IN2}, R_{OUT}. $A_V = R_{OUT}/R_{IN1}$, for $R_{IN1} = R_{IN2}$.

NC (Pin 5/Pins 3, 6, 7): Not Connected Internally.

+IN (Pin 6/Pin 8): Positive Sense Input Terminal. Connecting a source to V_S^+ and a load to V_S^- will allow the LT6105 to monitor the current through R_{SENSE}, refer to Figure 1. Connect +IN to an external gain-setting resistor R_{IN2} to set the gain. +IN remains functional for voltages up to 44V, referred to V^-.

Exposed Pad (Pin 7) DFN Only: V^-. The Exposed Pad is connected to the V^- pin. It should be connected to the V^- trace of the PCB, or left floating.

BLOCK DIAGRAM

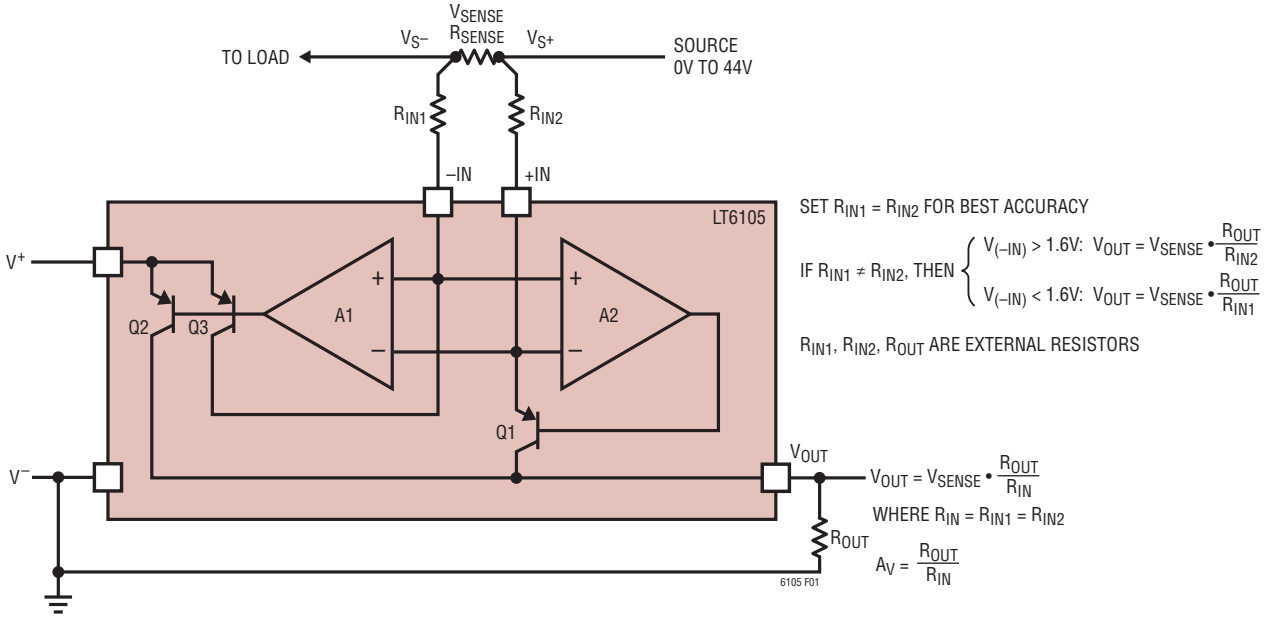


Figure 1. Simplified Block Diagram

APPLICATIONS INFORMATION

The LT6105 extended input range current sense amplifier (see Figure 1) provides accurate unidirectional monitoring of current through a user-selected sense resistor. The LT6105 is fully specified over a –0.3V to 44V input common mode range. A high PSRR V^+ supply (2.85V to 36V) powers the current sense amplifier. The input sense voltage is level shifted from the sensed power supply to the ground reference and amplified by a user-selected gain to the output. The output voltage is directly proportional to the current flowing through the sense resistor.

THEORY OF OPERATION (Refer to Figure 1)

Case 1: High Input Voltage (1.6V < V_{-IN} < 44V)

Current from the source at V_S^+ flows through R_{SENSE} to the load at V_S^-, creating a sense voltage, V_{SENSE}. Inputs V_S^+ and V_S^- apply the sense voltage to R_{IN2}. The opposite ends of resistors R_{IN1} and R_{IN2} are forced to be at equal potentials by the voltage gain of amplifier A2. Thus, the current through R_{IN2} is V_{SENSE}/R_{IN2}. The current through R_{IN2} is forced to flow through transistor Q1 and into R_{OUT}, creating an output voltage, V_{OUT}. Under this input operation range, amplifier A1 is kept off. The base current of Q1 has been compensated for and will not contribute to output error. The current from R_{IN2} flowing through resistor R_{OUT} gives an output voltage of $V_{OUT} = V_{SENSE} \bullet R_{OUT}/R_{IN2}$, producing a gain voltage of $A_V = V_{OUT}/V_{SENSE} = R_{OUT}/R_{IN2}$.

Case 2: Low Input Voltage (0V < V_{-IN} < 1.6V)

Current from the source at V_S^+ flows through R_{SENSE} to the load at V_S^-, creating a sense voltage, V_{SENSE}. Inputs V_S^+ and V_S^- apply the sense voltage to R_{IN1}. The opposite ends of resistors R_{IN1} and R_{IN2} are forced to be at equal potentials by the voltage gain of amplifier A1. Thus, the collector current of Q3 will flow out of the –IN pin through R_{IN1}. Q2 mirrors this current V_{SENSE}/R_{IN1} to R_{OUT}, creating an output voltage, V_{OUT}. Under this input operation range, amplifier A2 is kept off. This current V_{SENSE}/R_{IN1} flowing through resistor R_{OUT} gives an output voltage of $V_{OUT} = V_{SENSE} \bullet R_{OUT}/R_{IN1}$, producing a gain voltage of $A_V = V_{OUT}/V_{SENSE} = R_{OUT}/R_{IN1}$.

Selection of External Current Sense Resistor

External R_{SENSE} resistor selection is a delicate trade-off between power dissipation in the resistor and current measurement accuracy. For high current applications, the user may want to minimize the sense voltage to minimize the power dissipation in the sense resistor.

The system load current will cause both heat and voltage loss in R_{SENSE}. As a result, the sense resistor should be as small as possible while still providing the input dynamic range required by the measurement. Note that input dynamic range is the difference between the maximum input signal and the minimum accurately reproduced signal, and is limited primarily by input DC offset voltage of the internal amplifier of the LT6105.

The sense resistor value will be set from the minimum signal current that can be accurately resolved by this sense amp. As an example, the LT6105 has a typical input offset of 100µV. If the minimum current is 20mA, a sense resistor of 5mΩ will set V_{SENSE} to 100µV, which is the same value as the input offset. A larger sense resistor will reduce the error due to offset by increasing the sense voltage for a given load current, but it will limit the maximum peak current for a given application.

For a peak current of 2A and a maximum V_{SENSE} of 80mV, R_{SENSE} should not be more than 40mΩ. The input offset causes an error equivalent to only 2.5mA of load current. Peak dissipation is 160mW. If a 20mΩ sense resistor is employed, then the effective current error is 5mA, while the peak sense voltage is reduced to 40mV at 2A, dissipating only 80mW.

The LT6105's low input offset voltage of 100µV allows for high resolution while limiting the maximum sense voltages. Coupled with full scale sense voltage as large as 1V for R_{IN}= 1k, it can achieve 80dB of dynamic range.

Sense Resistor Connection

Kelvin connection of the LT6105's input resistors to the sense resistor should be implemented to provide the highest accuracy in high current applications. Solder connections and PC board interconnect resistance (approximately 0.5mΩ per square for 1oz copper) can be a large error in high current systems. A 5A application might choose

APPLICATIONS INFORMATION

a 20mΩ sense resistor to give a 100mV full-scale input to the LT6105. Input offset voltage will limit resolution to 5mA. Neglecting contact resistance at solder joints, even one square of PC board copper at each resistor end will cause an error of 5%. This error will grow proportionately higher as monitored current levels rise.

Gain Setting

The gain is set with three external resistors, R_{IN1}, R_{IN2}, R_{OUT}. The gain, R_{OUT}/R_{IN}, can be selected from 1V/V to 100V/V as long as the maximum current does not exceed 1mA. Select Gain = R_{OUT}/R_{IN2} for sense input voltage operation greater than 1.6V. Select gain = R_{OUT}/R_{IN1} for sense input voltage operation less than 1.6V. The overall system error will depend on the resistor tolerance chosen for the application. Set R_{IN1}= R_{IN2} for best accuracy across the entire input range. The total error will be gain error of the resistors plus the gain error of the LT6105 device.

Output Signal Range

The LT6105's output signal is developed by current through R_{IN2} (44V > V_{-IN} > 1.6V) or R_{IN1} (0V < V_{-IN} < 1.6V) conducted to the output resistor, R_{OUT}. This current is V_{SENSE}/R_{IN2} or V_{SENSE}/R_{IN1}. The sense amplifier's maximum output current before gain error begins to increase is 1mA. This allows low value output resistors to be used which helps preserve signal accuracy when the output pin is connected to other systems.

For zero V_{SENSE}, the internal circuitry gain will force V_{OUT} to $V_{O(MIN)}$ referred to V^-. Depending on output currents, V_{OUT} may swing positive to within $V_{O(MAX)}$ referred to V^+ or a maximum of 36V, a limit set by internal junction breakdown. Within these constraints, an amplified, level shifted representation of R_{SENSE} voltage is developed at V_{OUT}. The output is well behaved driving capacitive loads.

CM Input Signal Range

The LT6105 has high CMRR over the full input voltage range. The minimum operation voltage of the sense amplifier inputs is 0V whether V^+ is at 2.7V or 36V. The output remains accurate even when the sense inputs are driven to 44V. The graph in Figure 2 shows that V_{OS} changes very slightly over a wide input range. Furthermore, either sense inputs V_S^+ and V_S^- can collapse to 0V without incurring any damage to the device. The LT6105 can handle differential sense voltages up to 44V. For example, V_S^+ = 44V and V_S^- = 0V can be a valid condition in a current monitoring application (Figure 3) when an overload protection fuse is blown and V_S^- voltage collapses to ground. Under this condition, the output of the LT6105 goes to the positive rail, $V_{O(MAX)}$.

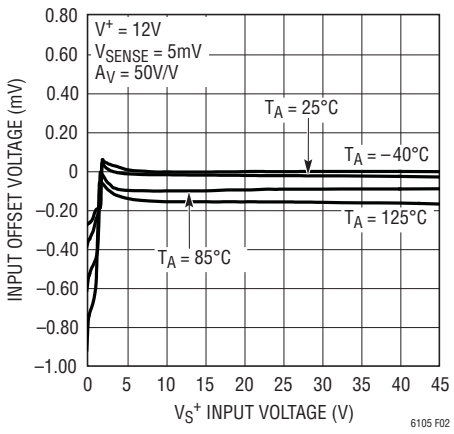


Figure 2. Input Offset Voltage vs V_S^+ Input Voltage

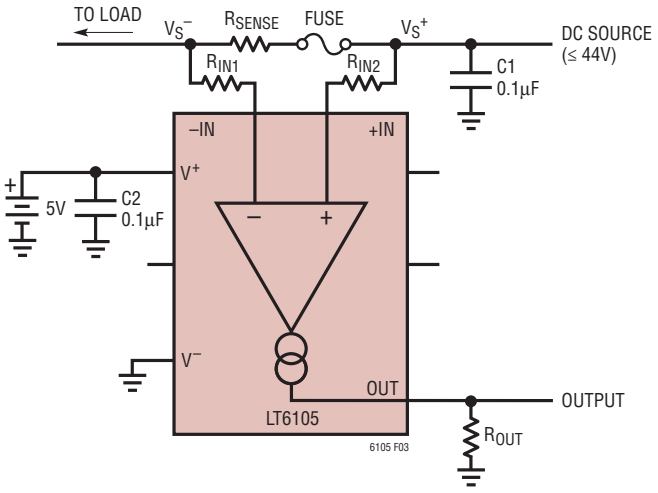


Figure 3. Current Monitoring of a Fuse Protected Circuit

APPLICATIONS INFORMATION

There is no phase inversion. For the opposite case, when V_S^+ collapses to ground with V_S^- held up at some higher voltage potential, the output will sit at $V_{O(MIN)}$.

The Two Input Stages Crossover Region

The wide common mode input range is achieved with two input stages. These two input stages consist of a pair of matched common base PNP input transistors and a pair of common emitter PNP input transistors. As result of two input stages, there will be three distinct operating regions around the transition region as shown in the Input Bias Current vs Sense Input Voltage curve in the Typical Performance Characteristics section.

The crossover voltage, the voltage where the g_m of one input stage is transferred to the other, occurs at 1.6V above V^-. Near this region, one input stage is shutting off while the other is turning on. Increases in temperature will cause the crossover voltage to decrease. For input operation between 1.6V and 44V, the common base PNPs are active (Q2, Q3 of Figure 1). The typical current through each input at V_{SENSE} = 0V is 15µA. The input offset voltage is 300µV maximum at room temperature. For input operation between 1.6V to 0V, the other PNP is active. The current out of the inputs at V_{SENSE} = 0V is 100nA. The input offset voltage is untrimmed and is typically 300µV.

Selection of External Output Resistor, R_{OUT}

The output resistor, R_{OUT}, determines how the output current is converted to voltage. V_{OUT} is simply $I_{RIN} \bullet R_{OUT}$.

In choosing an output resistor, the maximum output voltage must first be considered. If the following circuit is a buffer or ADC with limited input range, then R_{OUT} must be chosen so that $I_{OUT(MAX)} \bullet R_{OUT}$ is less than the allowed maximum input range of this circuit. In addition, the output impedance is determined by R_{OUT}.

If the circuit to be driven has high input impedance, then almost any useful output impedance will be acceptable. However, if the driven circuit has relatively low input impedance, or draws spikes of current such as an ADC might do, then a lower R_{OUT} value may be required in order to preserve the accuracy of the output. As an example, if the input impedance of the driven circuit is 100 times R_{OUT}, then the accuracy of V_{OUT} will be reduced by 1% since:

$$V_{OUT} = I_{OUT} \bullet \frac{R_{OUT} \bullet R_{IN(DRIVEN)}}{R_{OUT} + R_{IN(DRIVEN)}}$$

$$= I_{OUT} \bullet R_{OUT} \bullet \frac{100}{101} = 0.99 \bullet I_{OUT} \bullet R_{OUT}$$

Full-Scale Sense Voltage, Selection of External Input Resistor, R_{IN}

The external input resistor, R_{IN}, controls the transconductance of the current sense circuit. Since $I_{OUT} = V_{SENSE}/R_{IN}$, transconductance $g_m = 1/R_{IN}$. For example, if R_{IN} =100, then $I_{OUT} = V_{SENSE}/100$ or I_{OUT} = 1mA for V_{SENSE} =100mV. R_{IN} should be chosen to allow the required resolution while limiting the output current. The LT6105 can output more than 1mA into R_{OUT} without introducing a significant increase in gain error. By setting R_{IN} such that the largest expected sense voltage gives I_{OUT} = 1mA, then the maximum output dynamic range is available. Output dynamic range is limited by both the maximum allowed output current and the maximum allowed output voltage, as well as the minimum practical output signal. If less dynamic range is required, then R_{IN} can be increased accordingly, reducing the maximum output current and power dissipation. The LT6105's performance is optimized for values of R_{IN} = 100Ω to 1k. Values outside this range may result in additional errors. The power dissipation across R_{IN} and R_{OUT} should not exceed the resistors' recommended ratings.

APPLICATIONS INFORMATION

Error Sources

The current sense system uses an amplifier, current mirrors and external resistors to apply gain and level shifting. The output is then dependent on the matching characteristics of the current mirrors, characteristics of the amplifier such as gain and input offset, as well as matching of external resistors. Ideally, the circuit output is:

$$V_{OUT} = V_{SENSE} \bullet \frac{R_{OUT}}{R_{IN}}; V_{SENSE} = I_{SENSE} \bullet R_{SENSE}$$

In this case, the only error is due to resistor mismatch, which provides an error in gain only. Mismatch in the internal current mirror adds to gain error but is trimmed to less than 0.3%. Offset voltage and sense input current are the main cause of any additional error.

Error Due to Input Offset Voltage

Dynamic range is inversely proportional to the input offset voltage. Dynamic range can be thought of as the maximum V_{SENSE} divided by V_{OS}. The offset voltage of the LT6105 is typically only ±100µV.

Error Due to Sense Input Offset Current

Input offset current or mismatches in input bias current will introduce an additional input offset voltage term. Typical input offset current is 0.05µA. Lower values of R_{IN} will keep this error to a minimum. For example, if R_{IN} = 100Ω, then the additional offset is 5µV.

Output Current Limitations Due to Power Dissipation

The LT6105 can deliver up to 1mA continuous current to the output pin. This output current, I_{OUT}, is the mirrored current which flows through R_{IN2} and enters the current sense amp via the +IN pin for $V_{–IN}$ > 1.6V, and exits out of –IN through R_{IN1} for $V_{–IN}$ < 1.6V. The total power dissipation due to input currents, P_{IN}, and the dissipation due to internal mirrored currents, P_Q:

$$P_{TOTAL} = P_{IN} + P_Q$$

$$P_{IN} = (V_{+IN}) \bullet I_{RIN2};\ V_{–IN} > 1.6V$$

or

$$P_{IN} = (V^+ – (V_{–IN})) \bullet I_{RIN1};\ V_{–IN} < 1.6V$$

Since the current exiting –IN is coming from V^+, the voltage is $V^+ – V_{–IN}$. Taking the worst case $V_{–IN}$ = 0V, the above equation becomes:

$$P_{IN} \cong V^+ \bullet I_{RIN1},\ \text{for } V_{–IN} < 1.6V.$$

The power dissipated due to internal mirrored currents:

$$P_Q = 2 \bullet I_{OUT} \bullet V^+$$

The factor of 2 is the result of internal current shifting and 1:1 mirroring.

At maximum supply and maximum output current, the total power dissipation can exceed 100mW. This will cause significant heating of the LT6105 die. In order to prevent damage to the LT6105, the maximum expected dissipation in each application should be calculated. This number can be multiplied by the θ_{JA} value listed in the Pin Configuration section to find the maximum expected die temperature. This must not be allowed to exceed 150°C, or performance may be degraded. As an example, if an LT6105 in the MSOP package is to be run at V_S^+ = 44V and V^+ = 36V with 1mA output current at 80°C ambient:

$$P_{Q(MAX)} = 2 \bullet I_{OUT(MAX)} \bullet V^+ = P_{Q(MAX)} = 72mW$$

$$P_{IN(MAX)} = I_{RIN2(MAX)} \bullet V_{+IN(MAX)} = 44mW$$

$$T_{RISE} = \theta_{JA} \bullet P_{TOTAL(MAX)}$$

$$T_{MAX} = T_{AMBIENT} + T_{RISE}$$

T_{MAX} must be < 150°C

$P_{TOTAL(MAX)}$ = 116mW and the maximum die temperature will be 109°C. If this same circuit must run at 125°C ambient, the maximum die temperature will increase to 150°C. Note that supply current, and therefore P_Q, is proportional to temperature. Refer to the Typical Performance Characteristics section. In this condition, the maximum output current should be reduced to avoid device damage. The DCB package, on the other hand, has a lower θ_{JA} and subsequently, a lower die temperature increase than the MSOP. With the same condition as above, the DCB will rise only 7.5°C to 87.5°C and 132.5°C, respectively.

It is important to note that the LT6105 has been designed to provide at least 1mA to the output when required, and can deliver more under large V_{SENSE} conditions. Care must be taken to limit the maximum output current by proper choice of sense resistor and input resistors.

APPLICATIONS INFORMATION

Output Filtering

The output voltage, V_{OUT} is simply $I_{OUT} \bullet Z_{OUT}$. This makes filtering straightforward. Any circuit may be used which generates the required Z_{OUT} to get the desired filter response. For example, a capacitor in parallel with R_{OUT} will give a low pass response. This will reduce unwanted noise from the output, and may also be useful as a charge reservoir to keep the output steady while driving a switching circuit such as a mux or an ADC. This output capacitor in parallel with an output resistor will create a pole in the output response at:

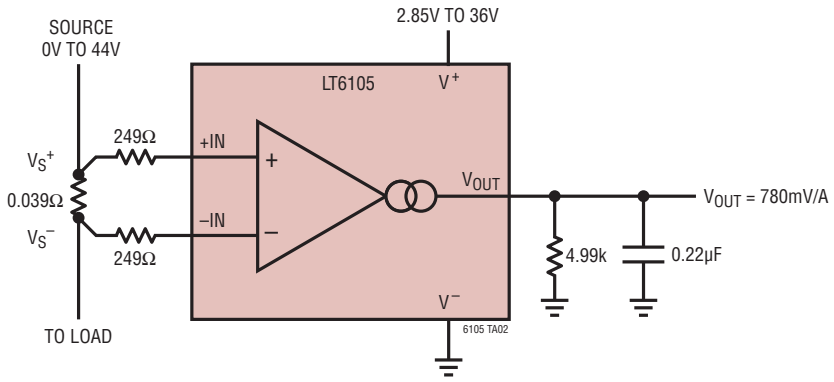
$$f_{-3db} = \frac{1}{2 \bullet \pi \bullet R_{OUT} \bullet C_{OUT}}$$

Response Time

The LT6105 is designed to exhibit fast response to inputs for the purpose of circuit protection or signal transmission. This response time will be affected by the external circuit in two ways—delay and speed. If the output current is very low and an input transient occurs, there may be an increased delay before the output voltage begins changing. This can be improved by increasing the minimum output current, either by increasing R_{SENSE} or decreasing R_{IN}. The effect of increased output current is illustrated in the step response curves in the Typical Performance Characteristics section of this data sheet. Note that the curves are labeled with respect to the initial output currents. The speed is also affected by the external circuit. In this case, if the input changes very quickly, the internal amplifier will slew the base of the internal output PNP (Figure 1) in order to maintain the internal loop. This results in current flowing through R_{IN} and the internal PNP. This current slew rate will be determined by the amplifier and PNP characteristics as well as the input resistor, R_{IN}. See the Slew Rate vs R_{IN} curve in the Typical Performance Characteristics section. Using a smaller R_{IN} will allow the output current to increase more quickly, decreasing the response time at the output. This will also have the effect of increasing the maximum output current.

TYPICAL APPLICATIONS

Gain of 20 Current Sense Amplifier with Output Filtering



TYPICAL APPLICATIONS

Solenoid Monitor

The large input common mode range of the LT6105 makes it suitable for monitoring currents in quarter, half and full bridge inductive load driving applications. Figure 4 shows an example of a quarter bridge. The MOSFET pulls down on the bottom of the solenoid to increase solenoid current. It lets go to decrease current, and the solenoid voltage freewheels around the Schottky diode. Current measurement waveforms are shown in Figure 5. The small glitches occur due to the action of the solenoid plunger, and this provides an opportunity for mechanical system monitoring without an independent sensor or limit switch.

Figure 6 shows another solenoid driver circuit, this time with one end of the solenoid grounded and a P-channel MOSFET pulling up on the other end. In this case, the inductor freewheels around ground, imposing a negative input common mode voltage of one Schottky diode drop. This voltage may exceed the input range of the LT6105. This does not endanger the device, but it severely degrades its accuracy. In order to avoid violating the input range, pull-up resistors may be used as shown.

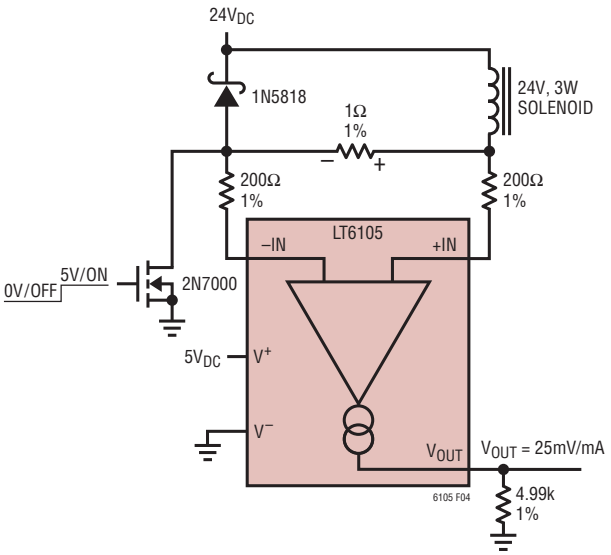


Figure 4. Simplest Form of a Solenoid Driver. The LT6105 Monitors the Current in Both On and Freewheel States. The Lowest Common Mode Voltage Is 0V, While the Highest Is 24V Plus the Forward Voltage of the Schottky Diode

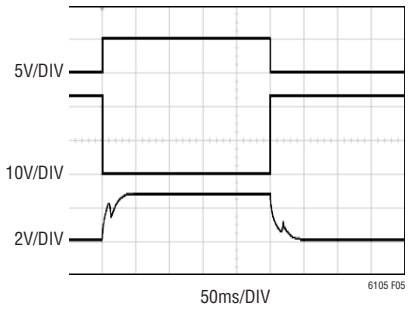


Figure 5. Current Measurement Waveforms. The Top Trace Is the MOSFET Gate with High On. The Middle Trace Is the Bottom of the Solenoid/Inductor. The Bottom Trace Is the LT6105 Output, Representing Solenoid Current at 80mA/DIV. Glitches Are Useful Indicators of Solenoid Plunger Movement

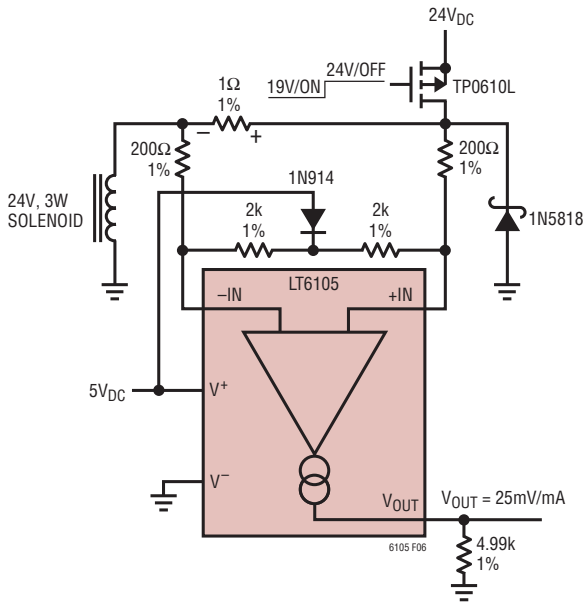
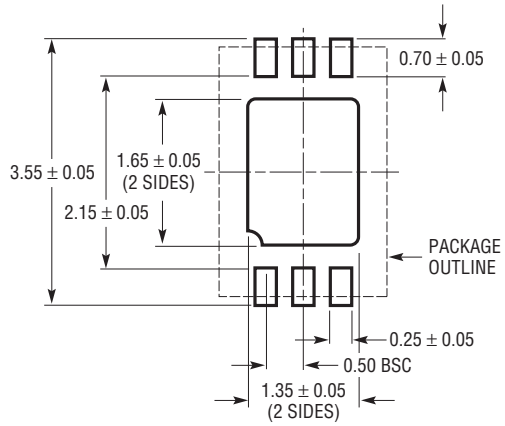


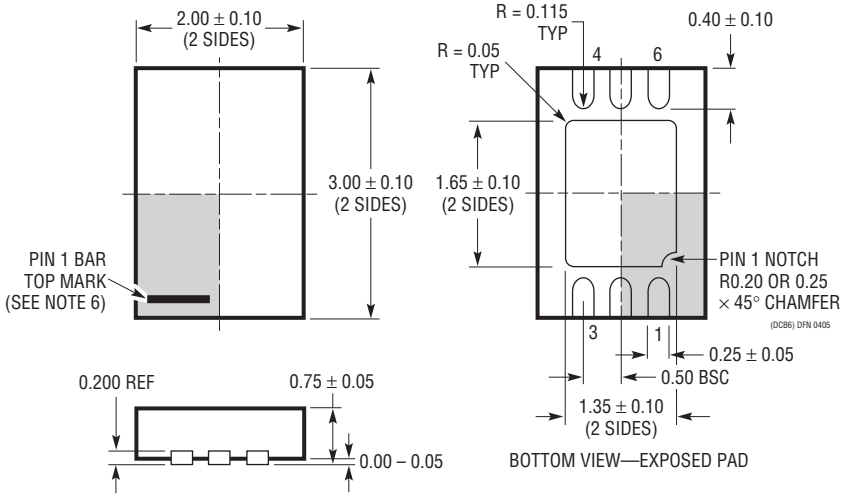
Figure 6. A Similar Circuit to Figure 4, but with Solenoid Grounded, so Freewheeling Forces Inputs Negative. Providing Resistive Pull-Ups Keeps Amplifier Inputs From Falling Outside of Their Accurate Input Range

PACKAGE DESCRIPTION

DCB Package
6-Lead Plastic DFN (2mm × 3mm)
(Reference LTC DWG # 05-08-1715)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

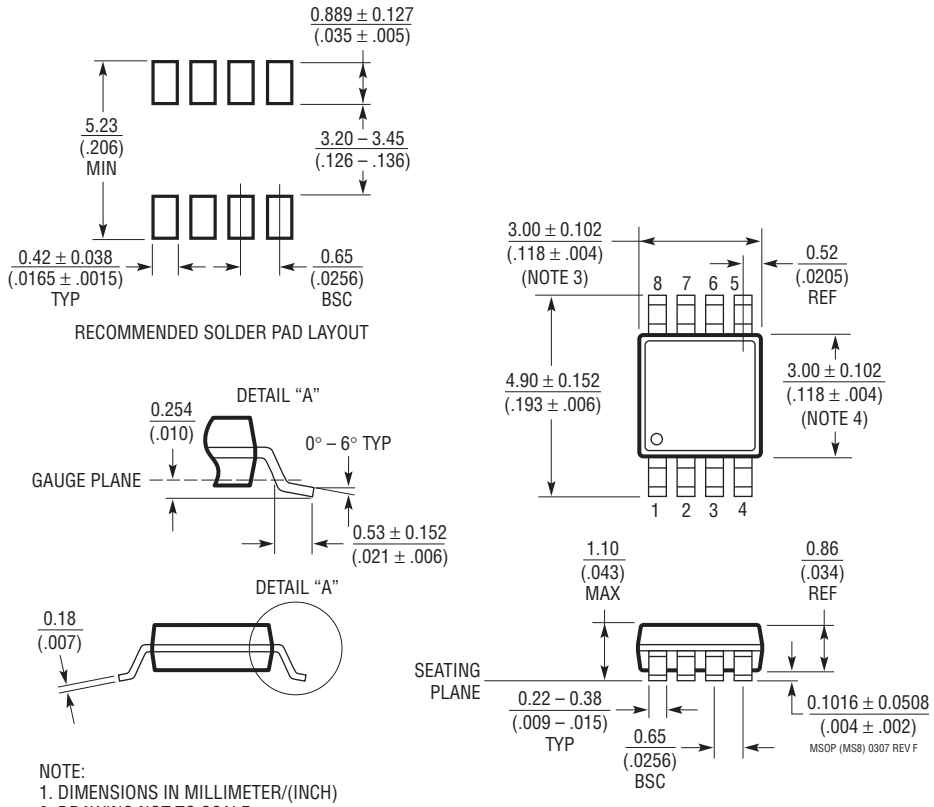


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (TBD)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

Supply Monitoring

The input common mode range of the LT6105 also makes it suitable for monitoring either positive or negative supplies. Figure 7 shows one LT6105 applied as a simple positive supply monitor, and another LT6105 as a simple negative supply monitor. Note that the schematics are practically identical and both have outputs conveniently referred to ground. The only requirement for negative supply monitoring, in addition to the usual constraints of the absolute maximum ratings, is that the negative supply to that LT6105 be at least as negative as the supply it is monitoring.

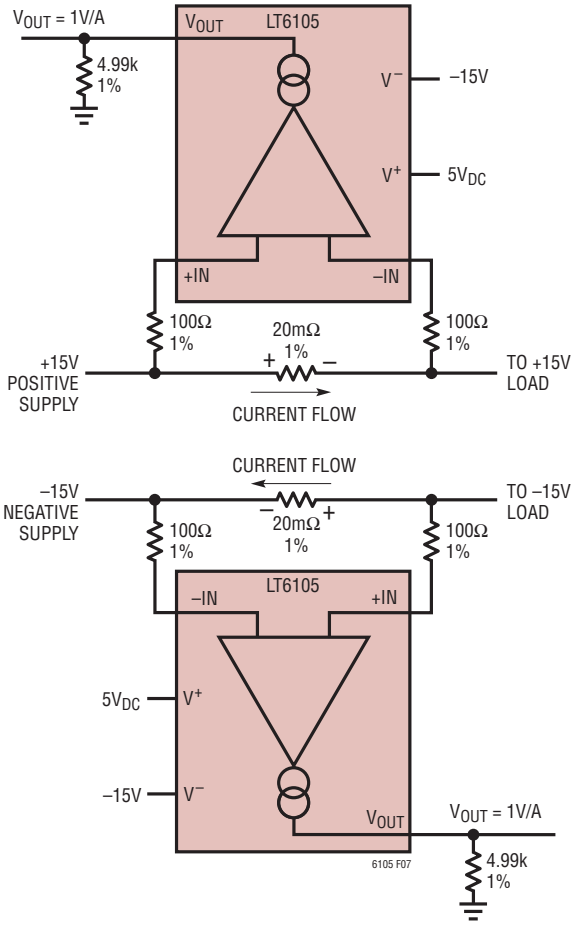


Figure 7. The LT6105 Can Monitor the Current of Either Positive or Negative Supplies, Without a Schematic Change. Just Ensure That the Current Flow Is in the Correct Direction

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1787/LT1787HV	Precision, Bidirectional, High Side Current Sense Amplifier	2.7V to 60V Operation, 75µV Offset, 60µA Current Draw
LTC4150	Coulomb Counter/Battery Gas Gauge	Indicates Charge Quantity and Polarity
LT6100	Gain-Selectable High Side Current Sense Amplifier	4.1V to 48V Operation, Pin-Selectable Gain: 10V/V, 12.5V/V, 20V/V, 25V/V, 40V/V, 50V/V
LTC6101/ LTC6101HV	High Voltage High Side Current Sense Amplifier	4V to 60V/5V to 100V Operation, External Resistor Set Gain, SOT23
LTC6102/ LTC6102HV	Zero Drift High Side Current Sense Amplifier	4V to 60V/5V to 100V Operation, ±10µV Offset, 1µs Step Response, MSOP8 / DFN
LTC6103	Dual High Side Precision Current Sense Amplifier	4V to 60V, Gain Configurable, 8-Pin MSOP
LTC6104	Bidirectional High Side Precision Current Sense Amplifier	4V to 60V, Gain Configurable, 8-Pin MSOP
LT6106	Low Cost, High Side Precision Current Sense Amplifier	2.7V to 36V, Gain Configurable, SOT23

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