LB11696V

ON Semiconductor®

Monolithic Digital IC

Brushless Motor Driver Application Note

Direct PWM Drive, Quiet Pre-driver IC

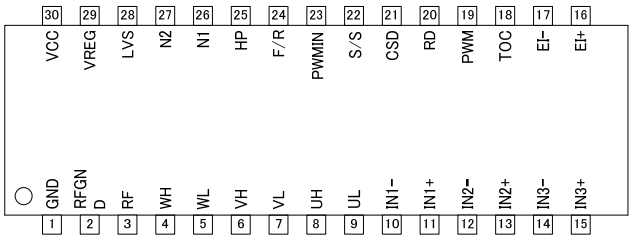
Overview

The LB11696V is a direct PWM drive pre-driver IC designed for three-phase power brushless motors. A motor driver circuit with the desired output power (voltage and current) can be implemented by adding discrete transistors in the output circuits. Furthermore, the LB11696V provides a full complement of protection circuits allowing it to easily implement high-reliability drive circuits. This device is optimal for driving all types of large-scale motors such as those used in air conditioners and on-demand water heaters.

Function

- Three-phase bipolar drive
- Direct PWM drive (controlled either by control voltage or PWM variable duty pulse input)
- Built-in forward/reverse switching circuit
- Start/stop mode switching circuit (stop mode power saving function)
- Built-in input amplifier
- 5V regulator output (VERG pin)
- Current limiter circuit (Supports 0.25V (typical) reference voltage sensing based high-precision detection)
- Under voltage protection circuit (The operating voltage can be set with a zener diode)
- Automatic recovery type constraint protection circuit with protection operating state discrimination output (RD pin)
- Four types of Hall signal pulse output
- Supports thermistor based thermal protection of the output transistors

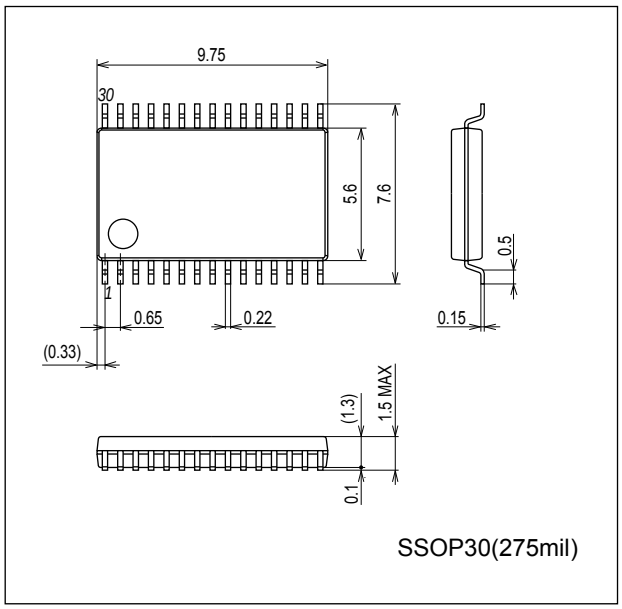
Pin Assignment



Top View

Package Dimensions

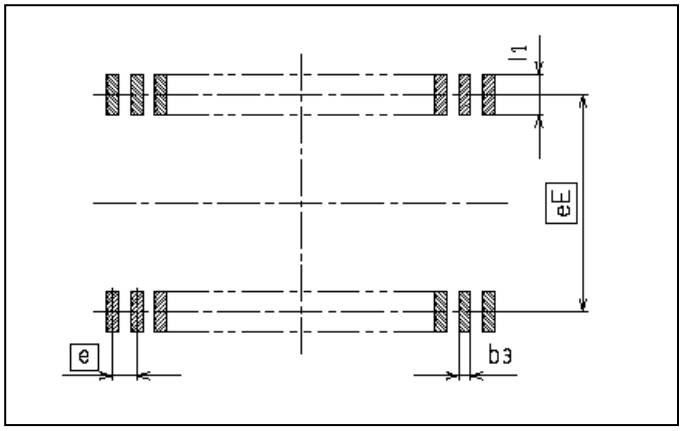
unit : mm (typ)
3191C



SSOP30(275mil)

Caution: The package dimension is a reference value, which is not a guaranteed value

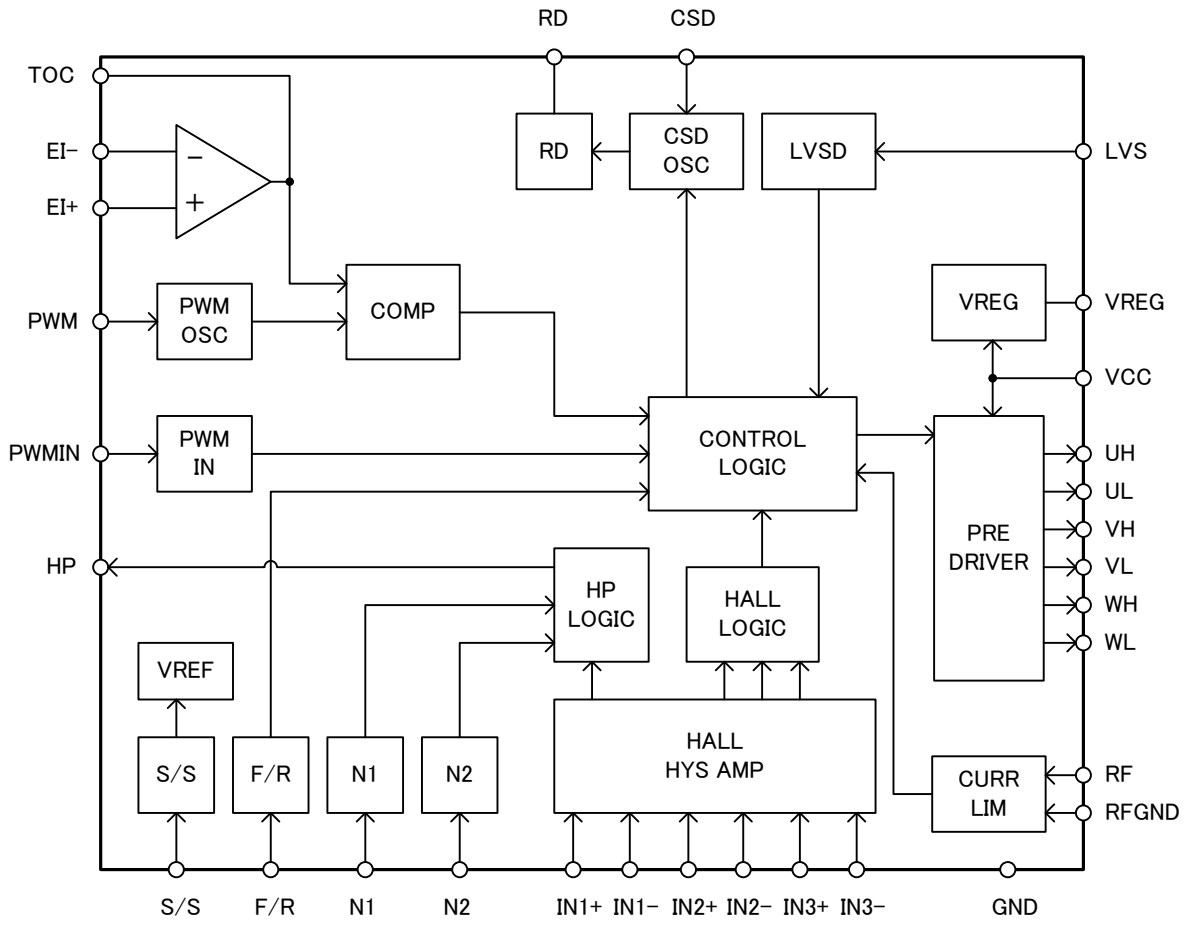
Recommended Soldering Footprint



(Unit:mm)

Reference symbol	SSOP30(275mil)
eE	7.00
e	0.65
b3	0.32
l1	1.00

Block Diagram



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max	V_{CC} pin	18	V
Output current	I_O max	UL, VL, WL, UH, VH, WH pins	30	mA
LVS pin applied voltage	LVS max	LVS pin	18	V
Allowable power dissipation	Pd max1	Independent IC	0.45	W
	Pd max2	Mounted on a specified circuit board.*	1.05	W
Operating temperature	Topr		-20 to +100	°C
Storage temperature	Tstg		-55 to +150	°C

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.
Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage range 1-1	V_{CC1-1}	Vcc pin	8		17	V
Supply voltage range1-2	V_{CC1-2}	Vcc pin, when Vcc is shorted to VREG.	4.5		5.5	V
Output current	I_O	UL, VL, WL, UH, VH, and WH pins		25		mA
5V constant voltage output current	I_{REG}			-30		mA
HP pin applied voltage	V_{HP}		0		17	V
HP pin applied current	I_{HP}		0		15	mA
RD pin applied voltage	V_{RD}		0		17	V
RD pin applied current	I_{RD}		0		15	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = 15V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain 1	$I_{CC}1$			12	16	mA
Current drain 2	$I_{CC}2$	Stop mode		2.5	4	mA
5V Constant Voltage Output (VREG pin)						
Output voltage	VREG		4.7	5.0	5.3	V
Line regulation	ΔVREG1	V_{CC} = 8 to 17V		40	100	mV
Load regulation	ΔVREG2	I_O = -5 to -20mA		10	30	mV
Temperature coefficient	ΔVREG3	Design target value		0		mV/□
Output Block						
Output voltage 1-1	V_{OUT1-1}	Low level, I_O = 400μA		0.2	0.5	V
Output voltage 1-2	V_{OUT1-2}	Low level, I_O = 10mA		0.9	1.2	V
Output voltage 2	V_{OUT2}	High level, I_O = -20mA	Vcc-1.1	Vcc-0.9		V
Output leakage current	$I_O$leak				10	μA
Hall Amplifier Block						
Input bias current	IHB (HA)		-2	-0.5		μA
Common-mode input voltage range 1	VICM1	When a Hall element device is used	0.5		Vcc-2.0	V
Common-mode input voltage range 2	VICM2	Single-sided input bias mode (when a Hall IC is used)	0		Vcc	V
Hall input sensitivity	VHIN	Sine wave, Hall element offset = 0V	80			mVp-p
Hysteresis	ΔV_{IN} (HA)		15	24	40	mV
Input voltage Low → High	VSLH(HA)		5	12	20	mV
Input voltage High → Low	VSHL(HA)		-20	-12	-5	mV

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
CTL Amplifier						
Input offset voltage	V_{IO} (CTL)		-10		10	mV
Input bias current	I_B (CTL)		-1		1	μA
Common-mode input voltage range	V_{ICM}		0		VREG-1.7	V
High-level output voltage	V_{OH} (CTL)	ITOC = -0.2mA	VREG-1.2	VREG-0.8		V
Low-level output voltage	V_{OL} (CTL)	ITOC = 0.2mA		0.8	1.05	V
Open-loop gain	G (CTL)	f(CTL) = 1kHz	45	51		dB
PWM Oscillator (PWM pin)						
High level output voltage	V_{OH} (PWM)		2.75	3.0	3.25	V
Low level output voltage	V_{OL} (PWM)		1.2	1.35	1.5	V
External frequency	ICHG	CVPWM = 2.1V	-120	-90	-65	kHz
Oscillation frequency	f (PWM)	C = 2000pF		22		kHz
Amplitude	V (PWM)		1.4	1.6	1.9	Vp-p
TOC pin						
Input voltage 1	VTOC1	Output duty : 100%	2.75	3.0	3.25	V
Input voltage 2	VTOC2	Output duty : 0%	1.2	1.35	1.5	V
Input voltage 1 low	VTOC1L	Design target value, when VREG = 4.7V, 100%	2.68	2.82	2.96	V
Input voltage 2 low	VTOC2L	Design target value, when VREG = 4.7V, 0%	1.23	1.29	1.34	V
Input voltage 1 high	VTOC1H	Design target value, when VREG = 5.3V, 100%	3.02	3.18	3.34	V
Input voltage 2 high	VTOC2H	Design target value, when VREG = 5.3V, 0%	1.37	1.44	1.50	V
HP Pin						
Output saturation voltage	VHPL	I_O = 10mA		0.2	0.5	V
Output leakage current	IHPleak	V_O = 18V			10	μA
CSD Oscillator Circuit (CSD pin)						
High level output voltage	V_{OH} (CSD)		2.7	3.0	3.3	V
Low level output voltage	V_{OL} (CSD)		0.7	1.0	1.3	V
External capacitor charging current	ICHG1	VCSD = 2.0V	-3.15	-2.5	-1.85	μA
External capacitor discharging current	ICHG2	VCSD = 2.0V	0.1	0.14	0.18	μA
Charge/discharge current ratio	RCSD	(Charge current)/(discharge current)	15	18	21	times
RD Pin						
Low-level output voltage	VRDL	I_O = 10mA		0.2	0.5	V
Output leakage current	I_L(RD)	V_O = 18V			10	μA
Current Limiter Circuit (RF pin)						
Limiter voltage	VRF		0.225	0.25	0.275	V
Under-voltage Protection Circuit (LVS pin)						
Operation voltage	VSDL		3.5	3.7	3.9	V
Release voltage	VSDH		3.95	4.15	4.35	V
Hysteresis	ΔVSD		0.3	0.45	0.6	V
PWMIN pin						
Input frequency	f (PI)				50	kHz
High-level input voltage	V_{IH} (PI)		2.0		VREG	V
Low-level input voltage	V_{IL} (PI)		0		1.0	V
Input open voltage	V_{IO} (PI)		VREG-0.5		VREG	V
Hysteresis	V_{IS} (PI)		0.2	0.25	0.4	V
High-level input current	I_{IH} (PI)	VPWMIN = VREG	-10	0	+10	μA
Low-level input current	I_{IL} (PI)	VPWMIN = 0V	-130	-90		μA

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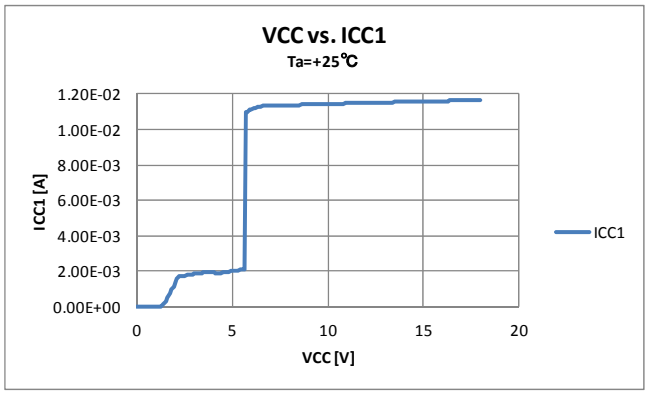
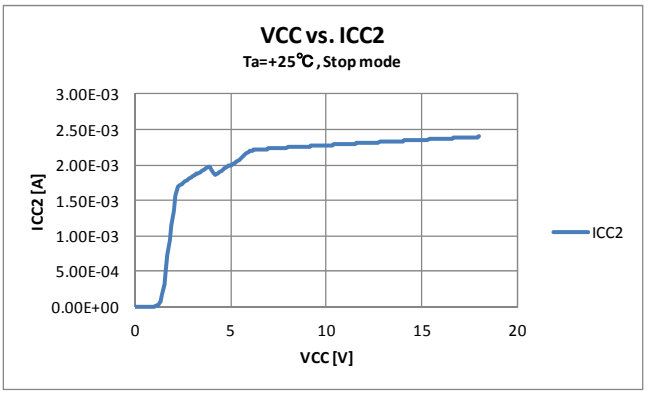
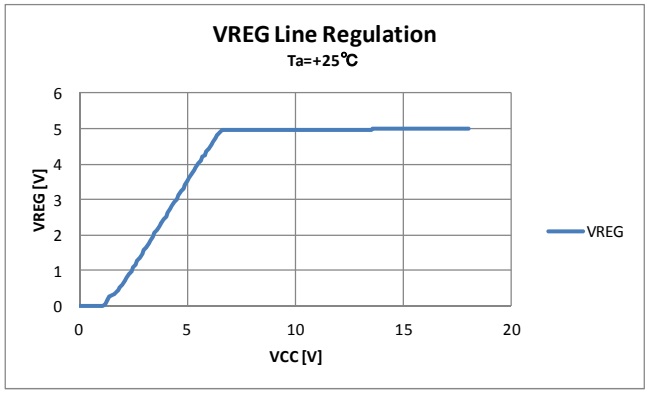
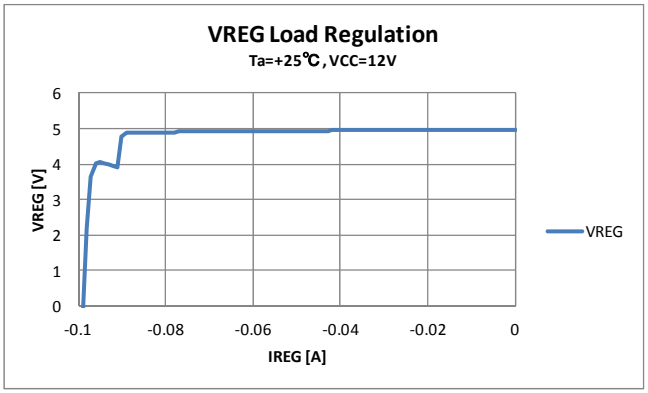
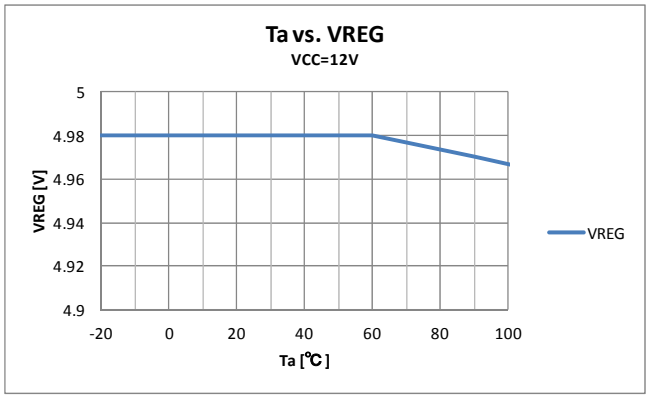
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
S/S pin						
High-level input voltage	VIH (SS)		2.0		VREG	V
Low-level input voltage	VIL (SS)		0		1.0	V
Hysteresis	V_{IS} (SS)		0.2	0.25	0.4	V
High-level input current	IIH (SS)	VS/S = VREG	-10	0	+10	μA
Low-level input current	IIL (SS)	VS/S = 0V	-10	-1		μA
F/R Pin						
High level input voltage	V_{IH} (FR)		2.0		VREG	V
Low level input voltage	V_{IL} (FR)		0		1.0	V
Input open voltage	V_{IO} (FR)		VREG-0.5		VREG	V
Hysteresis	V_{IS} (FR)		0.2	0.25	0.4	V
High-level input current	I_{IH} (FR)	VF/R = VREG	-10	0	+10	μA
Low-level input current	I_{IL} (FR)	VF/R = 0V	-130	-90		μA
N1 Pin						
High level input voltage	V_{IH} (N1)		2.0		VREG	V
Low level input voltage	V_{IL} (N1)		0		1.0	V
Input open voltage	V_{IO} (N1)		VREG-0.5		VREG	V
High-level input current	I_{IH} (N1)	VN1 = VREG	-10	0	+10	μA
Low-level input current	I_{IL} (N1)	VN1 = 0V	-130	-100		μA
N2 Pin						
High level input voltage	V_{IH} (N2)		2.0		VREG	V
Low level input voltage	V_{IL} (N2)		0		1.0	V
Input open voltage	V_{IO} (N2)		VREG-0.5		VREG	V
High-level input current	I_{IH} (N2)	VN2 = VREG	-10	0	+10	μA
Low-level input current	I_{IL} (N2)	VN2 = 0V	-130	-100		μA

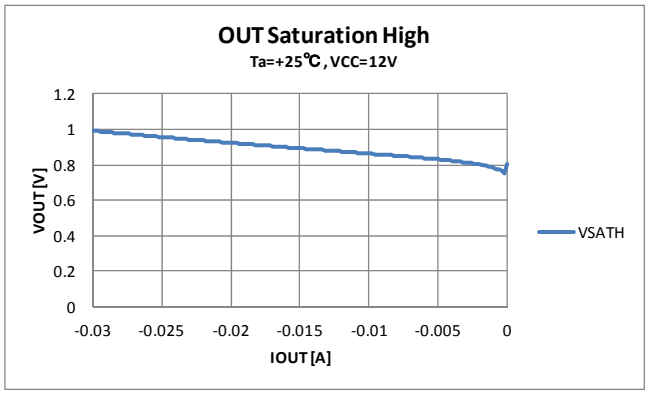


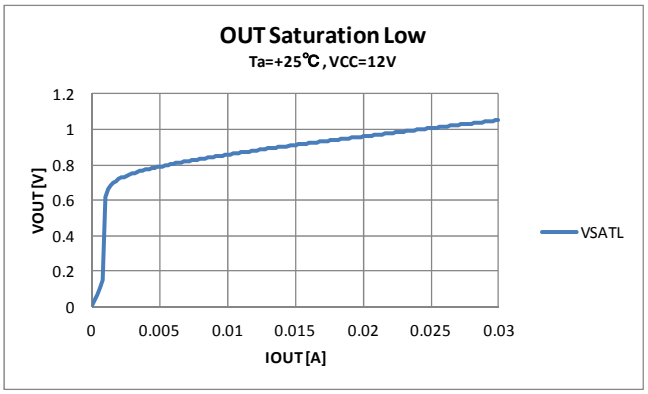


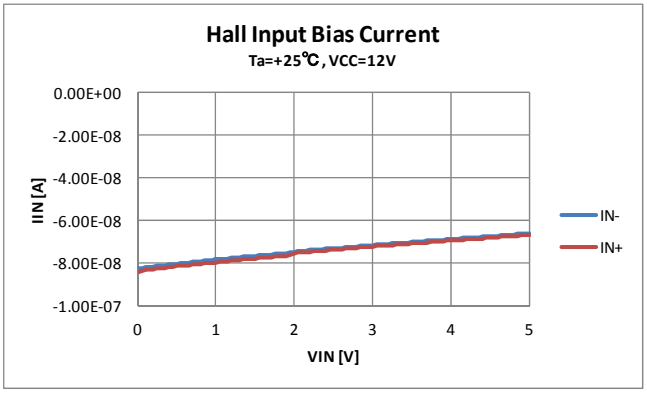


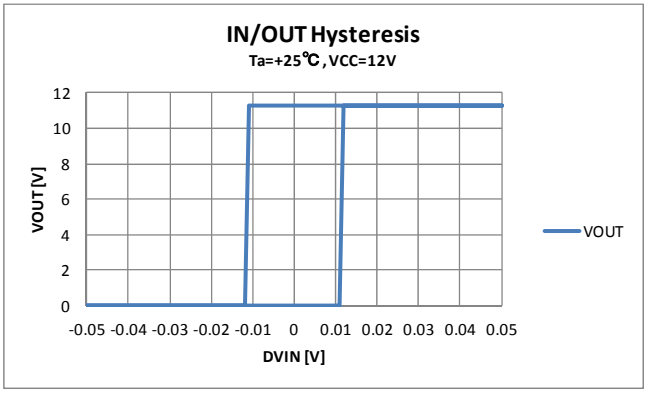


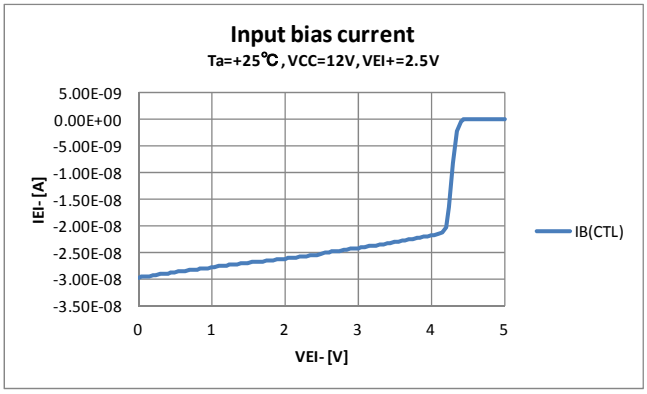


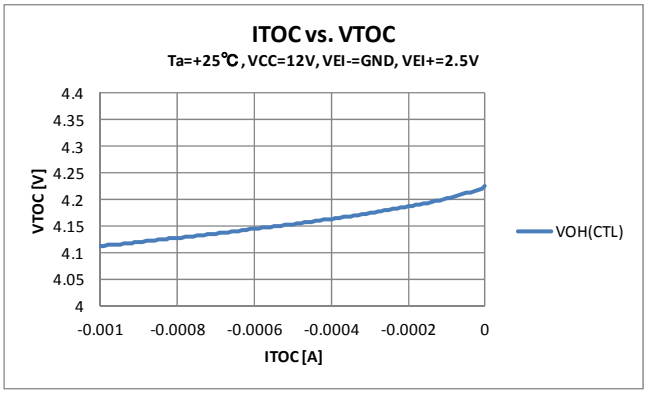


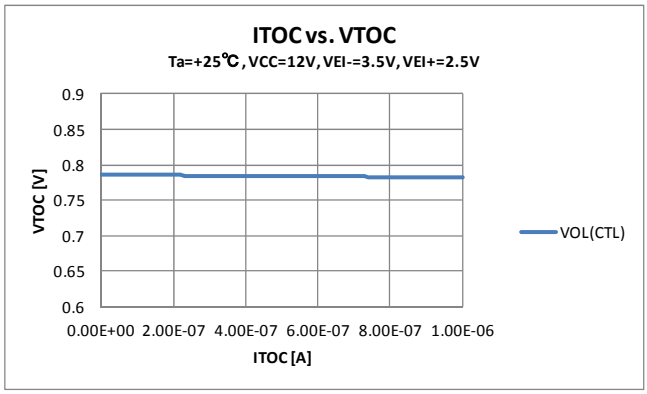


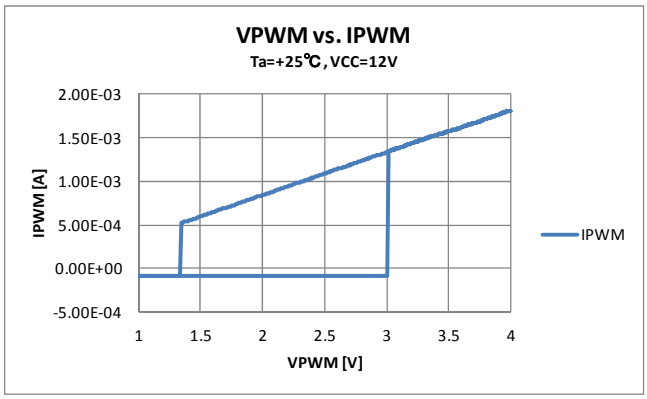


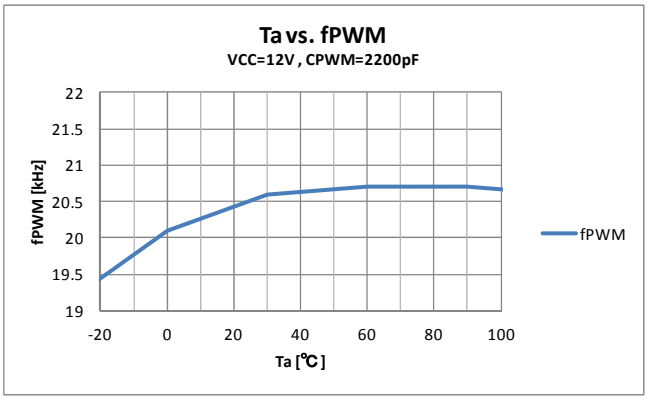


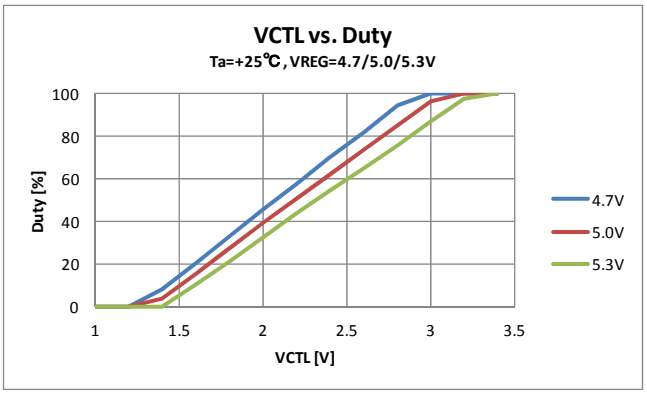


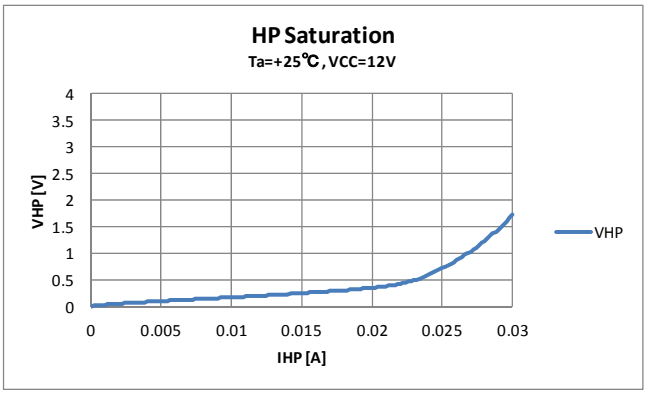


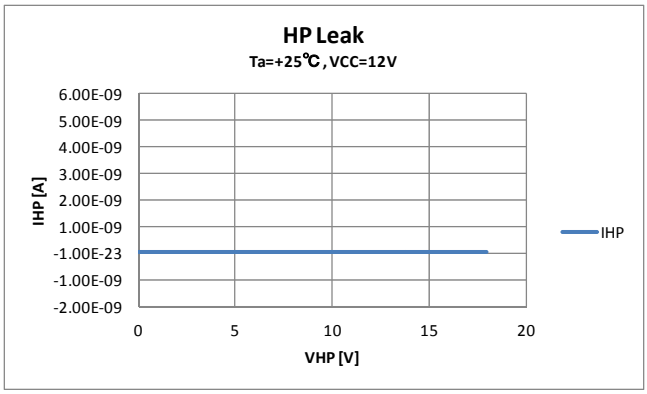


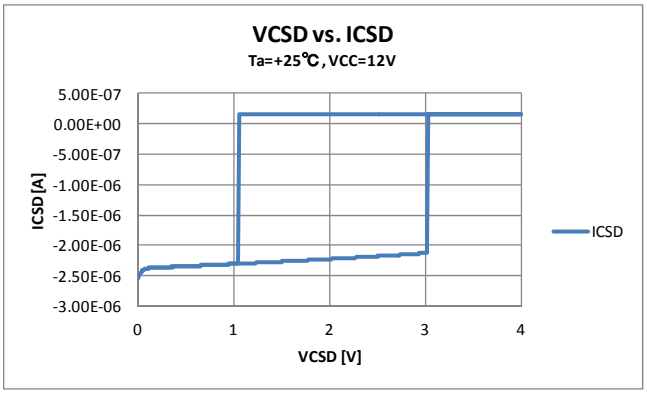


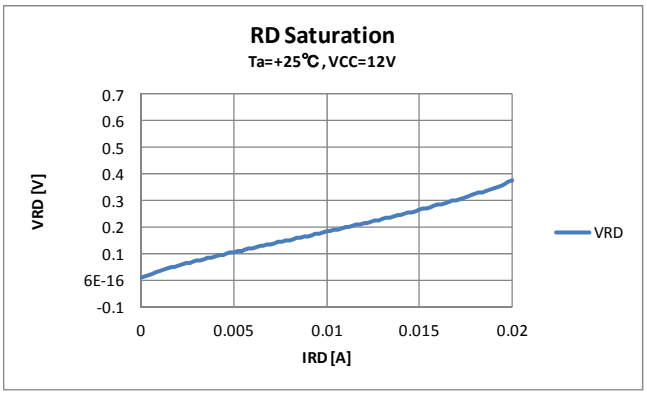


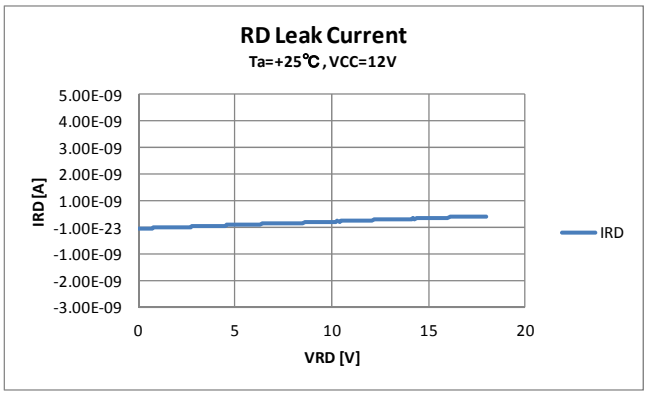


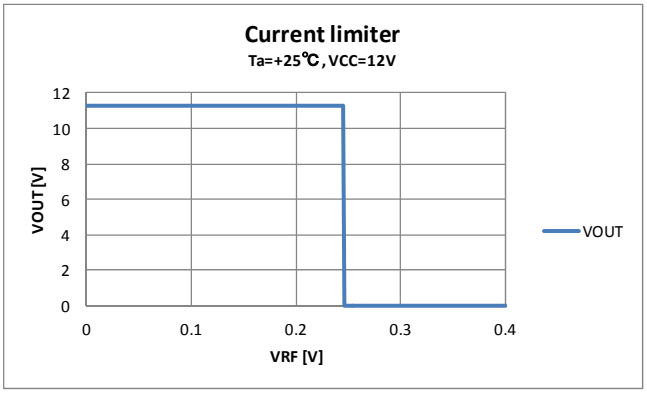


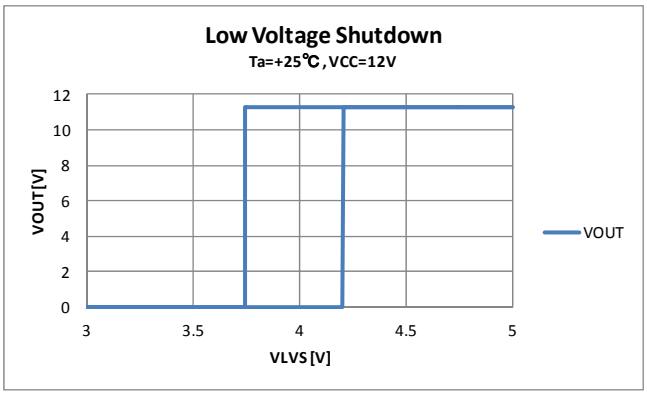


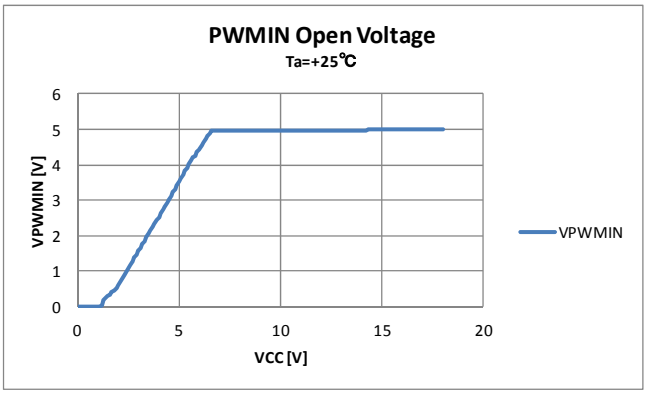


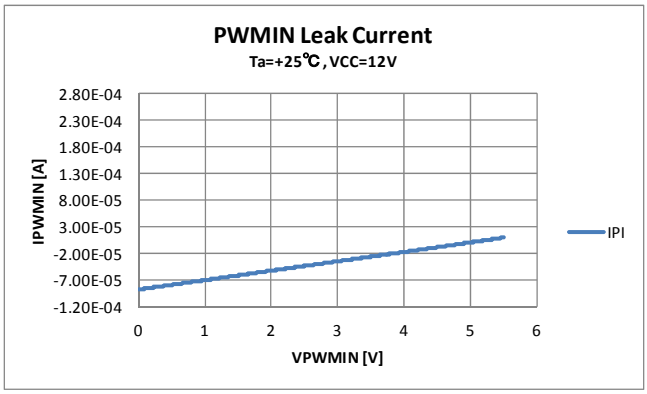


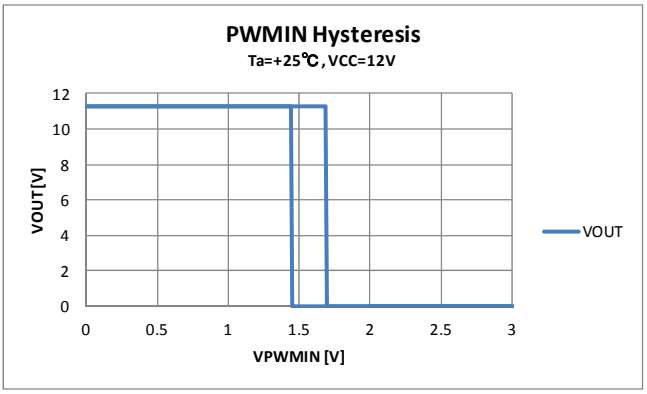


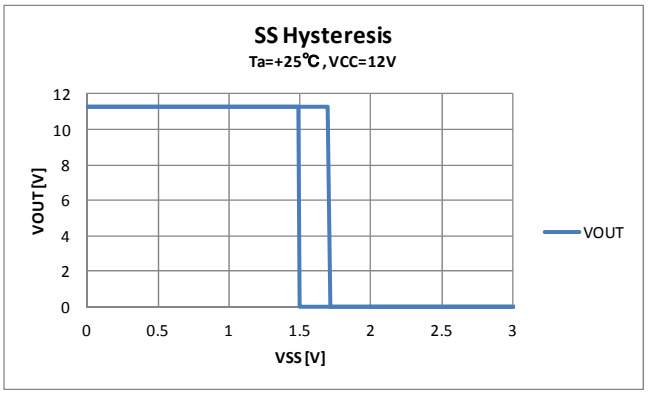


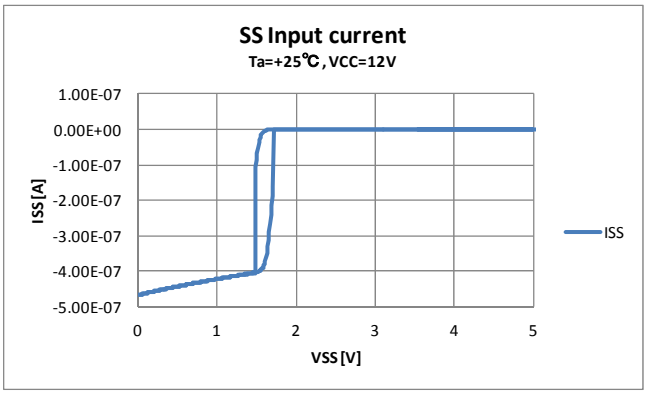


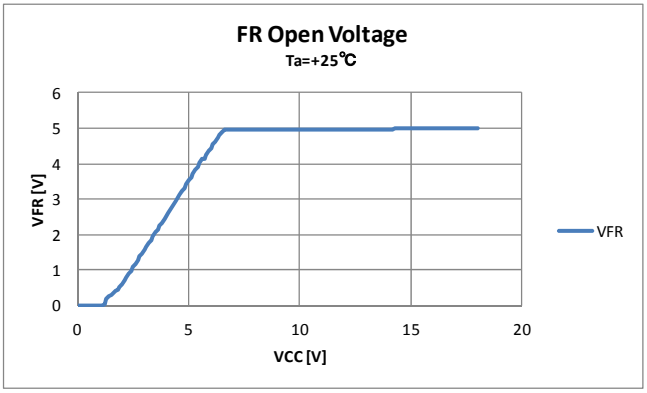


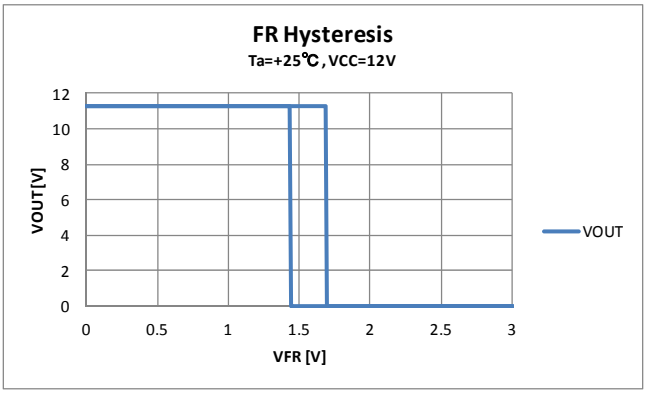


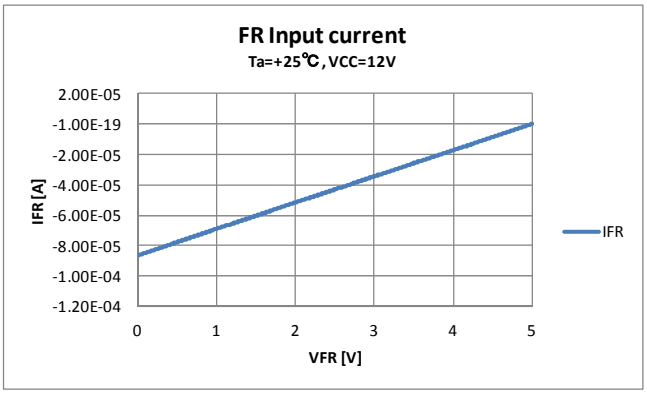


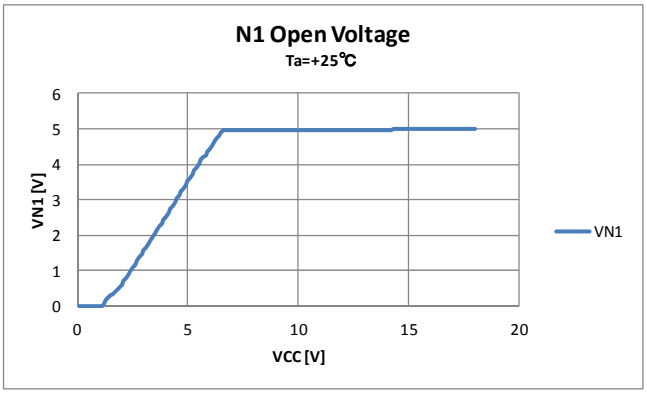


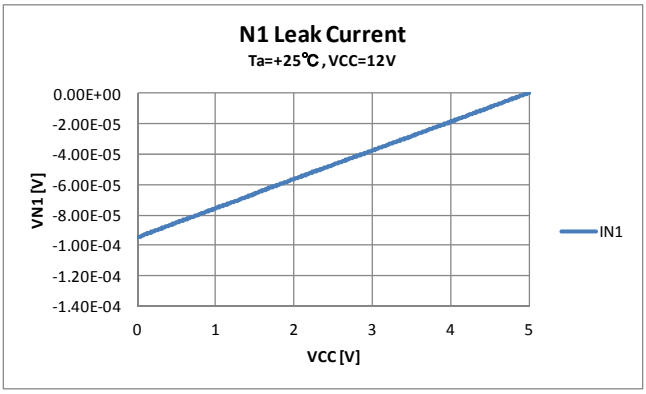


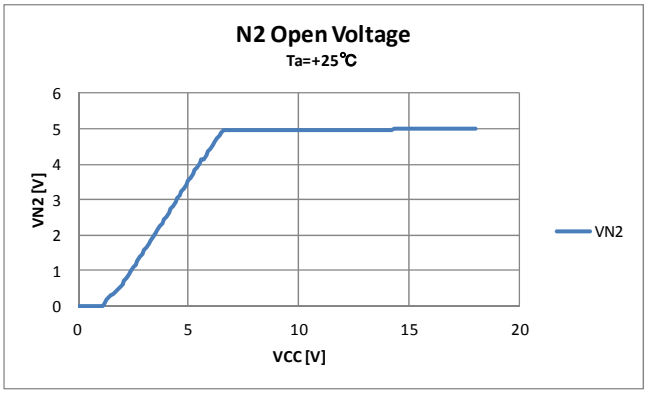


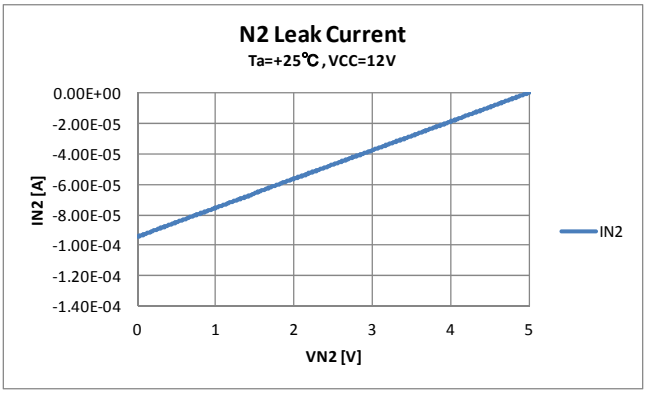












• Three-Phase Logic Truth Table (IN = “H” indicates the state where $IN^+ > IN^-$)

	F/R = “L”			F/R=“H”			Output	
	IN1	IN2	IN3	IN1	IN2	IN3	PWM	
1	H	L	H	L	H	L	VH	UL
2	H	L	L	L	H	H	WH	UL
3	H	H	L	L	L	H	WH	VL
4	L	H	L	H	L	H	UH	VL
5	L	H	H	H	L	L	UH	WL
6	L	L	H	H	H	L	VH	WL

• S/S pin

Input state	State
High	Stop
Low	Start

• PWMIN pin

Input state	State
High or open	Output off
Low	Output on

If the PWM pin is not used, the input must be held at the low level.

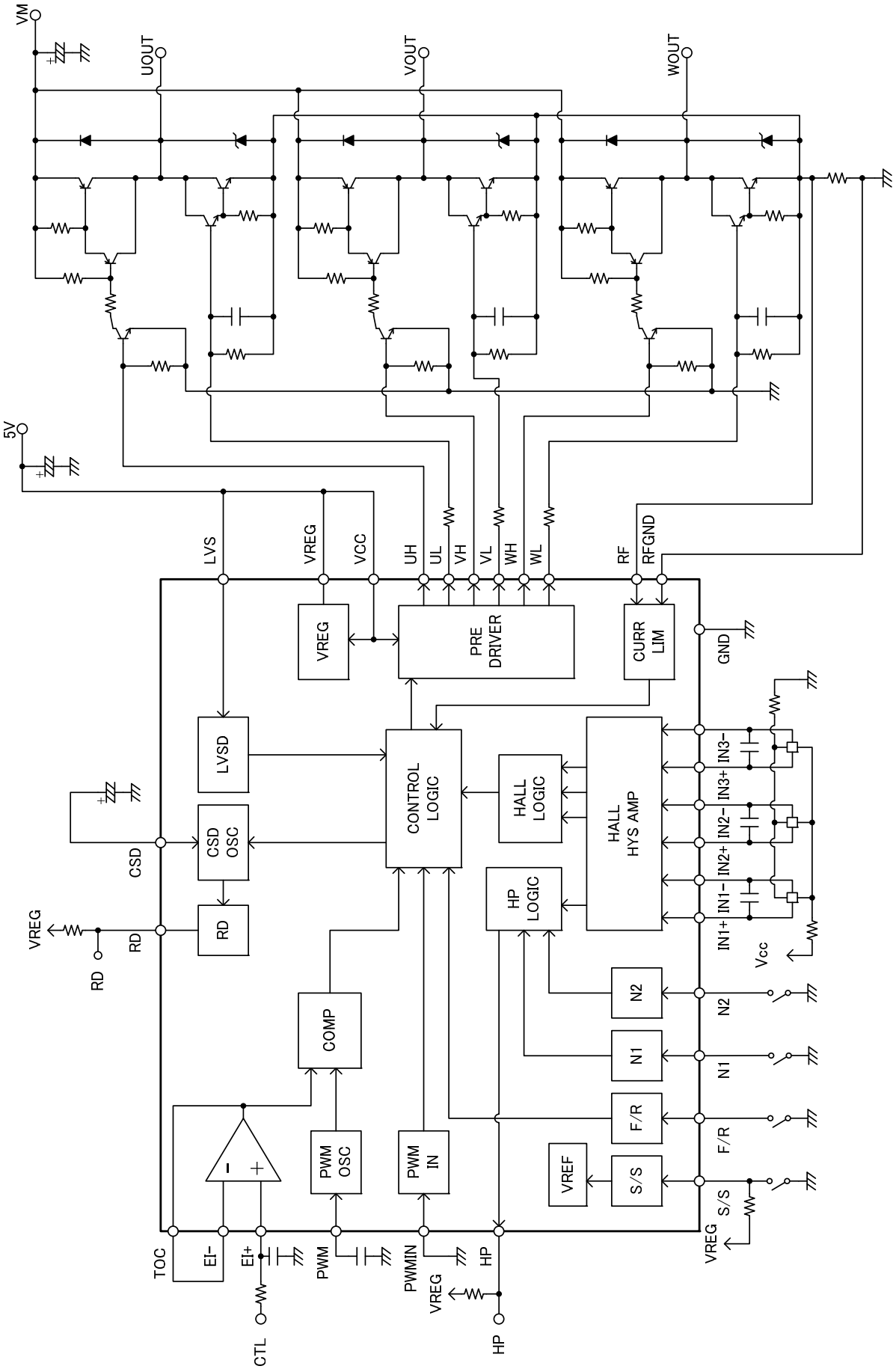
• N1 and N2 pins

Input state		HP output
N1 pin	N2 pin	
Low	Low	Single Hall sensor period divided by 2
Low	High or open	Single Hall sensor period
High or open	Low	Three Hall sensor synthesized period divided by 2
High or open	High or open	Three Hall sensor synthesized period

Since the S/S pin does not have an internal pull-up resistor, an external pull-up resistor or equivalent is required to set the IC to the stop state. If either the S/S or PWMIN pins are not used, the unused pin input must be set to the low-level voltage.
The HP output can be selected (by the N1 and N2 settings) to be one of the following four functions: the IN1 Hall input converted to a pulse output (one-Hall output), the one-Hall output divided by two, the three-phase output synthesized from the Hall inputs (three-Hall synthesized output) or the three-Hall synthesized output divided by two.

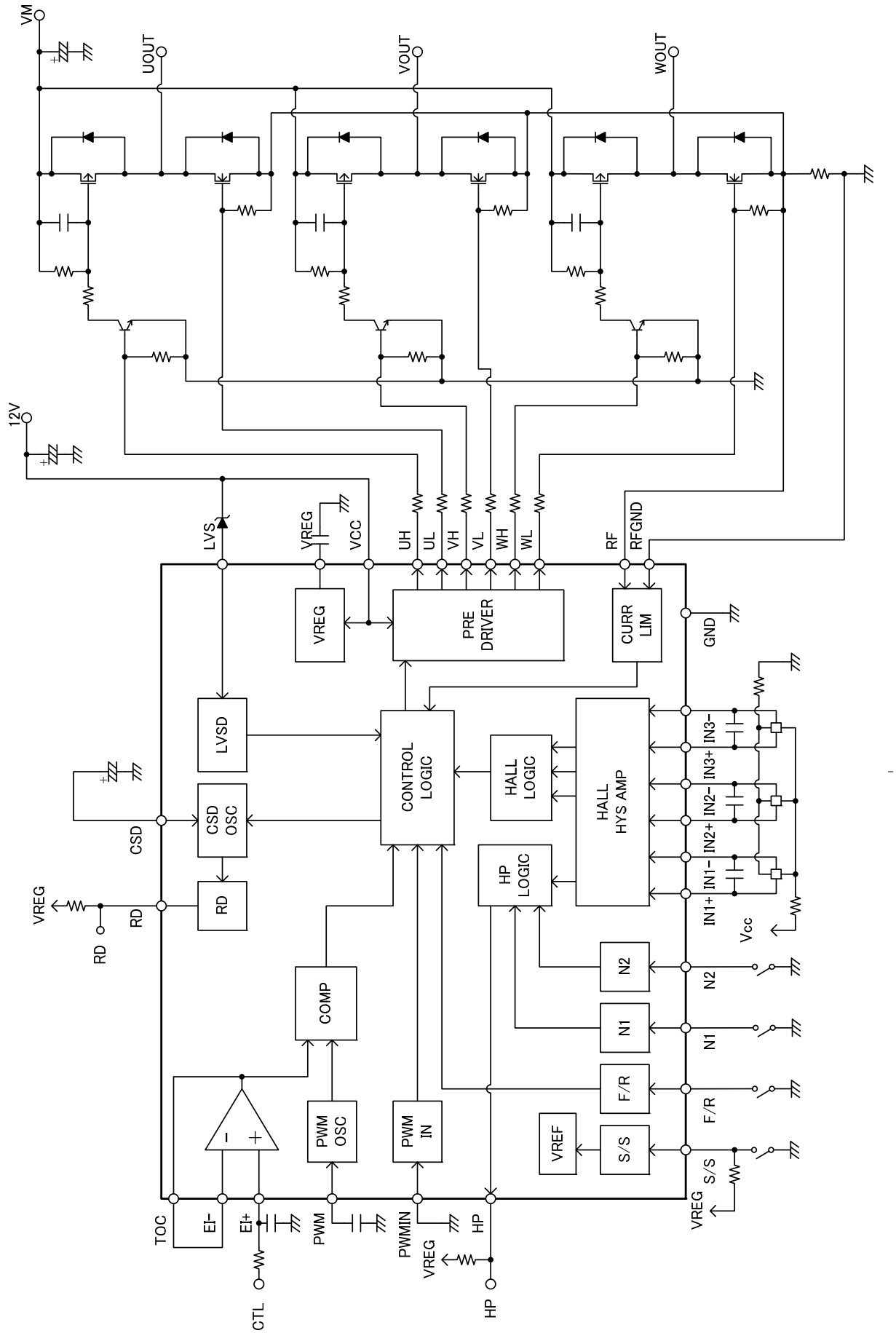
Application Circuit Example 1

Bipolar transistor drive (high side PWM) using 5V power supply



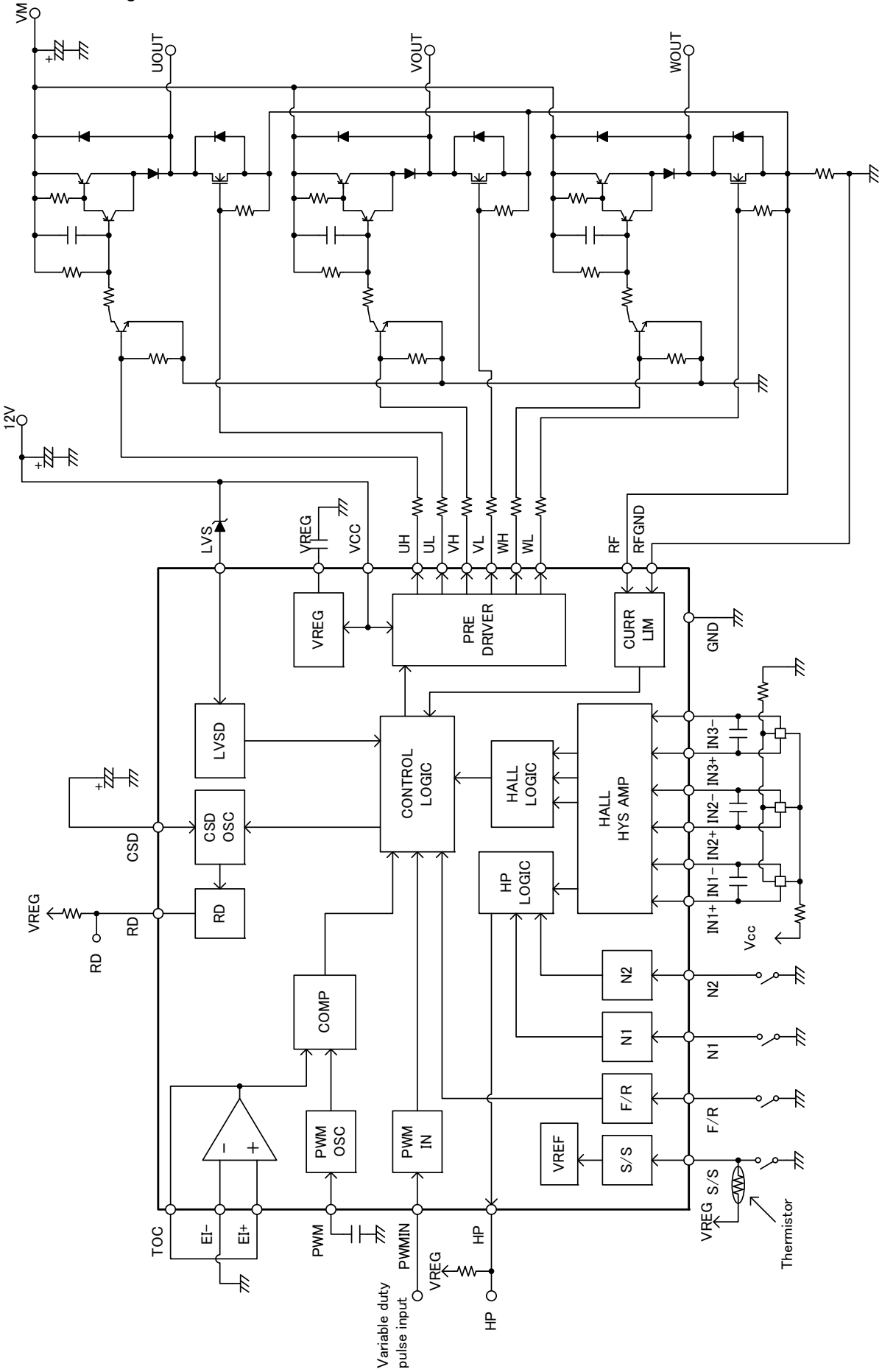
Application Circuit Example 2

MOS transistor drive (low side PWM) using 12V power supply

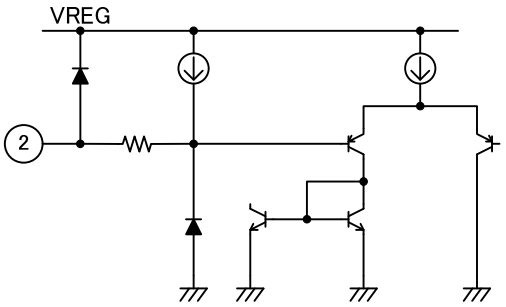
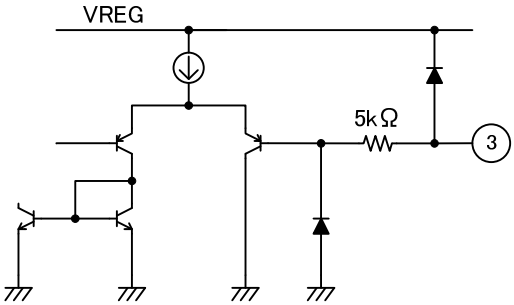
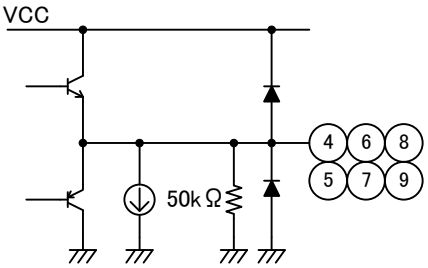
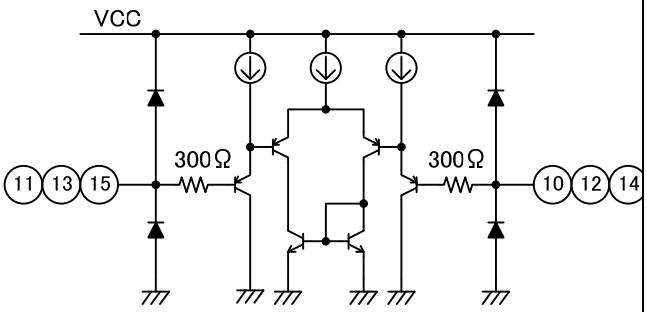
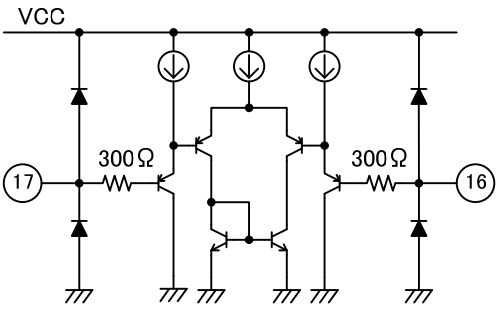


Application Circuit Example 3 (Hall element, FET)

NMOS transistor + PNP transistor drive (low side PWM) using 12V power supply with thermal protection implemented using thermistor



Pin Functions

Pin No.	Pin Name	Pin function	Equivalent Circuit
1	GND	Ground pin of the control circuit block.	
2	RFGND	Output current detection reference pin. Connect the ground terminal of external resistor RF to this pin.	
3	RF	Output current detection pin. Connect a resistor (Rf) with a small value between this pin and RFGND. This sets the maximum output current I_{OUT} to be 0.25V/Rf.	
4 6 8 5 7 9	WH VH UH WL VL UL	Outputs (External transistor drive outputs) The duty control applies to the UH, VH, and WH pins.	
10 11 12 13 14 15	$IN1^-$ $IN1^+$ $IN2^-$ $IN2^+$ $IN3^-$ $IN3^+$	Hall sensor signal input pins. A high-level state is recognized when IN+ > IN-, and a low-level state is recognized under the reverse condition. If noise on the Hall sensor signal becomes a problem, insert capacitors between the IN+ and IN- inputs.	
16 17	EI+ EI-	Control amplifier inputs. The PWMIN pin must be held at the low level for control using this pin to function.	

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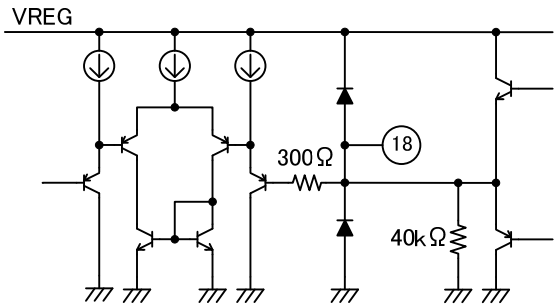
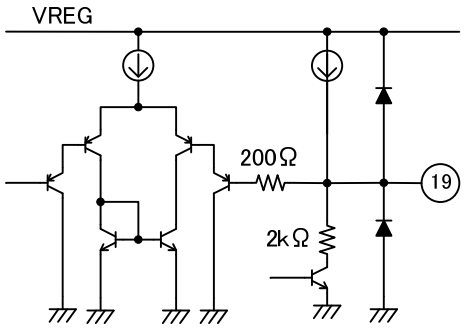
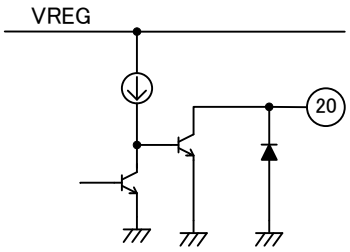
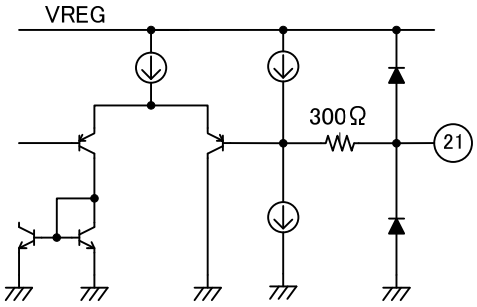
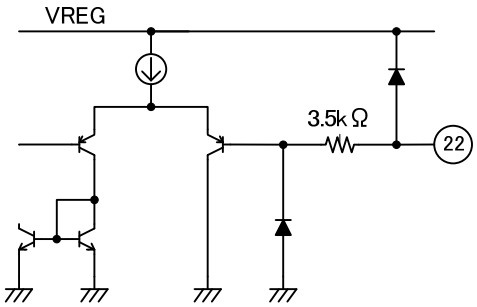
Pin No.	Pin Name	Pin function	Equivalent Circuit
18	TOC	Control amplifier output pin. When the TOC pin voltage rises, the IC changes the UH, VH, and WH output signal PWM duty to increase the torque output.	
19	PWM	Shared function pin: PWM oscillator frequency setting and initial reset pulse generation Insert a capacitor between this pin and ground. A capacitor of 2000pF sets a frequency of about 22kHz.	
20	RD	Motor constraint detection output pin This pin output is on when the motor is turning and off when the constraint protection circuit operates.	
21	CSD	Constraint protection circuit operating time setting insert a capacitor between this pin and ground. This pin must be connected to ground if the constraint protection circuit is not used.	
22	S/S	Start/Stop input pin. A low-level input sets the IC to start mode, and a high-level input sets it to stop mode.	

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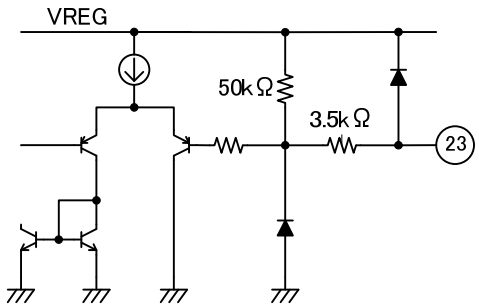
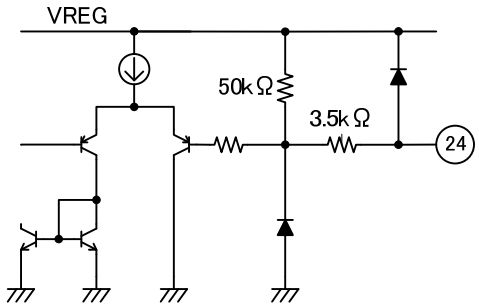
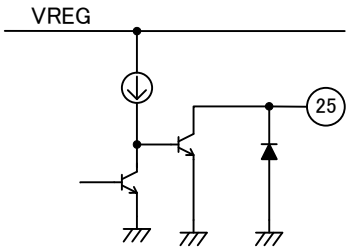
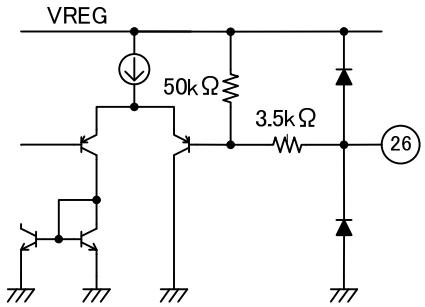
Pin No.	Pin Name	Pin function	Equivalent Circuit
23	PWMIN	PWM pulse input pin. A low-level input specifies the output drive state, and a high-level or open input specifies the output off state. When this pin is used for control, the TOC pin voltage must be set to a control amplifier input that results in a 100% duty.	
24	F/R	F/R Forward/reverse rotation setting pin. A low-level specifies forward rotation and a high-level specifies reverse rotation. This pin is held high when open.	
25	HP	Hall signal output pin. (this is an open-collector output) One of four output types is selected by the N1 and N2 pin settings.	
26	N1	Hall signal output (HP signal) type selector pin.	

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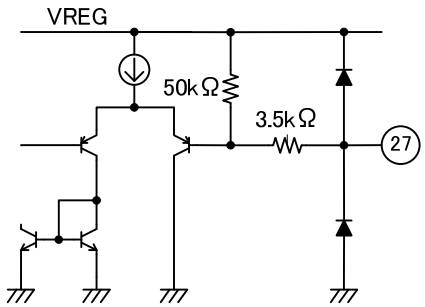
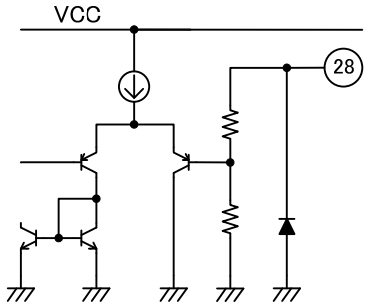
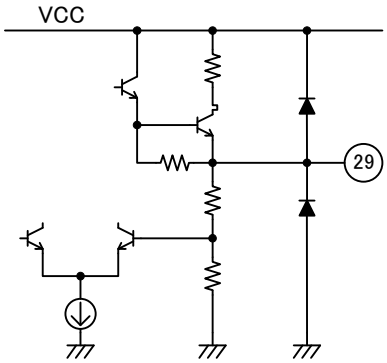
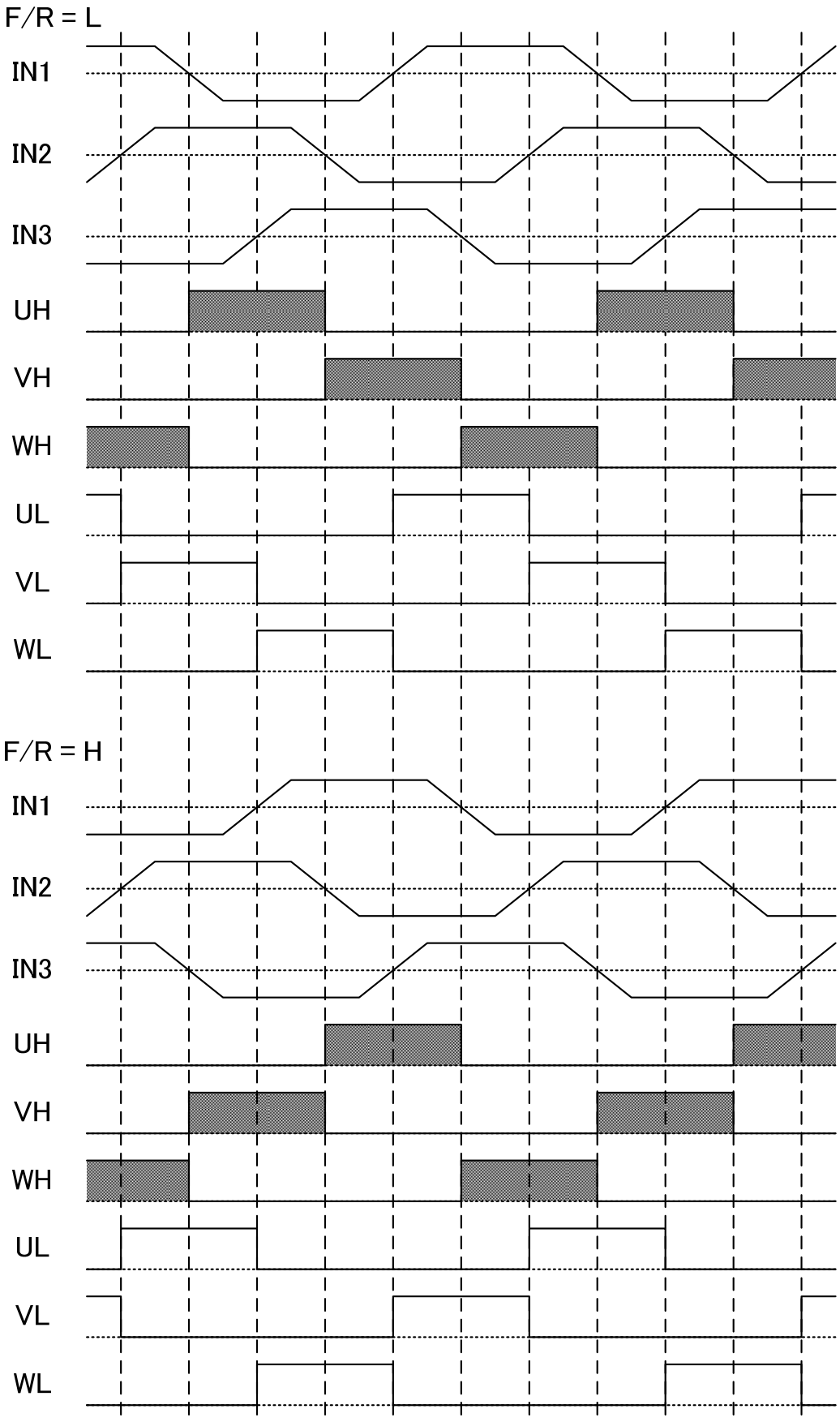
Pin No.	Pin Name	Pin function	Equivalent Circuit
27	N2	Hall signal output (HP signal) type selector pin.	
28	LVS	Under-voltage protection voltage detection pin. If 5V or higher supply voltage is to be detected, set the detection voltage by inserting an appropriate zener diode in series.	
29	VREG	Stabilized power supply output (5V output) pin Insert a capacitor (about 0.1μF) between this pin and ground for power stabilization.	
30	V_{CC}	Power supply pin. Insert a capacitor between this pin and ground to prevent the influence of noise, etc.	

Hall Sensor Signal Input / Output Timing Chart

(IN = “H” indicates the state in which IN^+ is greater than IN^-.)



Areas shown in gray ( ) indicate PWM output

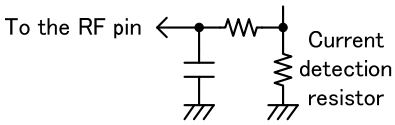
LB11696V Functional Description

1. Output Drive Circuit

The LB11696V adopts direct PWM drive to minimize power loss in the output. The output transistor are always saturated when on, and motor drive power is adjusted by changing the on duty of the output. The output PWM switching is performed on the UH, VH, and WH output. Since the UL to WL and UH to WH outputs have the same output form, applications can select either low side PWM or high side PWM drive by changing the way the external output transistors are connected. Since the reverse recovery time of the diodes connected to the non-PWM side of the outputs is a problem, these devices must be selected with care. (This is because through currents will flow at the instant the PWM side transistors turn on if diodes with a short reverse recovery time are not used.)

2. Current Limiter Circuit

The current limiter circuit limits the output current peak value to a level Determined by the equation I = VFR / Rf (VFR = 0.25V typical, Rf: current detection resistor). This circuit suppresses the output current by reducing the output on duty.

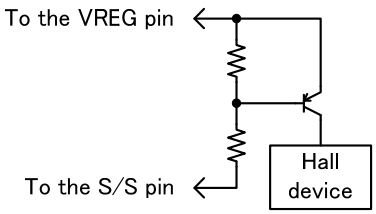


High-precision detection can be implemented by connecting the lines from the RF and RFGND pins close to the two terminal of the current detection resistor Rf.

The current limiter circuit includes an internal filter circuit to prevent incorrect current limiter circuit operation due to detecting the output diode reverse recovery current due to PWM operation. Although there should be no problems with the internal filter circuit in normal applications, applications should add an external filter circuit (such as an RC low-pass filter) if incorrect operation occurs (if the diode recovery current flows for longer than 1μs).

3. Power Saving Circuit

This IC goes to a low-power mode (power saving state) when set to the stop state with the S/S pin. In the power saving state, the bias currents in most of the circuits are cut off. However, the 5V regulator output (VREG) is still provided in the power saving state. If it is also necessary to cut the Hall device bias current, this function can be provided by an application that, for example, connects the Hall devices to 5V through PNP transistors.



4. Notes on PWM Frequency

The PWM frequency is determined by the capacitor C (F) connected to the PWM pin.

$$fPWM \approx 1/(22500 \times C)$$

If a 2000pF capacitor is used, the circuit will oscillate at about 22kHz. If the PWM frequency is too low, switching noise will be audible from the motor, and if is too high, the output power loss will increase. Thus a frequency in the range 15k to 50kHz must be used. The capacitor's ground terminal must be placed as close as possible to the IC's ground pin to minimize the influence of output noise and other noise sources.

5. Control Methods

The output duty can be controlled by either of the following methods

*Control based on comparing the TOC pin voltage to the PWM oscillator waveform

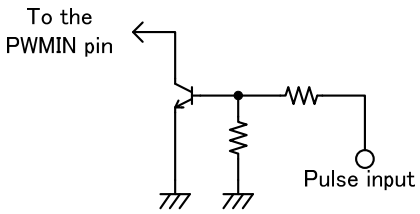
The low side output transistor duty is determined according to the result of comparing the TOC pin voltage to the PWM oscillator waveform. When the TOC pin voltage is 1.35V or lower, the duty will be 0%, and when it is 3.0V or higher, the duty will be 100%.

Since the TOC pin is the output of the control amplifier (CTL), a control voltage cannot be directly input to the TOC pin. Normally, the control amplifier is used as a full feedback amplifier (with the EI- pin connected to the TOC pin) and a DC voltage is input to EI+ pin (the EI+ pin voltage will become equal to the TOC pin voltage). When the EI+ pin voltage becomes higher, the output duty increases. Since the motor will be driven when the EI+ pin in the open state, a pull-down resistor must be connected to the EI+ pin if the motor should not operate when EI+ is open.

When TOC pin voltage control is used, a low-level input must be applied to the PWMIN pin or that pin connected to ground.

* Pulse Control Using the PWMIN Pin

A pulse signal can be input to the PWMIN pin, and the output can be controlled based on the duty of that signal. Note that the output is on when a low level is input to the PWMIN pin, and off when a high level is input. When the PWMIN pin is open it goes to the high level and the output is turned off.
If inverted input logic is required, this can be implemented with an external transistor (npn).
When controlling motor operation from the PWMIN pin, the EI- pin must be connected to ground, and the EI+ pin must be connected to the TOC pin.
Note that since the PWM oscillator is also used as the clock for internal circuits, a capacitor (about 2000pF) must be connected to the PWM pin even if the PWMIN pin is used for motor control.

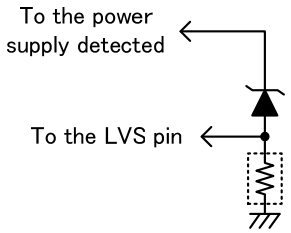


6. Hall Input Signals

A signal input with an amplitude in excess of the hysteresis (80mV maximum) is required for the Hall inputs. Considering the possibility of noise and phase displacement, an even larger amplitude is desirable.
If disruptions to the output waveforms (during phase switching) or to the HP output (Hall signal output) occur due to noise, this must be prevented by inserting capacitors across the inputs. The constraint protection circuit uses the Hall inputs to discriminate the motor constraint state. Although the circuit is designed to tolerate a certain amount of noise, care is required when using the constraint protection circuit.
If all three phases of the Hall input signal system go to the same input state, the outputs are all set to the off state (the UL, VL, WL, UH, VH, and WH outputs all go to the low level).
If the outputs from a Hall IC are used, fixing one side of the inputs (either the + or – side) at a voltage within the common-mode input voltage range allows the other input side to be used as an input over the 0V to V_{CC} range.

7. Under-voltage Protection Circuit

The under-voltage protection circuit turns one side of the outputs (UH, VH, and WH) off when the LVS pin voltage falls below the minimum operation voltage (see the Electrical Characteristics). To prevent this circuit from repeatedly turning the outputs on and off in the vicinity of the protection operating voltage, this circuit is designed with hysteresis. Thus the output will not recover until the operating voltage rises 0.45V (typical).
The protection operating voltage detection level is set up for 5V systems.
The detected voltage level can be increased by shifting the detection level.
The LVS influx current during detection is about 75μA. To increase the diode current to stabilize the zener diode voltage rise, insert a resistor between the LVS pin and ground.



If the LVS pin is left open, the internal pull-down resistor will result in the IC seeing a ground level input, and the output will be turned off. Therefore, a voltage in excess of the LVS circuit clear voltage (about 4.35V) must be applied to the LVS pin if the application does not use the under-voltage protection circuit. The maximum rating for the LVS pin applied voltage is 18V.

8. Constraint Protection Circuit

When the motor is physically constrained (held stopped), the CSD pin external capacitor is charged (to about 3.0V) by a constant current of about 2.5μA and is then discharged (to about 1.0V) by a constant current of about 0.14μA.
This process is repeated, generating a saw-tooth waveform. The constraint protection circuit turns motor drive on and off repeatedly based on this saw-tooth waveform. (The UH, VH, and WH side outputs are turned on and off.) Motor drive is on during the period the CSD pin external capacitor is being charged from about 1.0V to about 3.0V, and motor drive is off during the period the CSD pin external capacitor is being discharged from about 3.0V to about 1.0V.
The IC and the motor are protected by this repeated drive on/off operation when the motor is physically constrained.

The motor drive on and off times are determined by the value of the connected capacitor C (in μF).

TCSD1 (drive on period) ≈ 0.8 × C (seconds)
TCSD2 (drive off period) ≈ 14.3 × C (seconds)

When a 0.47μF capacitor is connected externally to the CSD pin, this iterated operation will have a drive on period of about 0.38 seconds and a drive off period of about 6.7 seconds.

While the motor is turning, the discharge pulse signal (generated once for each Hall input period) that is created by combining the Hall inputs internally in the IC discharges the CSD pin external capacitor. Since the CSD pin voltage does not rise, the constraint protection circuit does not operate.

When the motor is physically constrained, the Hall inputs do not change and the discharge pulses are not generated.
As a result, the CSD pin external capacitor is charged by a constant current of 2.5μA to about 3.0V, at which point the constraint protection circuit operates. When the constraint on the motor is released, the constraint protection function is released.
Connect the CSD pin to ground if the constraint protection circuit is not used.

9. Forward/Reverse Direction Switching
This IC is designed so that through currents (due to the output transistor off delay time when switching) do not flow in the output when switching directions when the motor is turning. However, if the direction is switched when the motor is turning, current levels in excess of the current limiter value may flow in the output transistors due to the motor coil resistance and the motor back EMF state when switching. Therefore, designers must consider selecting external output transistors that are not destroyed by those current levels or only switching directions after the speed has fallen below a certain speed.

10. Handling Different Power Supply Types
When this IC is operated from an externally supplied 5V power supply (4.5 to 5.5V), short the V_{CC} pin to the VREG pin and connect them to the external power supply.
When this IC is operated from an externally supplied 12V power supply (8 to 17 V), connect the V_{CC} pin to the power supply. (The VREG pin will generate a 5V level to function as the control circuit power supply.)

11. Power Supply Stabilization
Since this IC uses a switching drive technique, the power supply line level can be disturbed easily. Therefore capacitors with adequate capacitance to stabilize the power supply line must be inserted between V_{CC} and ground.
If diodes are inserted in the power supply lines to prevent destruction if the power supply is connected with reverse polarity, the power supply lines are even more easily disrupted, and even larger capacitors are required.
If the power supply is turned on and off by a switch, and if there is a significant distance between that switch and the stabilization capacitor, the supply voltage can be disrupted significantly by the line inductance and surge current into the capacitor. As a result, the withstand voltage of the device may be exceeded. In application such as this, the surge current must be suppressed and the voltage rise prevented by not using ceramic capacitors with a low series impedance, and by using electrolytic capacitors instead.

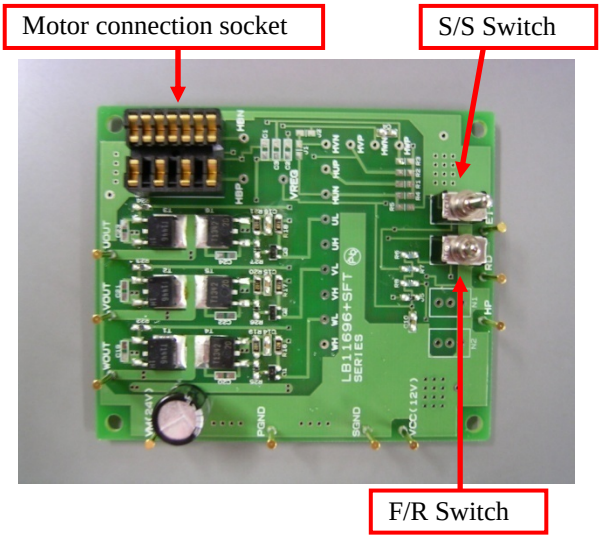
12. VREG Stabilization
To stabilize the VREG voltage, which is the control circuit power supply, a 0.1μF or larger capacitor must be inserted between the VREG pin and ground. The ground side of this capacitor must connected to the IC ground pin with a line that is as short as possible.

Evaluation Board Manual

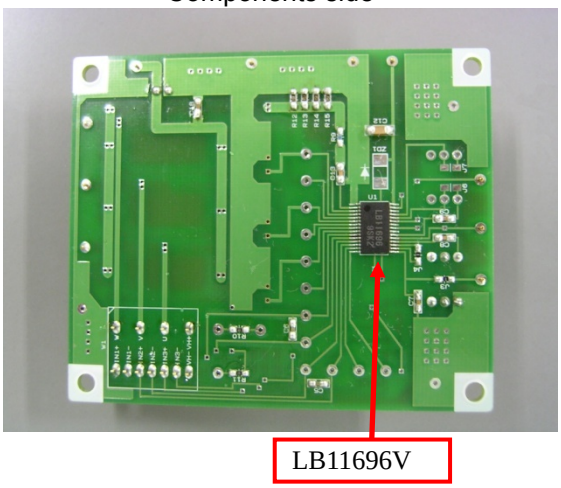
*This board is designed for Hall element input.

*To use Hall IC input to this board: Please check the application board circuit for Hall IC input.

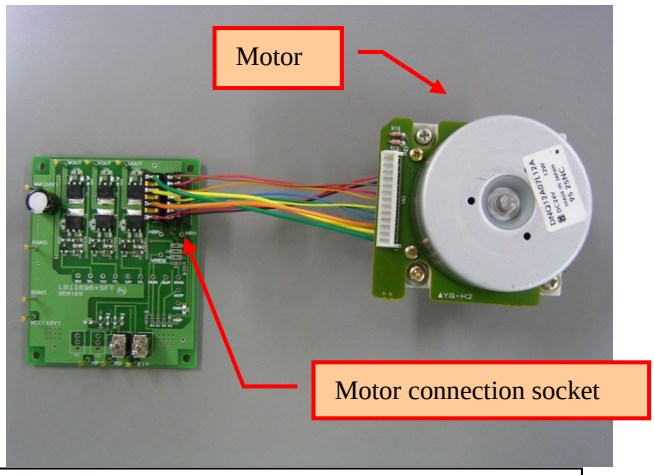
Wire Connection View of Application board



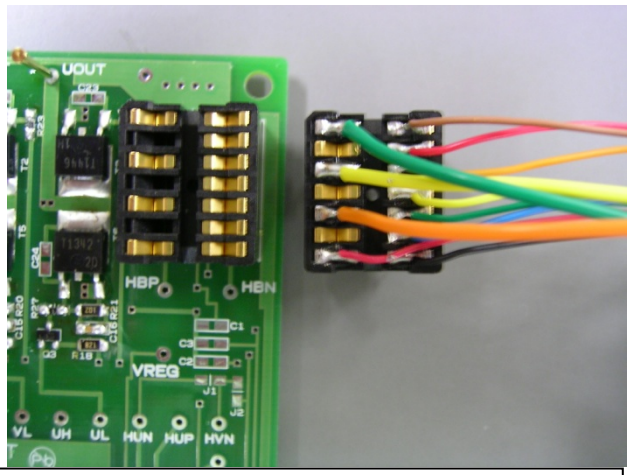
Wire Connection View of Application board
Hall element input
Components side



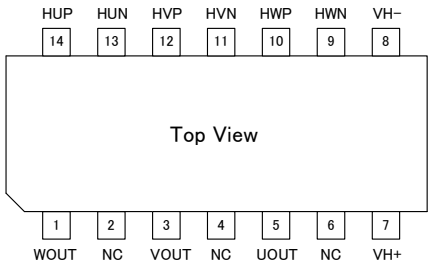
Connection Image…
Image of the motor and application board connection.



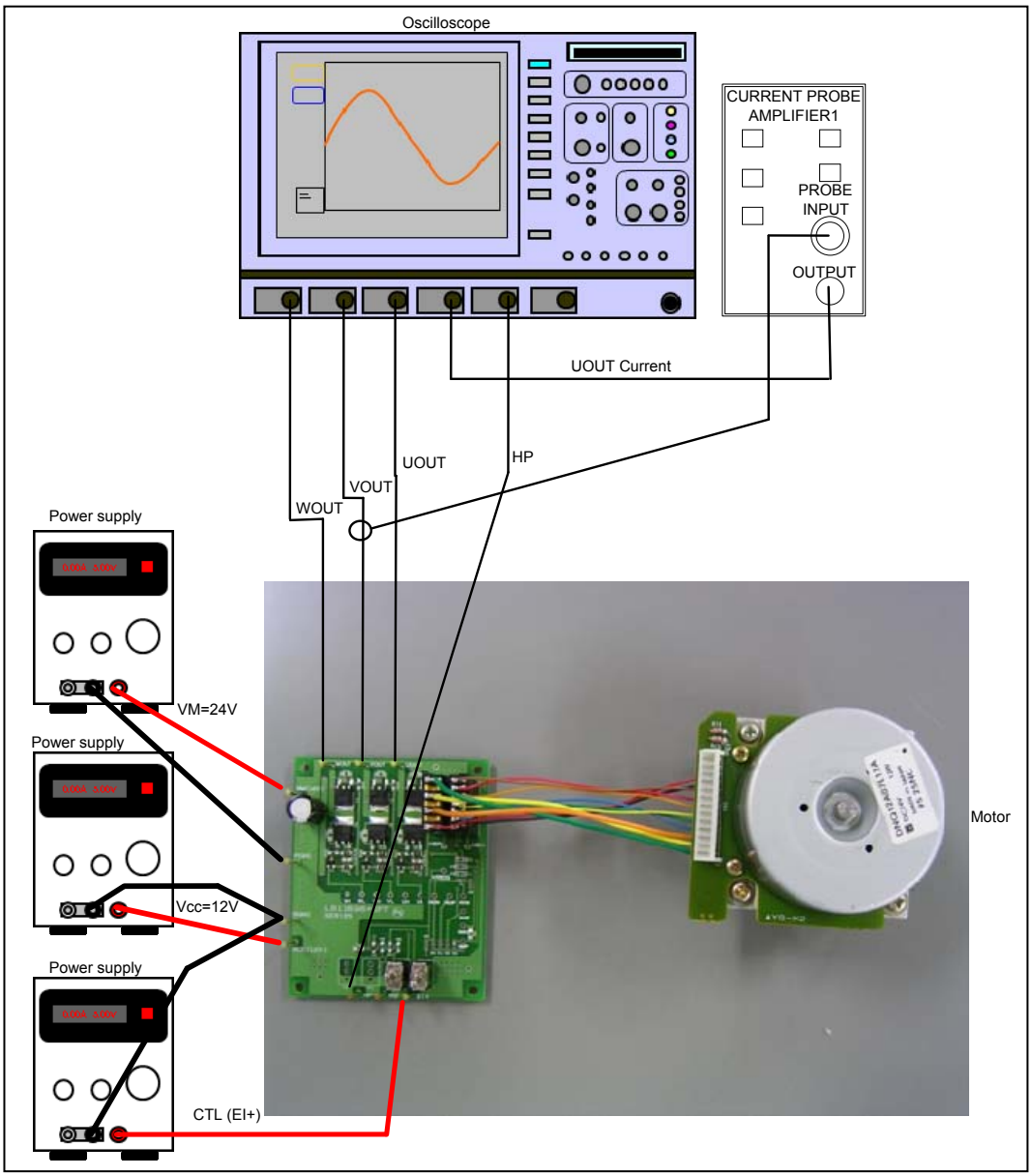
Socket pin assignment for motor connection



Motor connection socket (for Hall element input)



UOUT, VOUT, WOUT	:Motor driver output
VH+, VH-	:Hall element Bias
HUP, HVP, HWP	:Hall element signal input +
HUN , HVN, HWN	:Hall element signal input -



Test Procedure:

1. Connect the test setup as shown above.

2. Connect CTL power supply (0V to VREG) between EI+ and GND. First, set to 0V.

3. Connect IC power supply (8V to 17V) between VCC and GND. First, set to 12V.

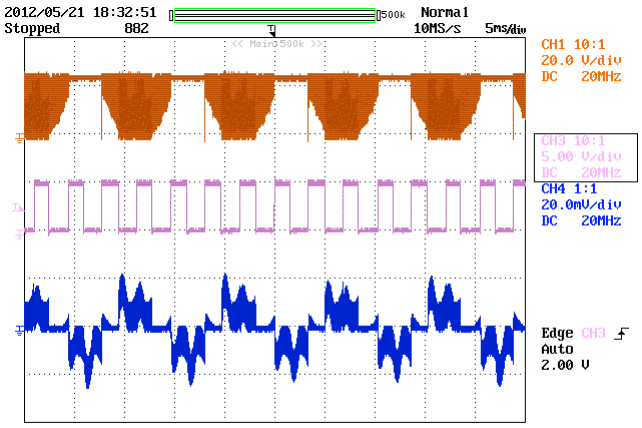
4. Connect motor power supply between VM and GND. *Initially, please set a lower voltage than the rated voltage of the VM for safety. (*Maximum voltage of capacitor C17 is 100V. Please use the ones that are sufficient to withstand voltage VM.)
   For example, in the case of VM=24Vtyp, please start from VM = 12V (approx.).

5. Please increase EI+ voltage to 3.0V.

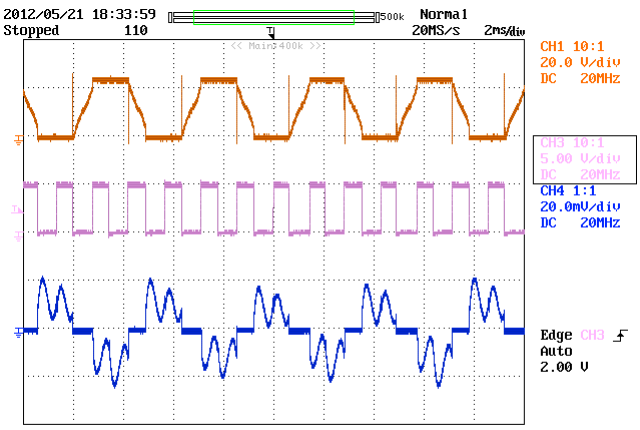
- **Initial check**
  Confirm that the motor rotates smoothly and in the correct direction.
  Check the some waveforms.
  Check the UOUT, VOUT, WOUT, RD and HP voltage waveform, and the output current waveform of UOUT by the oscilloscope.

ex) Waveforms can vary depend on usage motors.
VCC=12V, VM=24V, F/R=L

CH1:V-OUT, CH3=HP, CH4=V-OUT current
EI+=2.0V



CH1:V-OUT, CH3=HP, CH4=V-OUT current
EI+=3.0V



The case of Hall Element Input:
Evaluation Board Circuit Diagram (Hall Element Input) (Page27)
Please change the connection of Hall Sensor from VH+ and VH-.

The case of Hall IC Input:
Please refer to Evaluation Board Circuit Diagram (Hall IC Input) (Page32)

- **Speed control check**
  You can control rotation of the motor by changing the voltage of “EI+”(16PIN).
  EI+ input voltage ranges from 0 to VREG. Depends on voltage, a mode is switched into 2 types of modes: , Stop Mode and Drive Mode.
  (Drive Mode: 1.0V≤VCTL≤3.0V (TYP))
  Please refer to development specification for the details of each mode.
  - **Stop Mode** (0V<CTL<1.0) Motor rotation stop.
  - **Drive Mode** (1.0V<CTL<3.0V) Output PWM DUTY is controllable from 0% to 100%.

- **Forward/Reverse rotation check**
  “F/R” (24PIN) includes switch (SW) to select between VREG/GND.
  You can switch between forward/reverse.
  *Please do not use the switch while the motor is in rotation.

- **Lock detection check (Motor-Lock-mode)**
  Check the Lock detection behavior. (Lock)
  At each VCC, stop the Motor manually by force.
  After about 6.7 seconds, the motor will start rotation automatically.

- **Start/Stop check**
  “S/S” (22PIN) includes switch (SW) to select between VREG/GND.
  You can switch between Start/Stop mode.
  “H”:Stop Mode (2.0V<S/S)
  “L”:Start Mode (S/S<1.0V)

Note: This board is for evaluations. We do not guarantee the movement with the real product. When you perform a product design using the part fixed number of this board, please evaluate it enough.

***Other Settings**

1. Motor lock protection circuit

Time is configured according to capacity of the capacitor (C9) connected to “CSD”(21PIN).

C=0.47μF (CSD pin)

Drive on period setting time≈**0.38s**

Drive on period setting time (s) ≈0.8×C (μF)

Drive off period setting time≈**6.7s**

Drive off period setting time (s) ≈14.3×C (μF)

* Connect CSD pin to GND when lock protection is not used.

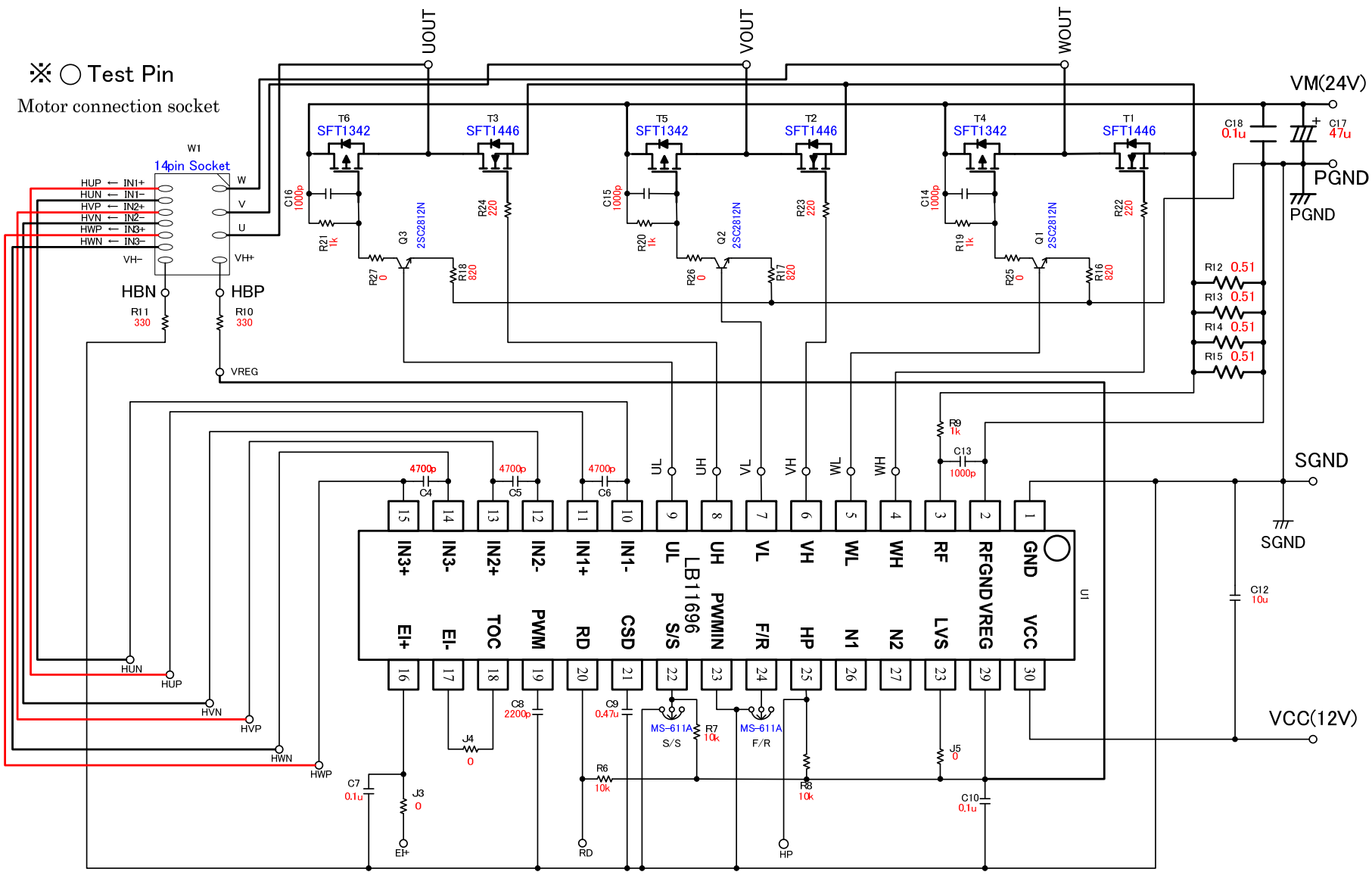
2. Current limit is adjustable with resistors (R12, R13, R14, R15) connected between “RF”(3PIN) and RFGND. This circuit limits peak current according to the current which is obtained as follows: I=VRF/Rf (VRF=0.25Vtyp, Rf: current detection resistance).

Setting value of the peripheral parts is 2.0A.

3. PWM frequency is 20kHz. (C8=2200pF)

*Make sure to use parts with good temperature characteristics.

Evaluation Board Circuit Diagram
(Hall element input)



Bill of Materials for LB11696V Evaluation Board (Hall element input)

Designator	Quantity	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Lead Free
U1	1	Motor Pre-Driver	-	-	SSOP30 (275mil)	ON Semiconductor	LB11696V	No	yes
Q1	1	WL:NPN Tr. for inverted logic	-	-	CPA	ON Semiconductor	2SC2812N	yes	yes
Q2	1	VL:NPN Tr. for inverted logic	-	-	CPA	ON Semiconductor	2SC2812N	yes	yes
Q3	1	UL:NPN Tr. for inverted logic	-	-	CPA	ON Semiconductor	2SC2812N	yes	yes
T1	1	W:Nch FET for low side driver	-	-	TP-FA	ON Semiconductor	SFT1446	yes	yes
T2	1	V:Nch FET for low side driver	-	-	TP-FA	ON Semiconductor	SFT1446	yes	yes
T3	1	U:Nch FET for low side driver	-	-	TP-FA	ON Semiconductor	SFT1446	yes	yes
T4	1	W:Pch FET for high side driver	-	-	TP-FA	ON Semiconductor	SFT1342	yes	yes
T5	1	V:Pch FET for high side driver	-	-	TP-FA	ON Semiconductor	SFT1342	yes	yes
T6	1	U:Pch FET for high side driver	-	-	TP-FA	ON Semiconductor	SFT1342	yes	yes
SW(S/S)	1	Switch	-	-		MIYAMA	MS-611A-A01	yes	yes
SW(F/R)	1	Switch	-	-		MIYAMA	MS-611A-A01	yes	yes
TP1-TP10	10	Test points	-	-		MAC8	ST-1-3	yes	yes
Socket	1	Motor connection socket	-	-		YAMAICHI	IC-91-1403-G4	yes	yes
R6	1	RD(pull up)	10k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	yes	yes
R7	1	S/S(pull up)	10k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	yes	yes
R8	1	HP(pull up)	10k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	yes	yes
R9	1	RF (filter)	1k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD102J	yes	yes
R10	1	Hall bias VREG	330 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD331J	yes	yes
R11	1	Hall bias GND	330 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD331J	yes	yes
R12-15	4	RF	0.51 (0.25W)	±5%	2012 (0805Inch)	ROHM	MCR10EZHZJLR51	yes	yes
R16-18	3	NPN Tr. Emitter resistor	820 (0.33W)	±5%	3216 (1206Inch)	ROHM	ESR18EZPJ821	yes	yes
R19-21	3	Pch FET Gate to Source	1k (0.33W)	±5%	3216 (1206Inch)	ROHM	ESR18EZPJ102	yes	yes
R22-24	3	Nch FET Gate resistor	220 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD221J	yes	yes
R25-27	3	Jumper	0 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1J 0ΩJ	yes	yes
J3	1	EI+ Jumper	0 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1J 0ΩJ	yes	yes
J4	1	EI-(to TOC)	0 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1J 0ΩJ	yes	yes
J5	1	LVS(to VREG)	0 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1J 0ΩJ	yes	yes
C4	1	IN3+/ -	4700pF /50V	±5%	1608 (0603Inch)	MURATA	GRM188B11H472K	yes	yes
C5	1	IN2+/ -	4700pF /50V	±5%	1608 (0603Inch)	MURATA	GRM188B11H472K	yes	yes
C6	1	IN1+/ -	4700pF /50V	±5%	1608 (0603Inch)	MURATA	GRM188B11H472K	yes	yes

Continued on next page.

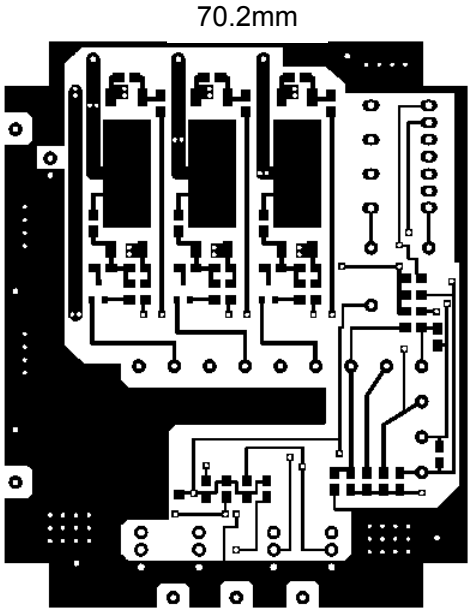
Continued from preceding page.

C7	1	EI+ Bypass Capacitor	0.1uF /25V	±10%	1608 (0603Inch)	MURATA	GRM188B11E104K	yes	yes
C8	1	PWM	2200pF /50V	±5%	1608 (0603Inch)	MURATA	GRM1882C1H222J	yes	yes
C9	1	CSD	0.47uF /25V	±10%	1608 (0603Inch)	MURATA	GRM188B31E474KA	yes	yes
C10	1	VREG Bypass capacitor	0.1uF /25V	±10%	1608 (0603Inch)	MURATA	GRM188B11E104K	yes	yes
C12	1	VCC Bypass Capacitor	10uF /25V	±10%	3216 (1206Inch)	MURATA	GRM31CB31E106KA	yes	yes
C13	1	RF (filter)	1000pF /50V	±5%	1608 (0603Inch)	MURATA	GRM1882C1H102J	yes	yes
C14-16	1	Pch FET Gate to Source	1000pF /50V	±5%	1608 (0603Inch)	MURATA	GRM1882C1H102J	yes	yes
C17	1	VM Bypass Capacitor	47uF /100V	±20%	-	PANASONIC	ECA2AHG470	yes	yes
C18	1	VM Bypass Capacitor	0.1uF /25V	±10%	1608 (0603Inch)	MURATA	GRM188B11E104K	yes	yes

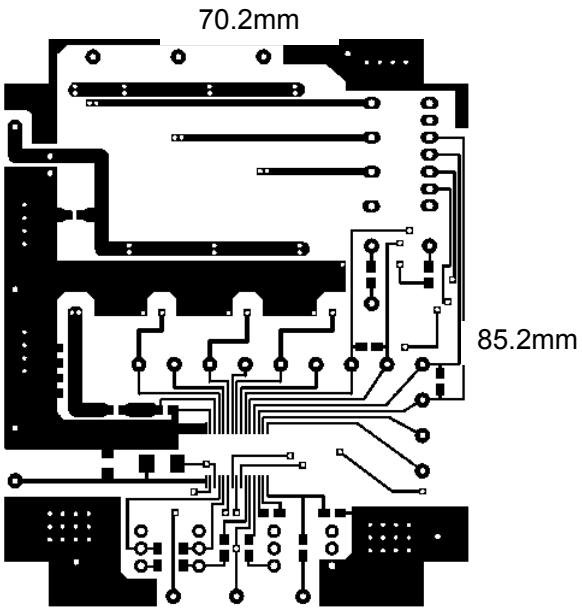
The points for attention in design applications

- VM, and each OUT, where large current flows should be laid out as fat and short as possible.
- VM and each OUT of high voltage line should be separated at least 3.2 mm or more from other patterns.
- VM bypass capacitor should be mounted as near as possible to Source pin of SFT1342.
- VCC bypass capacitor should be mounted as near as possible to VCC pin of LB11696V.
- VREG bypass capacitor should be mounted as near as possible to VREG pin.
- Do not exceed the absolute maximum ratings under no circumstance.
- "PGND" is the ground of the power system. "GND" is a small signal ground. They need to be laid out without any common impedance.
- The impedance of the island of GND needs to be as low as possible by making through-holes, for example.
- We recommend that the GND lines to connect a stabilization capacitor of VCC and to VM bypass capacitor are laid out independently and single-point-grounded at VM bypass capacitor
- VREG should be used in the IC as reference voltage. Capacitor should be connected between VREG pin and GND to stabilize VREG.
- VREG can be used as reference voltage for CTL(EI+) voltage setting. Therefore CTL(EI+) can be connected to VREG after having been devided with resistors.
- VREG can not be recommended to use for peripheral circuits because their output voltage are not so high in precision.
- F/R pin should be connected to 50kΩ pull-up in the chip. If the pin is open, the IC receives signals as H. But it may detect the signal falsely when the pin is affected by noise. When the pin is input H, it is recommended to switch to VREG pin.
- S/S pin is open. (High impedance) Therefore, when the pin is input H, it is recommended to switch to VREG. When the pin is input L, it is recommended to switch to ground.
- For CSD pin, make sure to connect this pin to GND when you do not use protection circuit.
- N1 & N2 pin should be connected to 50kΩ pull-up in the chip. If the pin is open, the IC receives signals as H. But it may detect the signal falsely when the pin is affected by noise. When the pin is input H, it is recommended to switch to VREG pin.

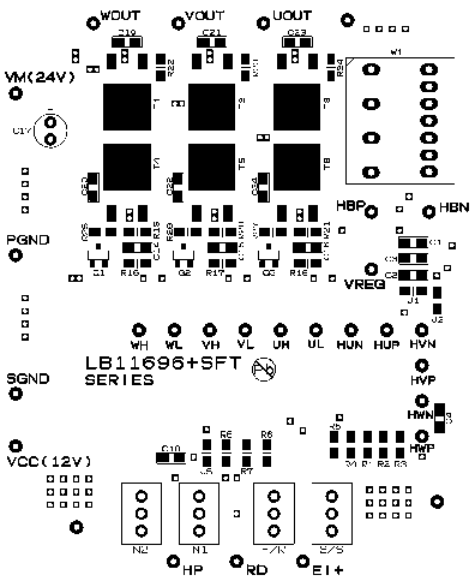
Evaluation Board PCB Design



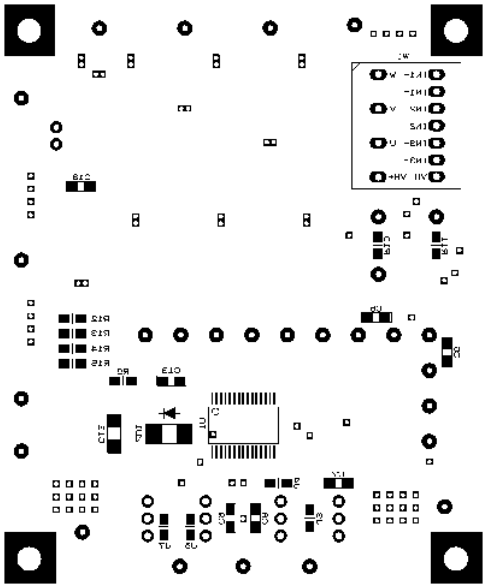
(Top side/ Pattern)



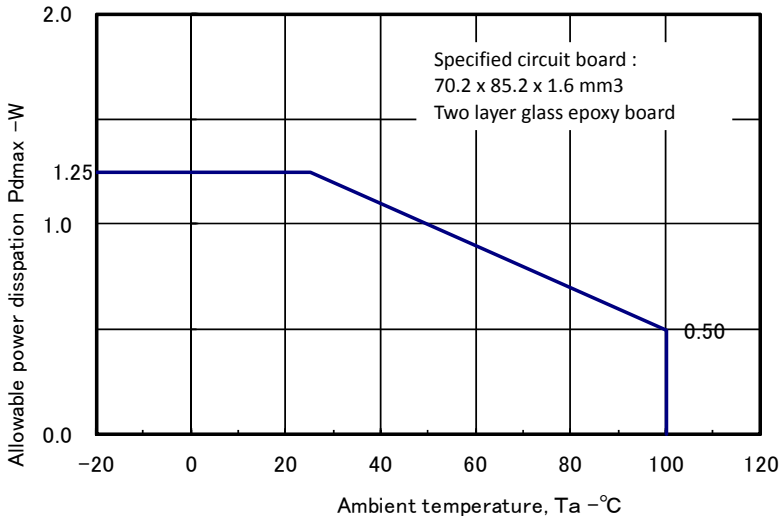
(Back side/ Pattern)



(Top side/ Resist & Silk)



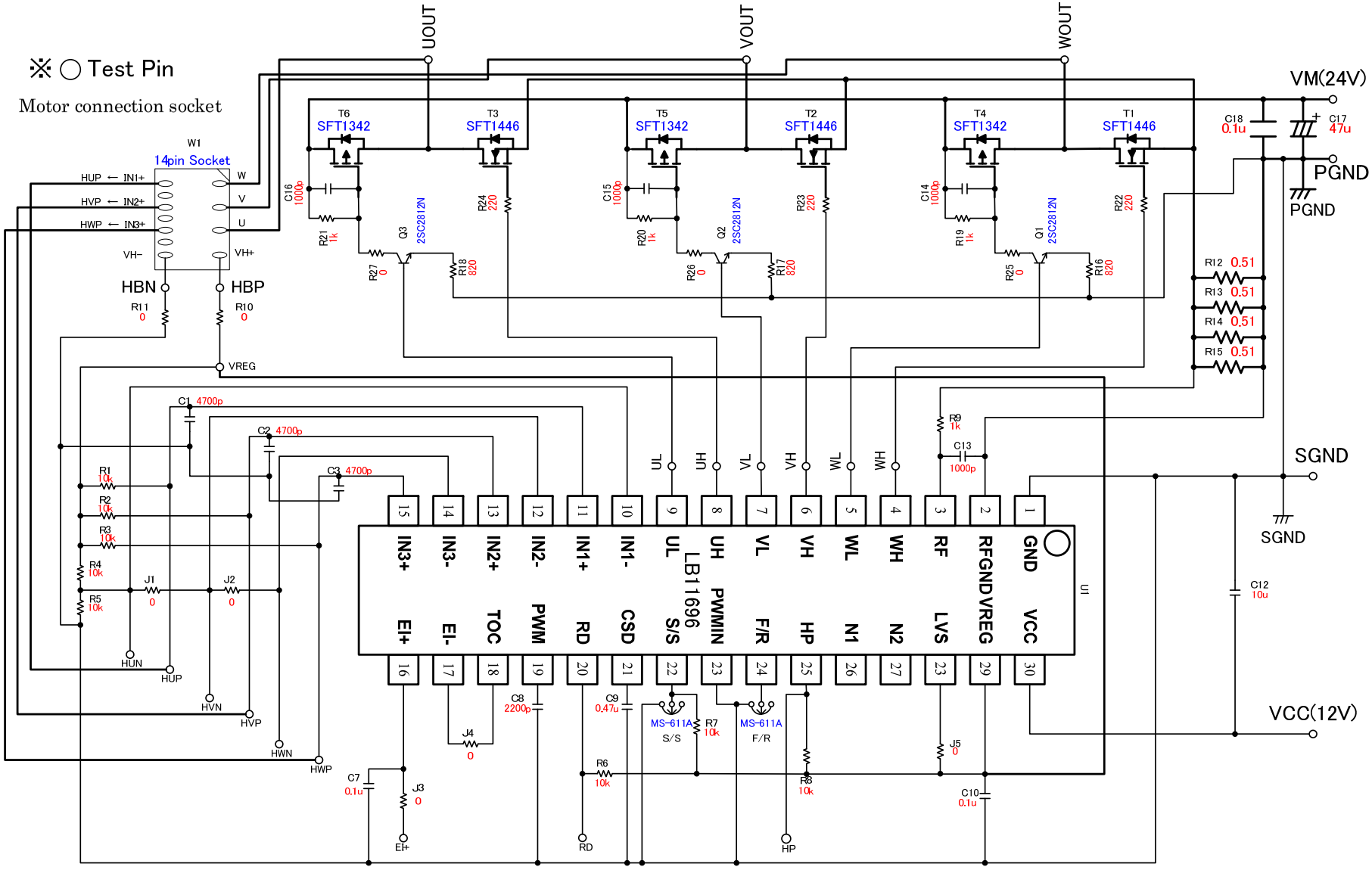
(Back side/ Resist & Silk)



Pdmax - Ta

Application Circuit Example
Evaluation Board Circuit Diagram
(Hall IC Input)

LB11696+SFT Series (VM=24V,VCC=12V,Iomax=2.0A)
Appreciation Board Circuit



Note : The Hall IC to be used must be of open collector or open drain type (no internal pull-up resistor connected to the output).

Application Circuit Example

Bill of Materials for LB11696V Evaluation Board (Hall IC Input)

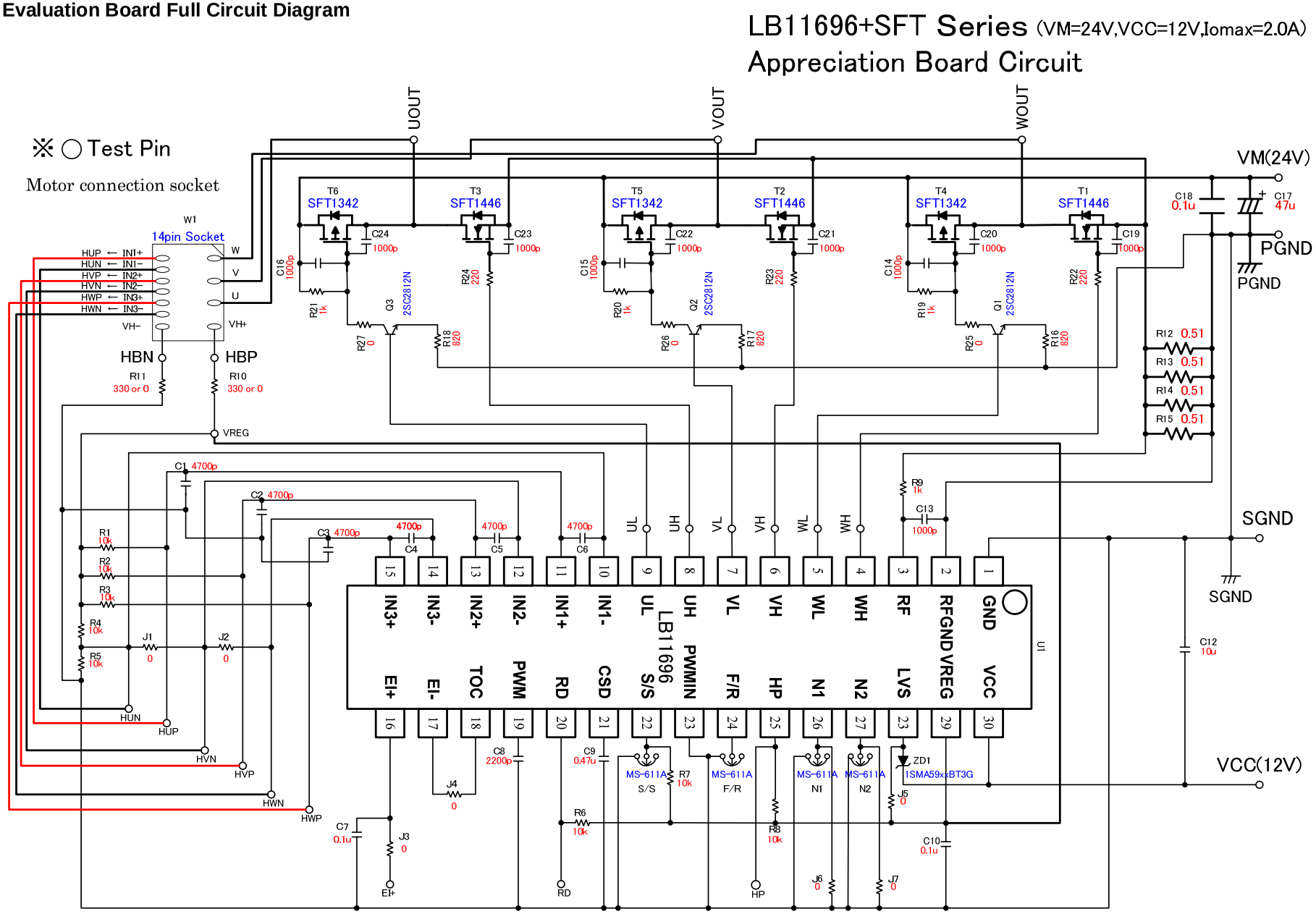
Designator	Quantity	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Lead Free
U1	1	Motor Pre-Driver	-	-	SSOP30 (275mil)	ON Semiconductor	LB11696V	No	yes
Q1	1	WL:NPN Tr. for inverted logic	-	-	CPA	ON Semiconductor	2SC2812N	yes	yes
Q2	1	VL:NPN Tr. for inverted logic	-	-	CPA	ON Semiconductor	2SC2812N	yes	yes
Q3	1	UL:NPN Tr. for inverted logic	-	-	CPA	ON Semiconductor	2SC2812N	yes	yes
T1	1	W:Nch FET for low side driver	-	-	TP-FA	ON Semiconductor	SFT1446	yes	yes
T2	1	V:Nch FET for low side driver	-	-	TP-FA	ON Semiconductor	SFT1446	yes	yes
T3	1	U:Nch FET for low side driver	-	-	TP-FA	ON Semiconductor	SFT1446	yes	yes
T4	1	W:Pch FET for high side driver	-	-	TP-FA	ON Semiconductor	SFT1342	yes	yes
T5	1	V:Pch FET for high side driver	-	-	TP-FA	ON Semiconductor	SFT1342	yes	yes
T6	1	U:Pch FET for high side driver	-	-	TP-FA	ON Semiconductor	SFT1342	yes	yes
SW(S/S)	1	Switch	-	-		MIYAMA	MS-611A-A01	yes	yes
SW(F/R)	1	Switch	-	-		MIYAMA	MS-611A-A01	yes	yes
TP1-TP10	10	Test points	-	-		MAC8	ST-1-3	yes	yes
Socket	1	Motor connection socket	-	-		YAMAICHI	IC-91-1403-G4	yes	yes
R1	1	Hall out(pull up)	10k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	yes	yes
R2	1	Hall out(pull up)	10k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	yes	yes
R3	1	Hall out(pull up)	10k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	yes	yes
R4	1	Input bias	10k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	yes	yes
R5	1	Input bias	10k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	yes	yes
R6	1	RD(pull up)	10k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	yes	yes
R7	1	S/S(pull up)	10k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	yes	yes
R8	1	HP(pull up)	10k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	yes	yes
R9	1	RF (filter)	1k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD102J	yes	yes
R10	1	Hall bias VREG	0 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1J 0ΩJ	yes	yes
R11	1	Hall bias GND	0 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1J 0ΩJ	yes	yes
R12-15	4	RF	0.51 (0.25W)	±5%	2012 (0805Inch)	ROHM	MCR10EZHZJLR51	yes	yes
R16-18	3	NPN Tr. Emitter resistor	820 (0.33W)	±5%	3216 (1206Inch)	ROHM	ESR18EZPJ821	yes	yes
R19-21	3	Pch FET Gate to Source	1k (0.33W)	±5%	3216 (1206Inch)	ROHM	ESR18EZPJ102	yes	yes
R22-24	3	Nch FET Gate resistor	220 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD221J	yes	yes
R25-27	3	Jumper	0 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1J 0ΩJ	yes	yes
J1	1	IN2- bias (Jumper)	0 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1J 0ΩJ	yes	yes

Continued on next page.

Continued from preceding page.

J2	1	IN3- bias (Jumper)	0 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1J 0ΩJ	yes	yes
J3	1	EI+ Jumper	0 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1J 0ΩJ	yes	yes
J4	1	EI-(to TOC)	0 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1J 0ΩJ	yes	yes
J5	1	LVS(to VREG)	0 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1J 0ΩJ	yes	yes
C1	1	IN1+	4700pF /50V	±5%	1608 (0603Inch)	MURATA	GRM188B11H472K	yes	yes
C2	1	IN2+	4700pF /50V	±5%	1608 (0603Inch)	MURATA	GRM188B11H472K	yes	yes
C3	1	IN3+	4700pF /50V	±5%	1608 (0603Inch)	MURATA	GRM188B11H472K	yes	yes
C7	1	EI+ Bypass Capacitor	0.1uF /25V	±10%	1608 (0603Inch)	MURATA	GRM188B11E104K	yes	yes
C8	1	PWM	2200pF /50V	±5%	1608 (0603Inch)	MURATA	GRM1882C1H222J	yes	yes
C9	1	CSD	0.47uF /25V	±10%	1608 (0603Inch)	MURATA	GRM188B31E474KA	yes	yes
C10	1	VREG Bypass capacitor	0.1uF /25V	±10%	1608 (0603Inch)	MURATA	GRM188B11E104K	yes	yes
C12	1	VCC Bypass Capacitor	10uF /25V	±10%	3216 (1206Inch)	MURATA	GRM31CB31E106KA	yes	yes
C13	1	RF (filter)	1000pF /50V	±5%	1608 (0603Inch)	MURATA	GRM1882C1H102J	yes	yes
C14-16	3	Pch FET Gate to Source	1000pF /50V	±5%	1608 (0603Inch)	MURATA	GRM1882C1H102J	yes	yes
C17	1	VM Bypass Capacitor	47uF /100V	±20%	-	PANASONIC	ECA2AHG470	yes	yes
C18	1	VM Bypass Capacitor	0.1uF /25V	±10%	1608 (0603Inch)	MURATA	GRM188B11E104K	yes	yes

Evaluation Board Full Circuit Diagram



Application Circuit Example

Bill of Materials for LB11696V Evaluation Board (All parts)

Designator	Quantity	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Lead Free
U1	1	Motor Pre-Driver	-	-	SSOP30 (275mil)	ON Semiconductor	LB11696V	No	yes
Q1	1	WL:NPN Tr. for inverted logic	-	-	CPA	ON Semiconductor	2SC2812N	yes	yes
Q2	1	VL:NPN Tr. for inverted logic	-	-	CPA	ON Semiconductor	2SC2812N	yes	yes
Q3	1	UL:NPN Tr. for inverted logic	-	-	CPA	ON Semiconductor	2SC2812N	yes	yes
T1	1	W:Nch FET for low side driver	-	-	TP-FA	ON Semiconductor	SFT1446	yes	yes
T2	1	V:Nch FET for low side driver	-	-	TP-FA	ON Semiconductor	SFT1446	yes	yes
T3	1	U:Nch FET for low side driver	-	-	TP-FA	ON Semiconductor	SFT1446	yes	yes
T4	1	W:Pch FET for high side driver	-	-	TP-FA	ON Semiconductor	SFT1342	yes	yes
T5	1	V:Pch FET for high side driver	-	-	TP-FA	ON Semiconductor	SFT1342	yes	yes
T6	1	U:Pch FET for high side driver	-	-	TP-FA	ON Semiconductor	SFT1342	yes	yes
SW(S/S)	1	Switch	-	-		MIYAMA	MS-611A-A01	yes	yes
SW(F/R)	1	Switch	-	-		MIYAMA	MS-611A-A01	yes	yes
SW(N1)	1	Switch	-	-		MIYAMA	MS-611A-A01	yes	yes
SW(N2)	1	Switch	-	-		MIYAMA	MS-611A-A01	yes	yes
TP1-TP25	25	Test points	-	-		MAC8	ST-1-3	yes	yes
ZD1	1	Zener diode for Low Voltage Shutdown	5.1V	-	SMA	ON Semiconductor	1SMA5918BT3G	yes	yes
Socket	1	Motor connection socket	-	-		YAMAICHI	IC-91-1403-G4	yes	yes
R1	1	Hall out(pull up)	10k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	yes	yes
R2	1	Hall out(pull up)	10k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	yes	yes
R3	1	Hall out(pull up)	10k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	yes	yes
R4	1	Input bias	10k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	yes	yes
R5	1	Input bias	10k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	yes	yes
R6	1	RD(pull up)	10k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	yes	yes
R7	1	S/S(pull up)	10k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	yes	yes
R8	1	HP(pull up)	10k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	yes	yes
R9	1	RF (filter)	1k (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD102J	yes	yes
R10	1	Hall bias VREG	330 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD331J	yes	yes
R11	1	Hall bias GND	330 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD331J	yes	yes
R12-15	4	RF	0.51 (0.25W)	±5%	2012 (0805Inch)	ROHM	MCR10EZHZJLR51	yes	yes
R16-18	3	NPN Tr. Emitter resistor	820 (0.33W)	±5%	3216 (1206Inch)	ROHM	ESR18EZPJ821	yes	yes
R19-21	3	Pch FET Gate to Source	1k (0.33W)	±5%	3216 (1206Inch)	ROHM	ESR18EZPJ102	yes	yes
R22-24	3	Nch FET Gate resistor	220 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD221J	yes	yes

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R25-27	3	Jumper	0 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1J 0ΩJ	yes	yes
J1	1	IN2- bias (Jumper)	0 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1J 0ΩJ	yes	yes
J2	1	IN3- bias (Jumper)	0 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1J 0ΩJ	yes	yes
J3	1	EI+ Jumper	0 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1J 0ΩJ	yes	yes
J4	1	EI-(to TOC)	0 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1J 0ΩJ	yes	yes
J5	1	LVS(to VREG)	0 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1J 0ΩJ	yes	yes
J6	1	N1(to GND)	0 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1J 0ΩJ	yes	yes
J7	1	N2(to GND)	0 (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1J 0ΩJ	yes	yes
C1	1	IN1+	4700pF /50V	±5%	1608 (0603Inch)	MURATA	GRM188B11H472K	yes	yes
C2	1	IN2+	4700pF /50V	±5%	1608 (0603Inch)	MURATA	GRM188B11H472K	yes	yes
C3	1	IN3+	4700pF /50V	±5%	1608 (0603Inch)	MURATA	GRM188B11H472K	yes	yes
C4	1	IN3+/ -	4700pF /50V	±5%	1608 (0603Inch)	MURATA	GRM188B11H472K	yes	yes
C5	1	IN2+/ -	4700pF /50V	±5%	1608 (0603Inch)	MURATA	GRM188B11H472K	yes	yes
C6	1	IN1+/ -	4700pF /50V	±5%	1608 (0603Inch)	MURATA	GRM188B11H472K	yes	yes
C7	1	EI+ Bypass Capacitor	0.1uF /25V	±10%	1608 (0603Inch)	MURATA	GRM188B11E104K	yes	yes
C8	1	PWM	2200pF /50V	±5%	1608 (0603Inch)	MURATA	GRM1882C1H222J	yes	yes
C9	1	CSD	0.47uF /25V	±10%	1608 (0603Inch)	MURATA	GRM188B31E474KA	yes	yes
C10	1	VREG Bypass capacitor	0.1uF /25V	±10%	1608 (0603Inch)	MURATA	GRM188B11E104K	yes	yes
C12	1	VCC Bypass Capacitor	10uF /25V	±10%	3216 (1206Inch)	MURATA	GRM31CB31E106KA	yes	yes
C13	1	RF (filter)	1000pF /50V	±5%	1608 (0603Inch)	MURATA	GRM1882C1H102J	yes	yes
C14-16	1	Pch FET Gate to Source	1000pF /50V	±5%	1608 (0603Inch)	MURATA	GRM1882C1H102J	yes	yes
C17	1	VM Bypass Capacitor	47uF /100V	±20%	-	PANASONIC	ECA2AHG470	yes	yes
C18	1	VM Bypass Capacitor	0.1uF /25V	±10%	1608 (0603Inch)	MURATA	GRM188B11E104K	yes	yes
C19	1	Nch FET Gate to Source	1000pF /50V	±5%	1608 (0603Inch)	MURATA	GRM1882C1H102J	yes	yes
C20	1	Pch FET Gate to Drain	1000pF /50V	±5%	1608 (0603Inch)	MURATA	GRM1882C1H102J	yes	yes
C21	1	Nch FET Gate to Source	1000pF /50V	±5%	1608 (0603Inch)	MURATA	GRM1882C1H102J	yes	yes
C22	1	Pch FET Gate to Drain	1000pF /50V	±5%	1608 (0603Inch)	MURATA	GRM1882C1H102J	yes	yes
C23	1	Nch FET Gate to Source	1000pF /50V	±5%	1608 (0603Inch)	MURATA	GRM1882C1H102J	yes	yes
C24	1	Pch FET Gate to Drain	1000pF /50V	±5%	1608 (0603Inch)	MURATA	GRM1882C1H102J	yes	yes