Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 µA V_{GS} = 0 V, I_D = 250 µA	Q1 Q2	–20 20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C I_D = 250 µA, Referenced to 25°C	Q1 Q2		–14 12		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –16 V, V_{GS} = 0 V V_{DS} = 16 V, V_{GS} = 0 V	Q1 Q2			–1 1	µA
I_{GSS}	Gate-Body Leakage	V_{GS} = ±12 V, V_{DS} = 0 V V_{GS} = ±12 V, V_{DS} = 0 V	Q1 Q2			±100 ±100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 µA V_{DS} = V_{GS}, I_D = 250 µA	Q1 Q2	–0.6 0.6	–1.0 1.0	–1.5 1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C I_D = 250 µA, Referenced to 25°C	Q1 Q2		3 –3		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = –4.5 V, I_D = –4.2 A V_{GS} = –2.5 V, I_D = –3.4 A V_{GS} = –4.5 V, I_D = –4.2 A, T_J =125°C	Q1		45 65 58	55 82 73	mΩ
		V_{GS} = 4.5 V, I_D = 5.9 A V_{GS} = 2.5 V, I_D = 4.9 A V_{GS} = 4.5 V, I_D = 5.9 A, T_J = 125°C	Q2		23 33 31	27 39 39	
g_{FS}	Forward Transconductance	V_{DS} = –5 V, I_D = – 4.2 A V_{DS} = 5 V, I_D = 5.9 A	Q1 Q2		13 23		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q1: V_{DS} = –10 V, V_{GS} = 0 V, f = 1.0 MHz Q2: V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	Q1 Q2		753 677		pF
C_{oss}	Output Capacitance		Q1 Q2		163 171		pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		83 91		pF
R_G	Gate Resistance	V_{GS} = 15mV, f = 1.0 MHz	Q1		8		Ω
			Q2		2.2		
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	Q1: V_{DD} = –10 V, I_D = –1 A, V_{GS} = –4.5 V, R_{GEN} = 6 Ω Q2: V_{DD} = 10 V, I_D = 1 A, V_{GS} = 4.5V, R_{GEN} = 6 Ω	Q1 Q2		13 11	23 20	ns
t_r	Turn-On Rise Time		Q1 Q2		8 16	16 29	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		26 18	42 32	ns
t_f	Turn-Off Fall Time		Q1 Q2		14 7	52 14	ns
Q_g	Total Gate Charge	Q1: V_{DS} = –10 V, I_D = –4.2 A, V_{GS} = –4.5V Q2: V_{DS} = 10 V, I_D = 5.9 A, V_{GS} = 4.5 V	Q1 Q2		7 6	10 8	nC
Q_{gs}	Gate-Source Charge		Q1 Q2		1.6 1.5		nC
Q_{gd}	Gate-Drain Charge		Q1 Q2		1.9 1.8		nC

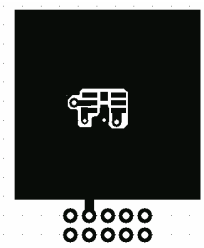
Electrical Characteristics (continued)

T_A = 25°C unless otherwise noted

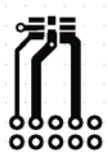
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q1 Q2			–1.3 1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –1.3 A (Note 2) V_{GS} = 0 V, I_S = 1.3 A (Note 2)	Q1 Q2		–0.8 0.7	–1.2 1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = – 4.2A,d_{IF}/d_t = 100 A/µs I_F = 5.9A, d_{IF}/d_t = 100 A/µs	Q1 Q2		17 15		nS
Q_{rr}	Diode Reverse Recovery Charge	I_F = – 4.2A,d_{IF}/d_t = 100 A/µs I_F = 5.9A, d_{IF}/d_t = 100 A/µs	Q1 Q2		6 4		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 68°C/W when mounted on a 1in^2 pad of 2 oz copper (Single Operation).



b) 102°C/W when mounted on a minimum pad of 2 oz copper (Single Operation).

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics : Q1

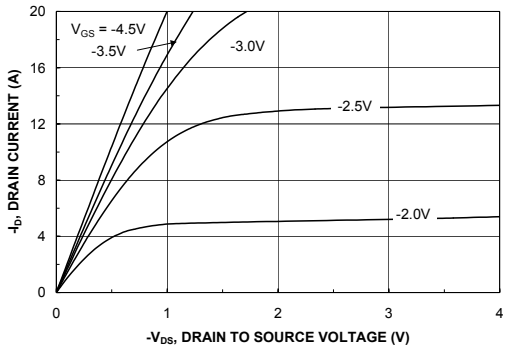


Figure 1. On-Region Characteristics.

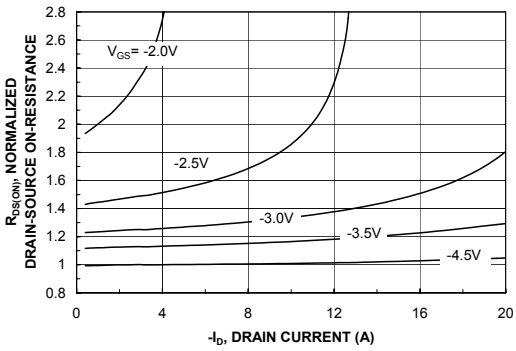


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

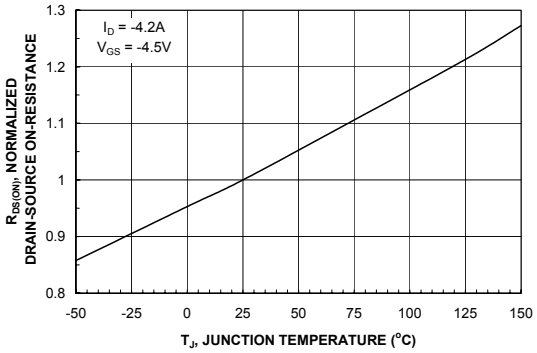


Figure 3. On-Resistance Variation with Temperature.

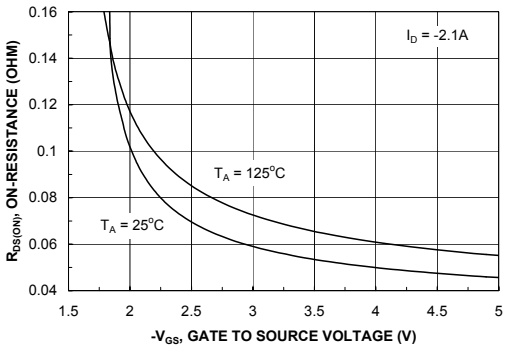


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

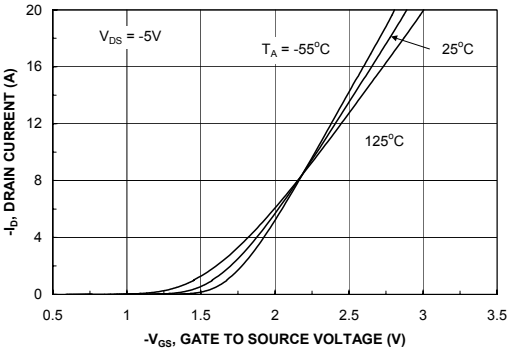


Figure 5. Transfer Characteristics.

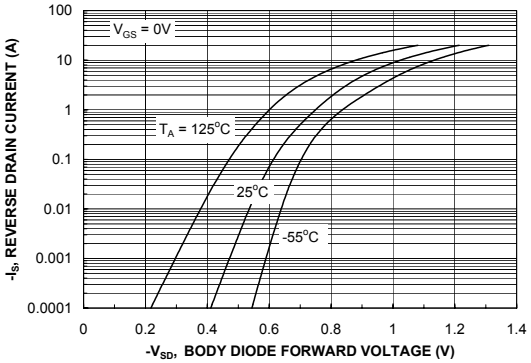


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics : Q1

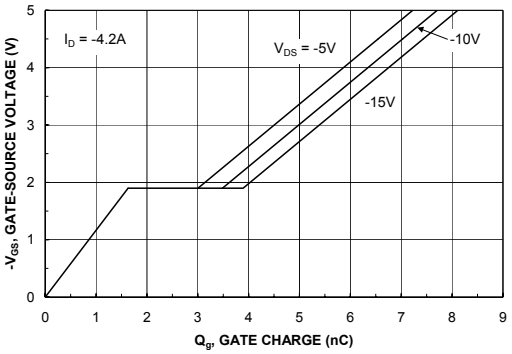


Figure 7. Gate Charge Characteristics.

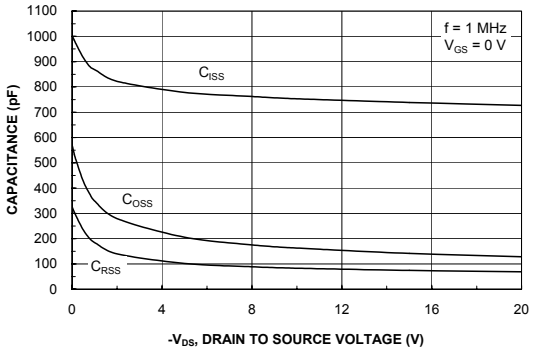


Figure 8. Capacitance Characteristics.

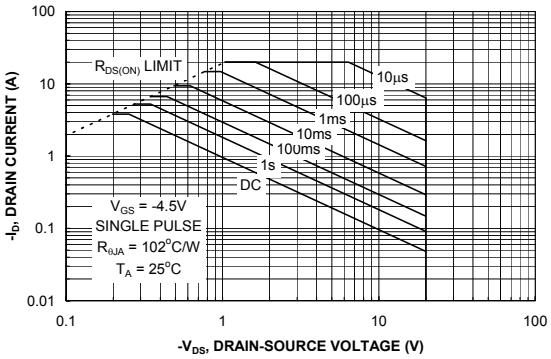


Figure 9. Maximum Safe Operating Area.

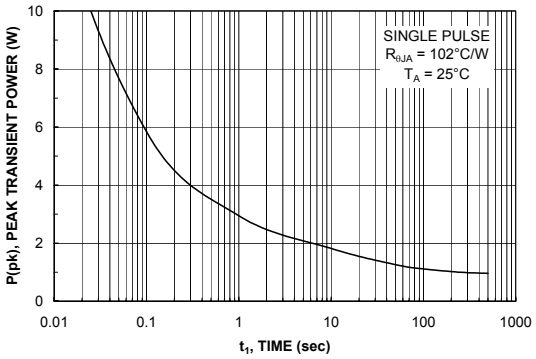


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics : Q2

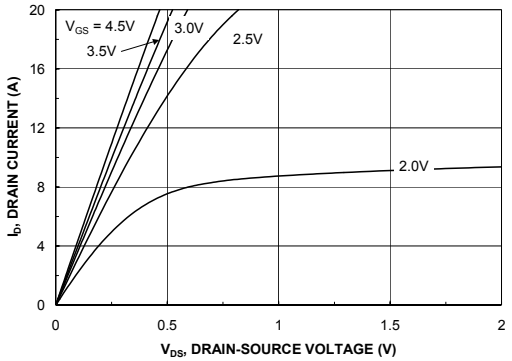


Figure 11. On-Region Characteristics.

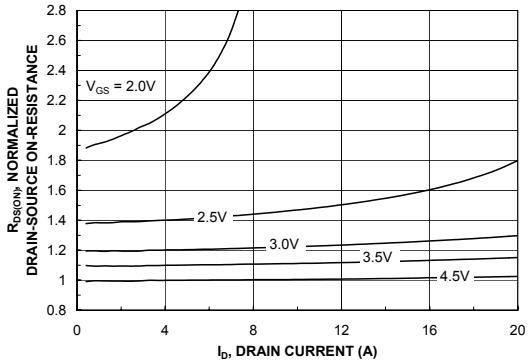


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

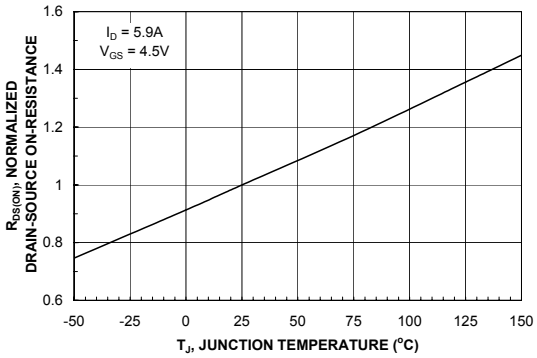


Figure 13. On-Resistance Variation with Temperature.

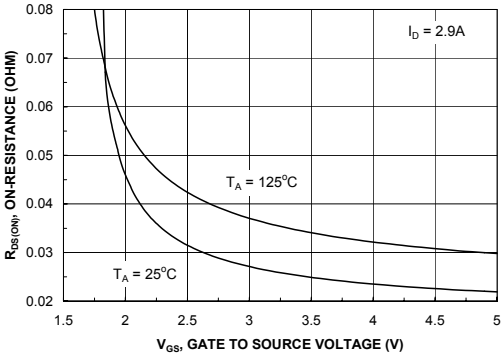


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

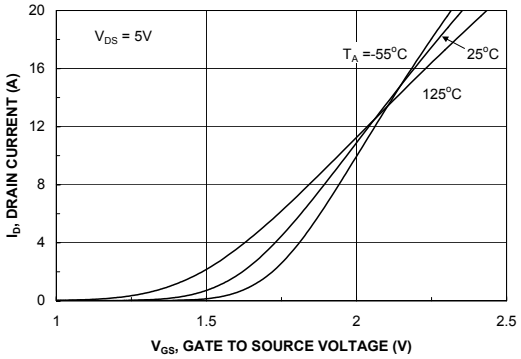


Figure 15. Transfer Characteristics.

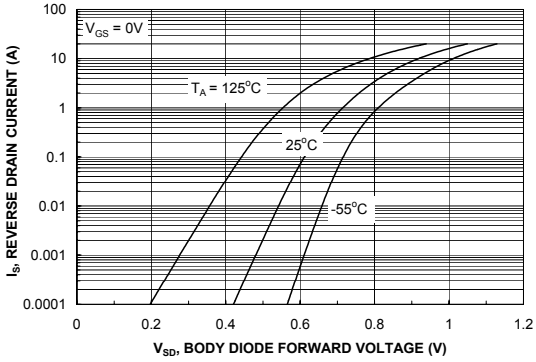


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics : Q2

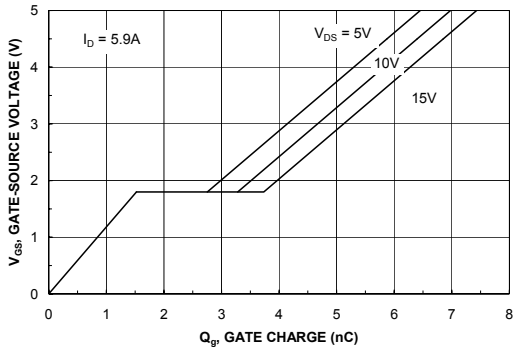


Figure 17. Gate Charge Characteristics.

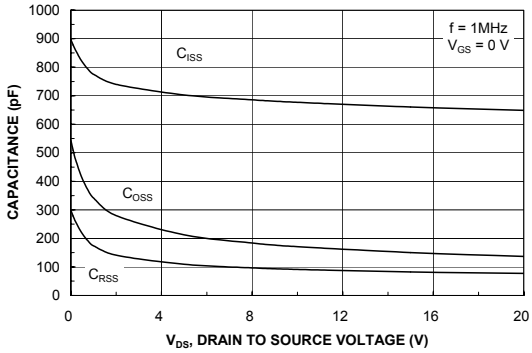


Figure 18. Capacitance Characteristics.

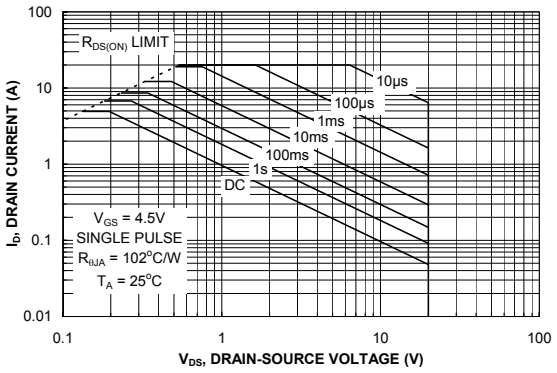


Figure 19. Maximum Safe Operating Area.

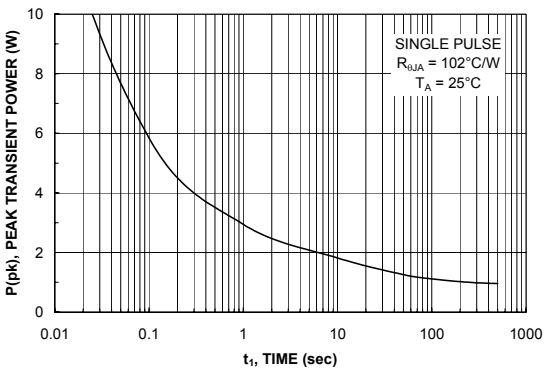


Figure 20. Single Pulse Maximum Power Dissipation.

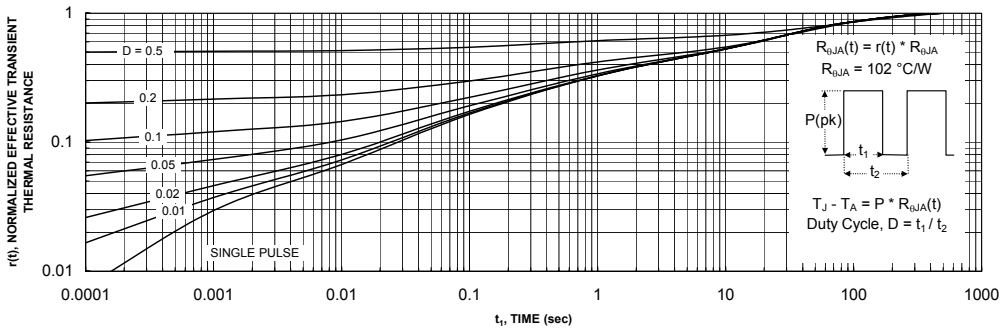
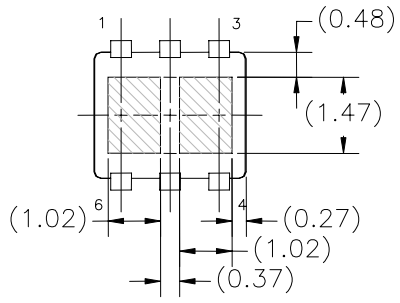


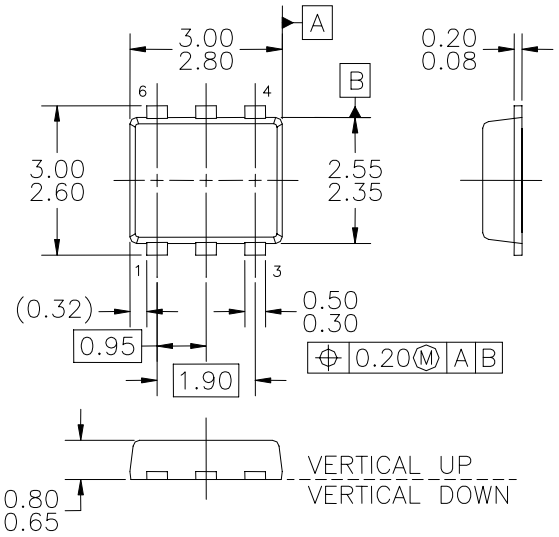
Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

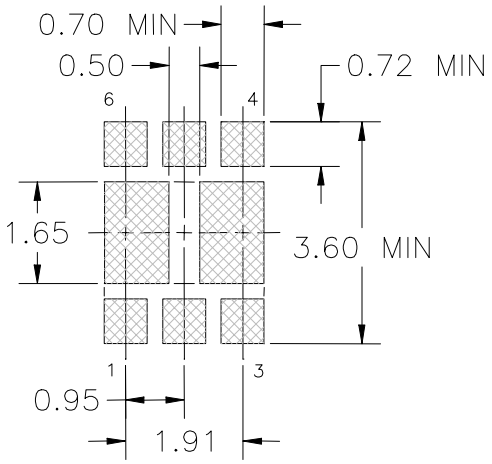
Dimensional Outline and Pad Layout



Bottom View



Top View



Recommended Landing Pattern

For Standard Dual Configuration

NOTES: UNLESS OTHERWISE SPECIFIED

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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