

FAN7083_GF085

High Side Gate Driver with Reset

Features

- Qualified to AEC Q100
- Floating channel designed for bootstrap operation up fully operational to + 600V
- Tolerance to negative transient voltage on VS pin
- dv/dt immune.
- Gate drive supply range from 10V to 20V
- Under-voltage lockout
- CMOS Schmitt-triggered inputs with pull-down
- High side output in phase with input
- RESET input is 3.3V and 5V logic compatible

Typical Applications

- Diesel and gasoline injectors/valves
- MOSFET-and IGBT high side driver applications

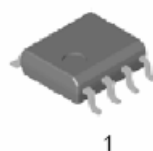


For Fairchild's definition of "green" Eco Status, please visit:
http://www.fairchildsemi.com/company/green/rohs_green.html

Description

The FAN7083_GF085 is a high-side gate drive IC with reset input. It is designed for high voltage and high speed driving of MOSFET or IGBT, which operates up to 600V. Fairchild's high-voltage process and common-mode noise cancellation technique provide stable operation in the high side driver under high-dv/dt noise circumstances. An advanced level-shift circuit allows high-side gate driver operation up to VS=-5V (typical) at VBS=15V. Logic input is compatible with standard CMOS outputs. The UVLO circuits prevent from malfunction when VCC and VBS are lower than the specified threshold voltage. It is available with space saving SOIC-8 Package. Minimum source and sink current capability of output driver is 200mA and 400mA respectively, which is suitable for magnetic-and piezo type injectors and general MOSFET/IGBT based high side driver applications.

SOIC-8

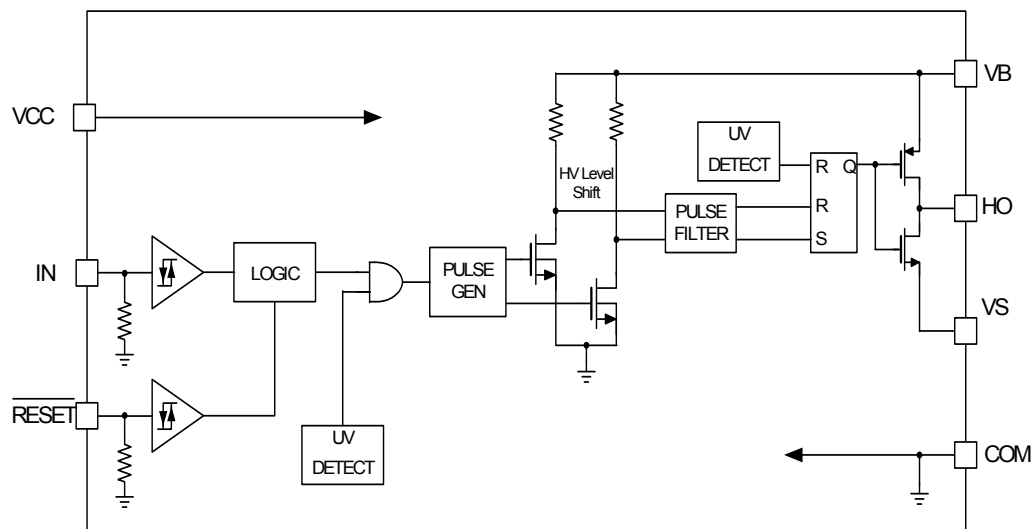


Ordering Information

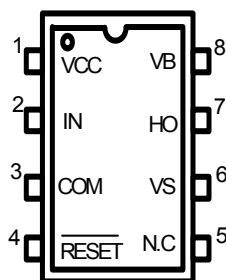
| Device | Package | Operating Temp. |
|-----------------|---------|-----------------|
| FAN7083M_GF085 | SOIC-8 | -40 °C ~ 125 °C |
| FAN7083MX_GF085 | SOIC-8 | -40 °C ~ 125 °C |

X : Tape & Reel type

Block Diagrams



Pin Assignments



Pin Definitions

| Pin Number | Pin Name | I/O | Pin Function Description |
|------------|----------|-----|---|
| 1 | VCC | P | Driver supply voltage |
| 2 | IN | I | Logic input for high side gate drive output, in phase with HO |
| 3 | COM | P | Ground |
| 4 | RESET | I | Reset input |
| 5 | NC | - | NC |
| 6 | VS | P | High side floating offset for MOSFET Source connection |
| 7 | HO | A | High side drive output for MOSFET Gate connection |
| 8 | VB | P | Driver output stage supply |

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM.

| Parameter | Symbol | Min. | Max. | Unit |
|---|--------|--------|---------|------|
| High side floating supply offset voltage | VS | VB-25 | VB+0.3 | V |
| High side floating supply voltage | VB | -0.3 | 625 | V |
| High side floating output voltage | VHO | Vs-0.3 | VB+0.3 | V |
| Supply voltage | VCC | -0.3 | 25 | V |
| Input voltage for IN | VIN | -0.3 | VCC+0.3 | V |
| Input voltage for RESET | VRESET | -0.3 | VCC+0.3 | V |
| Power Dissipation ¹⁾ | Pd | | 0.625 | W |
| Thermal resistance, junction to ambient ¹⁾ | Rthja | | 200 | °C/W |
| Electrostatic discharge voltage (Human Body Model) | VESD | 1K | | V |
| Charge device model | VCDM | 500 | | V |
| Junction Temperature | Tj | | 150 | °C |
| Storage Temperature | Ts | -55 | 150 | °C |

Note: 1) The thermal resistance and power dissipation rating are measured bellow conditions;

JESD51-2: Integrated Circuit Thermal Test Method Environmental Conditions - Natural convection(StillAir)

JESD51-3 : Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Package

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. -40°C ≤ Ta ≤ 125°C

| Parameter | Symbol | Min. | Max. | Unit |
|---|--------------------|---|---------|------|
| High side floating supply voltage -10V Transient 0.2us | VB | Vs + 10 | Vs + 20 | V |
| High side floating supply offset voltage(DC) | VS | -4 (@VBS ≥ 10V) -5 (@VBS ≥ 11.5V) | 600 | V |
| High side floating supply offset voltage(Transient) | VS | -25 (~200ns) -20(200ns~240ns) -7(240ns~400ns) | 600 | V |
| High side floating output voltage | VHO | Vs | VB | V |
| Allowable offset voltage Slew Rate ¹⁾ | dv/dt | - | 50 | V/ns |
| Supply voltage | VCC | 10 | 20 | V |
| Input voltage for IN | VIN | 0 | Vcc | V |
| Input voltage for RESET | VRESET | 0 | Vcc | V |
| Switching Frequency ²⁾ | Fs | | 200 | KHz |
| Minimum Pulse Width ⁽³⁾ | T _{pulse} | 85 | - | ns |
| Ambient Temperature | Ta | -40 | 125 | °C |

Note : 1) Guaranteed by design.

2) Duty = 0.5

3) Guaranteed by design. Refer to Figure 4a, 4b and 4c on Page 9.

Statics Electrical Characteristics

Unless otherwise specified, $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$, $V_{CC} = 15\text{V}$, $V_{BS} = 15\text{V}$, $V_{RESET} = 5\text{V}$, $V_S = 0\text{V}$, $R_L = 50\Omega$, $C_L = 2.5\text{nF}$.

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|--|------------------|--|------------|------|----------|----------|
| Vcc and VBS supply Characteristics | | | | | | |
| VCC and VBS supply under voltage positive going threshold | VCCUV+ VBSUV+ | - | - | 9.0 | 9.8 | V |
| VCC and VBS supply under voltage negative going threshold | VCCUV- VBSUV- | - | 7.4 | 8.4 | - | V |
| VCC and VBS supply under voltage hysteresis | VCCUVH VBSUVH | - | 0.2 | 0.6 | - | V |
| Under voltage lockout response time | tduvcc tduvbs | VCC: 10V-->7.3V or 7.3V-->10V VBS: 10V-->7.3V or 7.3V-->10V | 0.5 0.5 | | 20 20 | us us |
| Offset supply leakage current | ILK | VB=VS=600V | - | - | 50 | uA |
| Quiescent VBS supply current | IQBS | VIN=0, VRESET=5V | - | 50 | 100 | uA |
| | | | | | | |
| Quiescent Vcc supply current | IQCC1 | VIN=VRESET=0 | - | 65 | 140 | uA |
| Quiescent Vcc supply current | IQCC2 | VIN=15V, VRESET=0 | - | 75 | 160 | uA |
| Input Characteristics | | | | | | |
| High logic level input voltage for IN | VIH | - | 0.63Vcc | | - | V |
| Low logic level input voltage for IN | VIL | - | - | - | 0.4Vcc | V |
| High logic level input current for IN | IIN+ | VIN=15V | - | 15 | 50 | uA |
| Low logic level input bias current for IN | IIN- | VIN=0 | - | 0 | 1 | uA |
| High logic level input voltage for $\overline{\text{RESET}}$ | VRIH | - | 3.0 | - | - | V |
| Low logic level input voltage for $\overline{\text{RESET}}$ | VRIL | - | - | - | 1.4 | V |
| High logic level input current for $\overline{\text{RESET}}$ | IRIN+ | VRESET=5V | - | 5 | 30 | uA |
| Low logic level input bias current for $\overline{\text{RESET}}$ | IRIN- | VRESET=0 | - | 0 | 1 | uA |
| Output characteristics | | | | | | |
| High level output voltage, VBIAS- VO | VOH | IO=0 | - | - | 0.1 | V |
| Low level output voltage, VO | VOL | IO=0 | - | - | 0.1 | V |
| Peak output source current | IO1+ | - | 200 | - | - | mA |
| Peak output sink current | IO1- | - | 400 | - | - | mA |
| Equivalent output resistance | ROP | | | 54 | 75 | Ω |
| | RON | | | 24 | 38 | Ω |

Note: The input parameter are referenced to COM. The VO and IO parameters are referenced to COM.

Dynamic Electrical Characteristics

Unless otherwise specified, $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$, $V_{CC} = 15\text{V}$, $V_{BS} = 15\text{V}$, $V_{RESET} = 5\text{V}$, $V_S = 0\text{V}$, $R_L = 50\Omega$, $C_L = 2.5\text{nF}$.

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|--|----------------------|---|------|------|------|------|
| IN-to-output turn-on propagation delay | t _{plh} | 50% input level to 10% output level, V _S = 0V | - | 115 | 250 | ns |
| IN-to-output turn-off propagation delay | t _{phl} | 50% input level to 90% output level V _S = 0V | - | 90 | 200 | ns |
| RESET-to-output turn-off propagation delay | t _{phl_res} | 50% input level to 90% output level | - | 90 | 200 | ns |
| RESET-to-output turn-on propagation delay | t _{plh_res} | 50% input level to 10% output level | - | 115 | 250 | ns |
| Output rising time | t _{r1} | T _j =25°C, V _{BS} =15V | - | 200 | 400 | ns |
| | t _{r2} | | - | - | 500 | ns |
| Output falling time | t _{f1} | T _j =25°C, V _{BS} =15V | - | 25 | 200 | ns |
| | t _{f2} | | - | - | 400 | ns |

Application Information

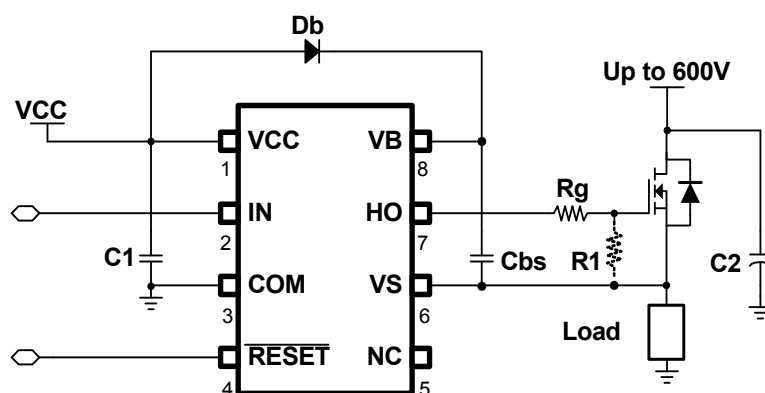
1. Relationship in input/output and supplies

| VCC | VBS | RESET | IN | HO |
|------------|------------|-------|------|-----|
| < VCCUVLO- | X | X | X | OFF |
| X | < VBSUVLO- | X | X | OFF |
| X | X | LOW | X | OFF |
| X | X | X | LOW | OFF |
| > VCCUVLO+ | > VBSUVLO+ | HIGH | HIGH | ON |

Notes:

X means independent from signal

Typical Application Circuit



Typical Waveforms

1. Input/Output Timing

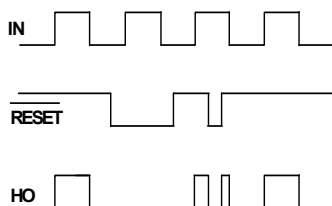


Figure 1a. Input/output Timing Diagram

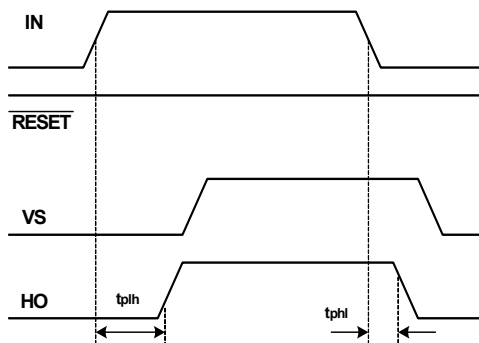


Figure 1b. Input(IN)/output Timing Diagram

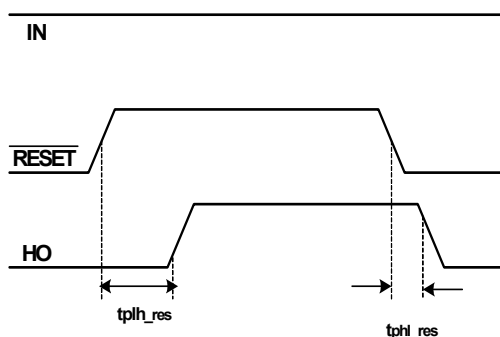


Figure 1c. Input(RESET)/output Timing Diagram

2. Output(HO) Switching Timing

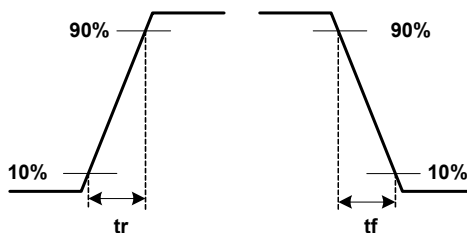


Figure 2. Switching Time Waveform Definitions

3.VB Drop Voltage Diagram

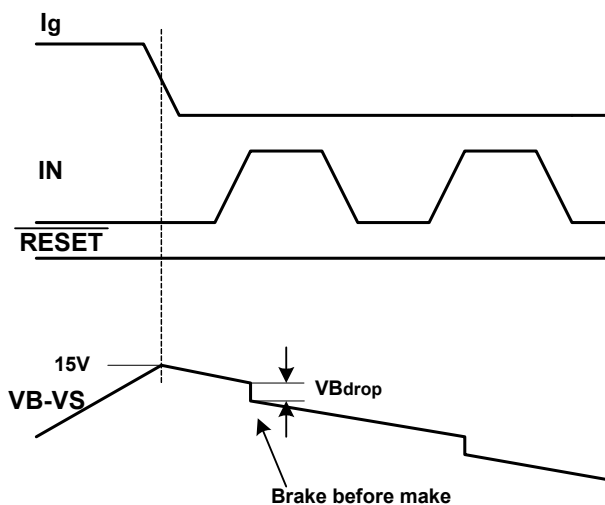


Figure 3a. VB Drop Voltage Diagram

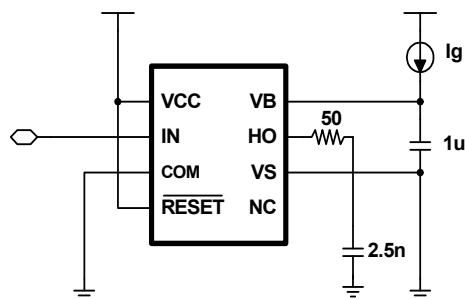


Figure3b. VB Drop Voltage Test Circuit

4.Recommendation Min. Short Pulse Width

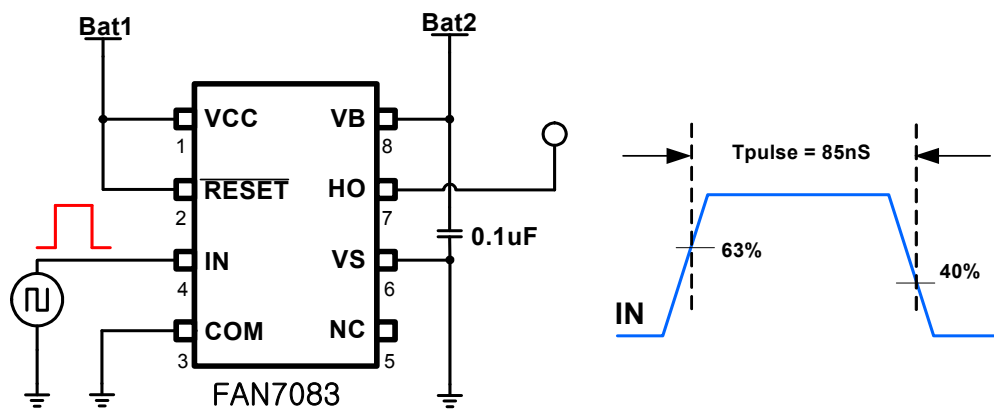


Figure 4a.Short Pulse Width Test Circuit and Pulse Width Waveform

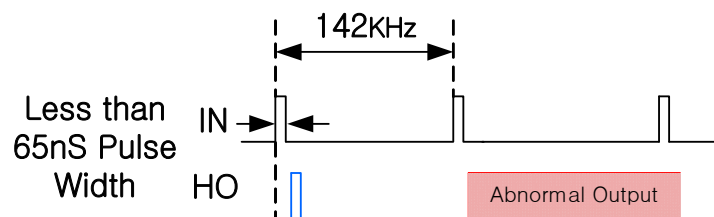


Figure 4b. Abnormal Output Waveform with short pulse width

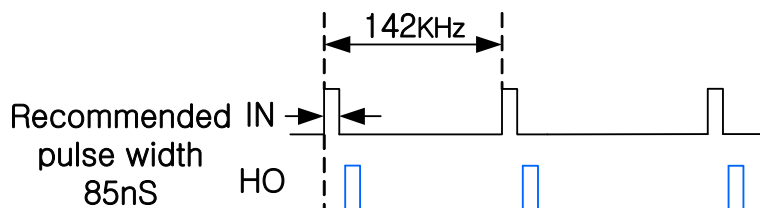


Figure 4c. Recommendation of pulse width Output Waveform

Performance Graphs

This performance graphs based on ambient temperature -40°C ~ 125°C

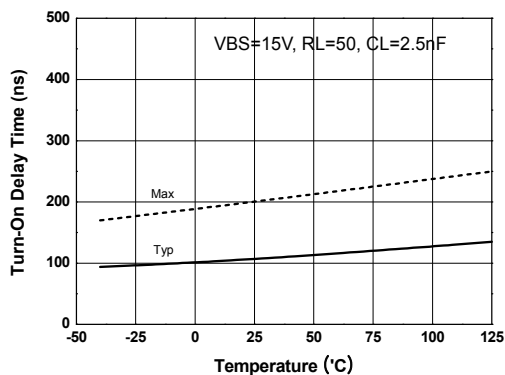


Figure 5a. Turn-On Delay Time vs Temperature

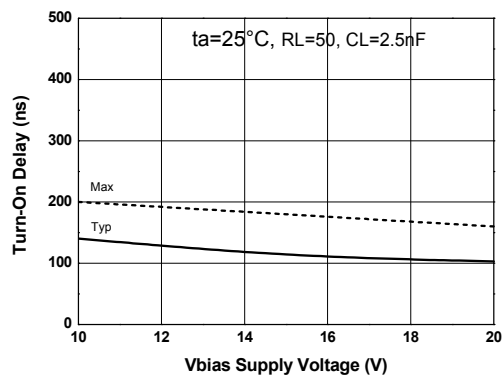


Figure 5b. Turn-On Delay Time vs VBS Supply Voltage

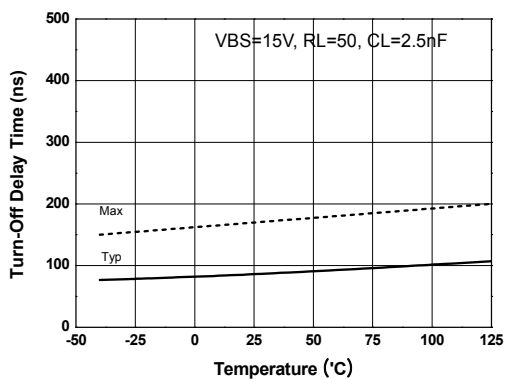


Figure 6a. Turn-Off Delay Time vs Temperature

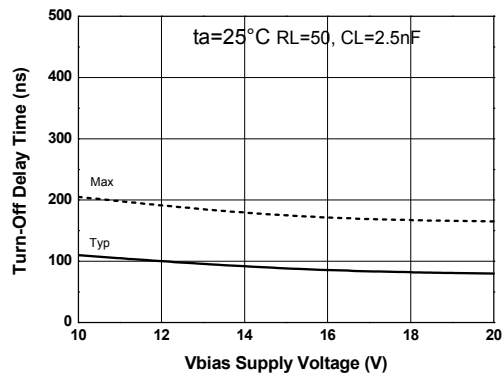


Figure 6b. Turn-Off Delay Time vs VBS Supply Voltage

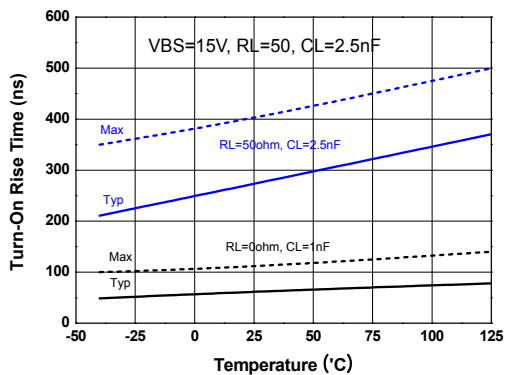


Figure 7a. Turn-On Rise Time vs Temperature

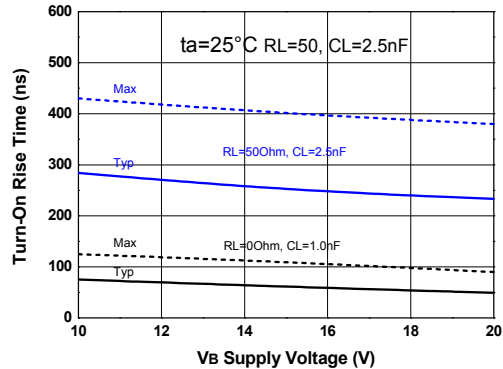


Figure 7b. Turn-On Rise Time vs VBS Supply Voltage

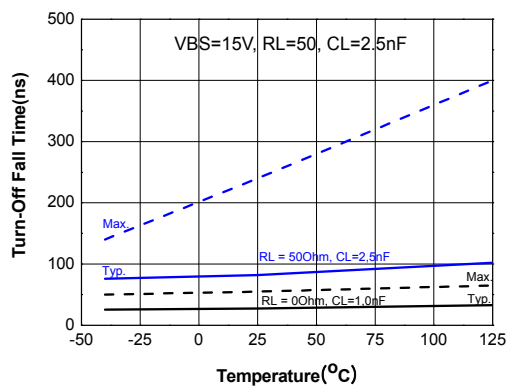


Figure 8a. Turn-Off Falling Time vs Temperature

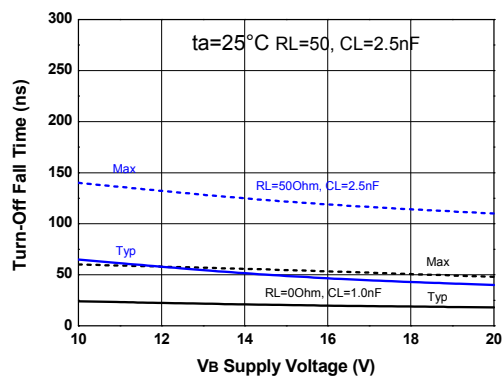


Figure 8b. Turn-Off Falling Time vs VBS Supply Voltage

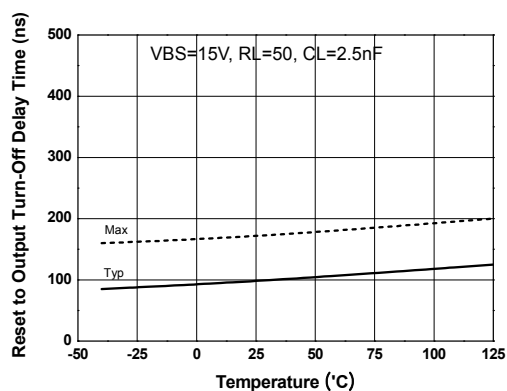


Figure 9a. RESET to output Turn-Off Delay Time vs Temperature

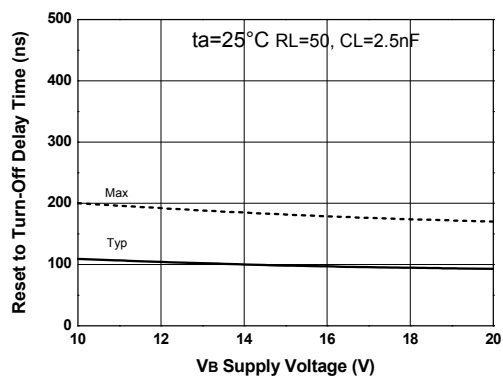


Figure 9b. RESET to output Turn-Off Delay Time vs VBS Supply

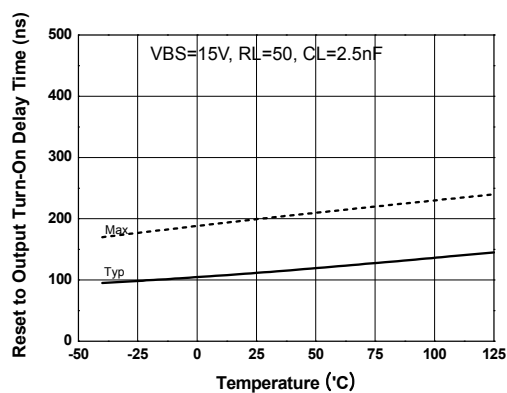


Figure 10a. RESET to output Turn-On Delay Time vs Temperature

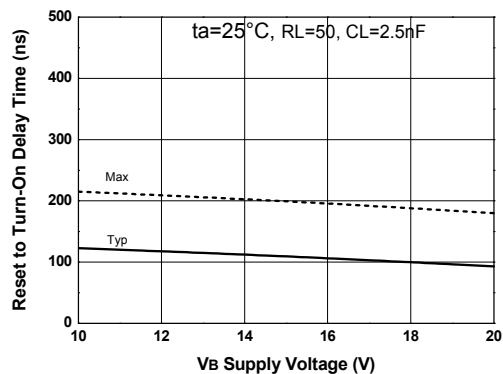


Figure 10b. RESET to output Turn-On Delay Time vs VBS Supply

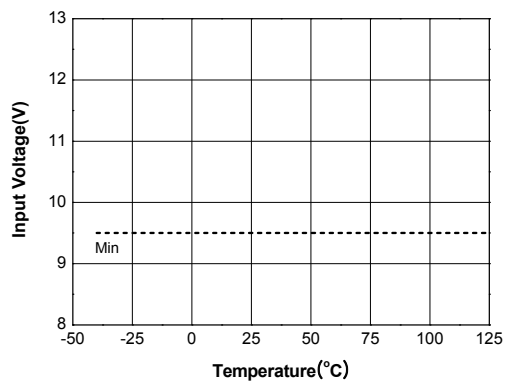


Figure 11a. Logic "1" IN Threshold vs Temperature

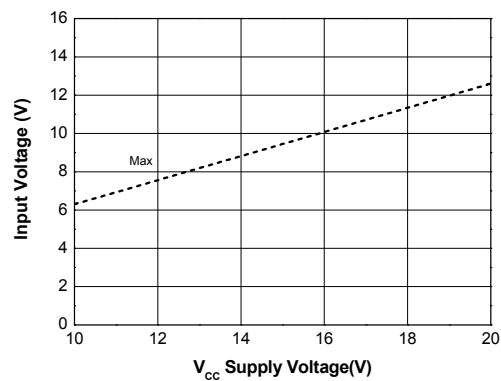


Figure 11b. Logic "1" IN Threshold vs VCC Supply Voltage

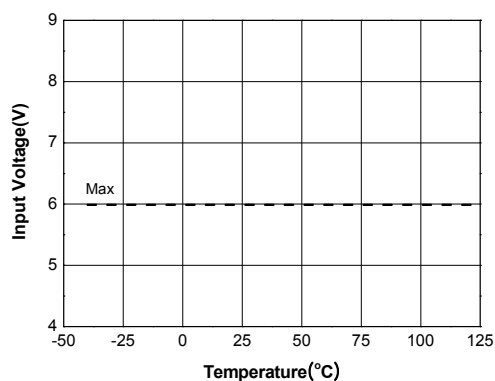


Figure 12a. Logic "0" IN Threshold vs Temperature

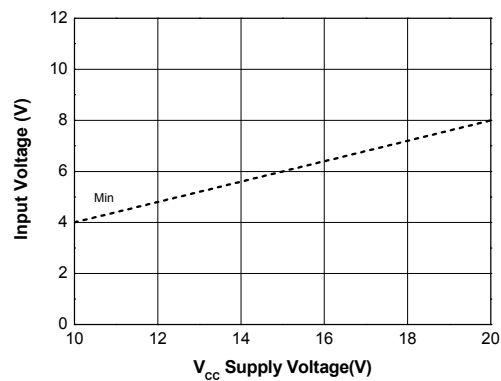


Figure 12b. Logic "0" IN Threshold vs VCC Supply Voltage

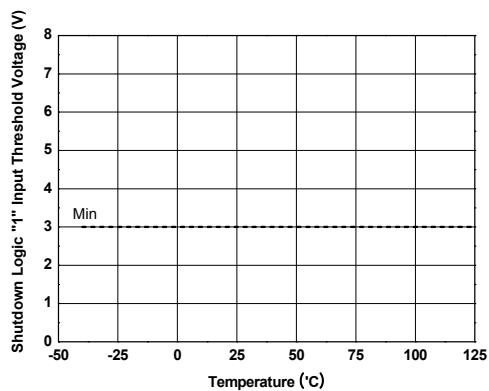


Figure 13a. Logic "1" Reset Threshold vs Temperature

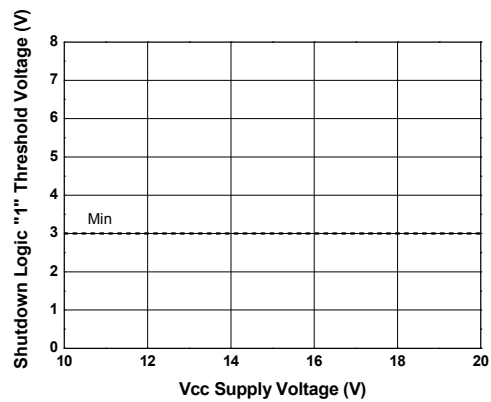


Figure 13b. Logic "1" Reset Threshold vs VCC Supply Voltage

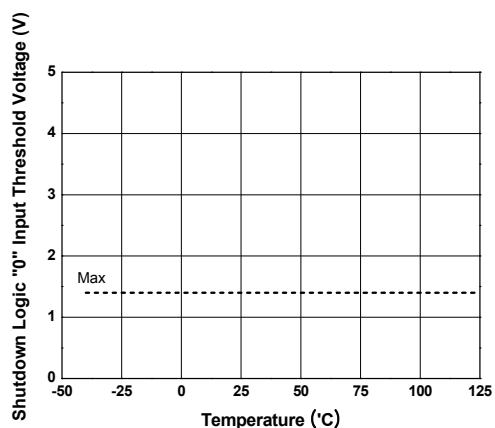


Figure 14a. Logic "0" Reset Threshold vs Temperature

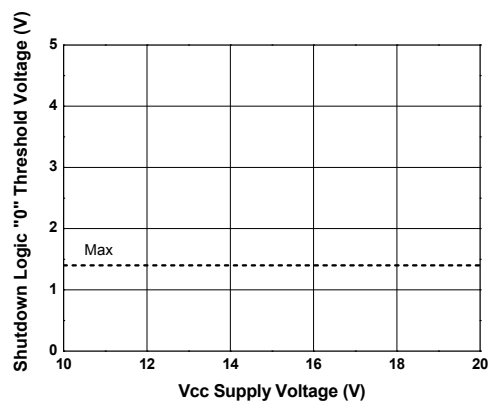


Figure 14b. Logic "0" Reset Threshold vs VCC Supply Voltage

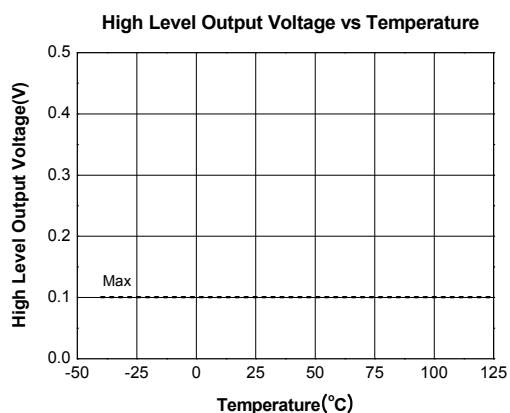


Figure 15a. High Level Output vs Temperature

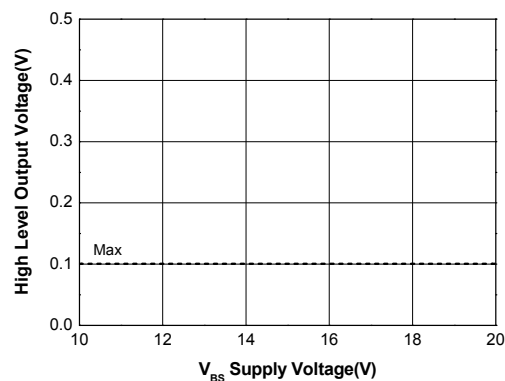


Figure 15b. High Level Output vs VBS Supply Voltage

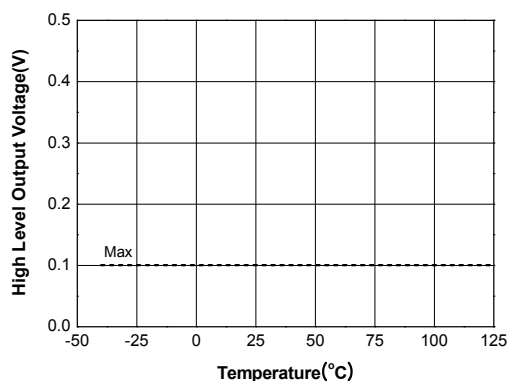


Figure 16a. Low Level Output vs Temperature

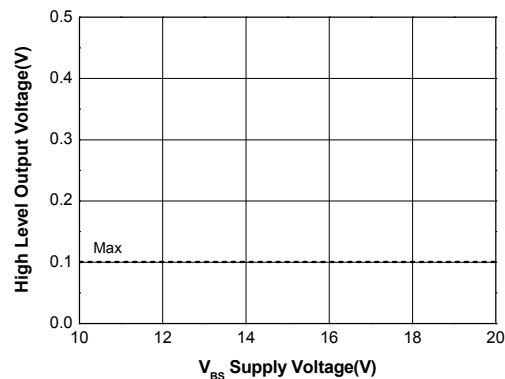


Figure 16b. Low Level Output vs VBS Supply Voltage

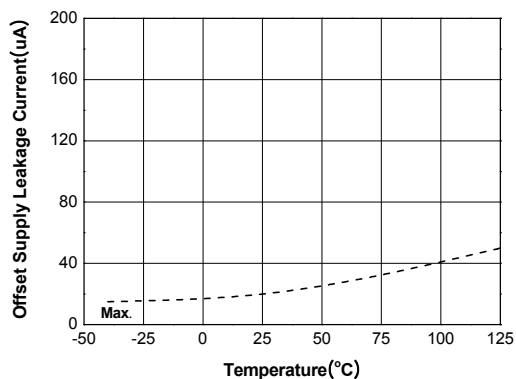


Figure 17a. Offset Supply Leakage vs Temperature

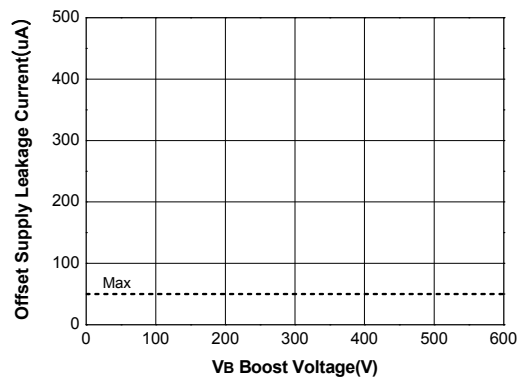


Figure 17b. Offset Supply Leakage vs Voltage

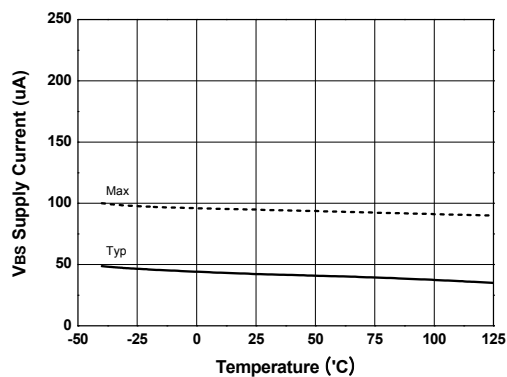


Figure 18a. VBS Supply Current vs Temperature

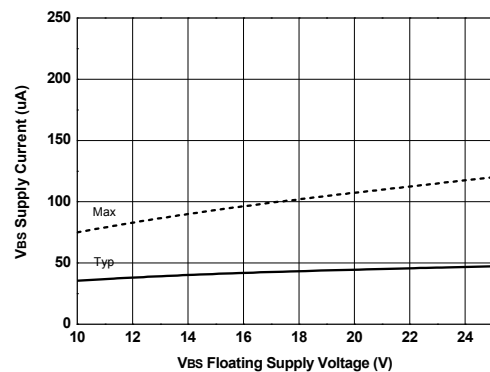


Figure 18b. VBS Supply Current vs VBS Supply Voltage

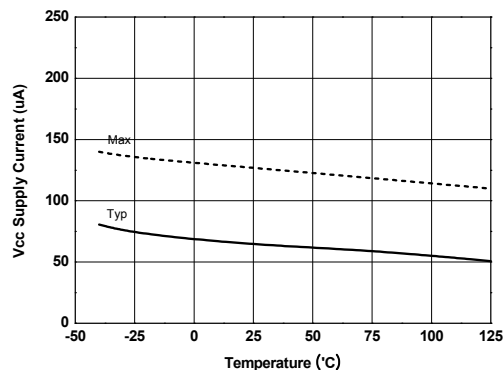


Figure 19a. VCC supply Current vs Temperature

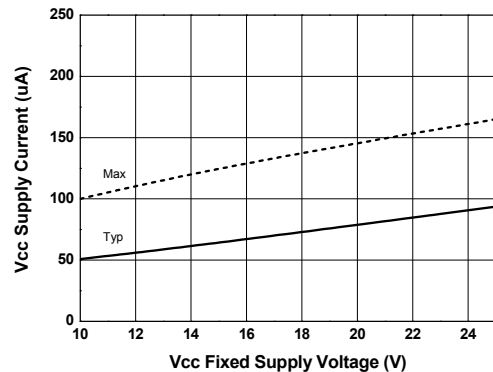


Figure 19b. VCC supply Current vs VCC Supply Voltage

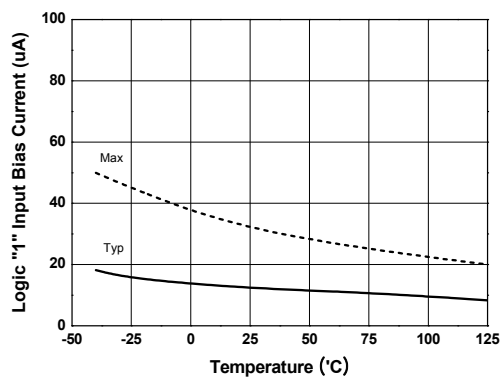


Figure 20a. Logic "1" IN Current vs Temperature

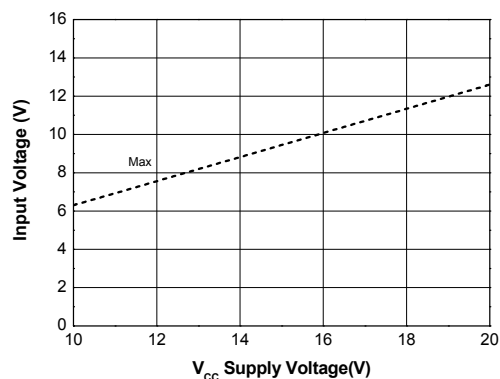


Figure 20b. Logic "1" IN Current vs Voltage

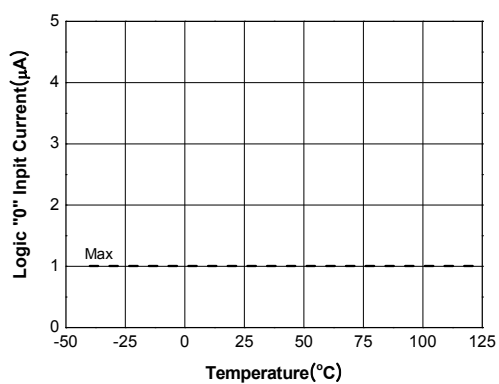


Figure 21a. Logic "0" IN Current vs Temperature

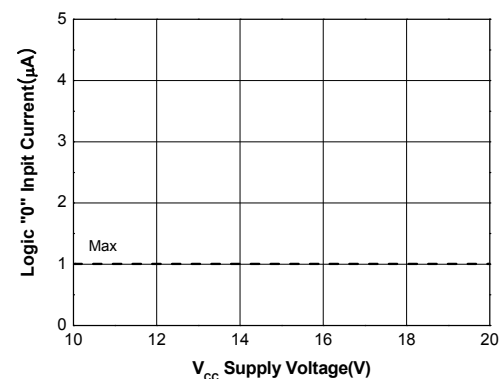


Figure 21b. Logic "0" IN Current vs Voltage

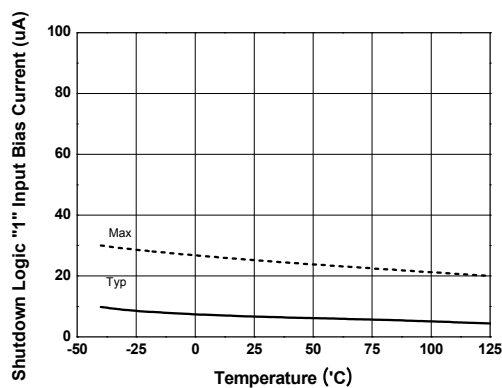


Figure 22. Logic "1" Reset Current vs Temperature

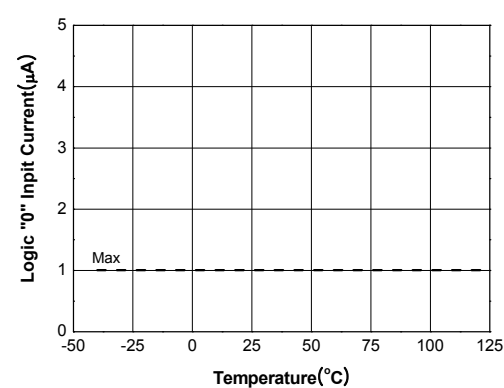


Figure 23. Logic "1" Reset Current vs Temperature

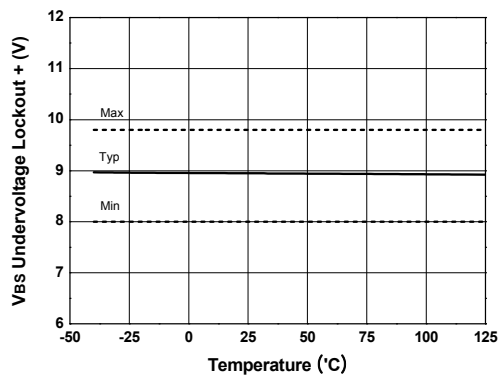


Figure 24a. VBS Undervoltage(+) vs Temperature

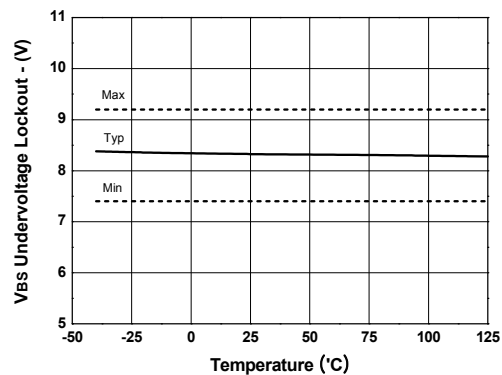


Figure 24b. VBS Undervoltage(-) vs Temperature

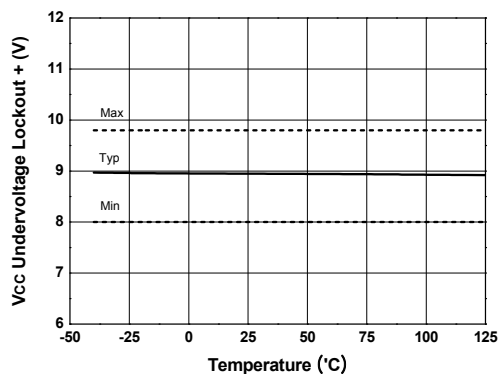


Figure 25a. VCC Undervoltage(+) vs Temperature

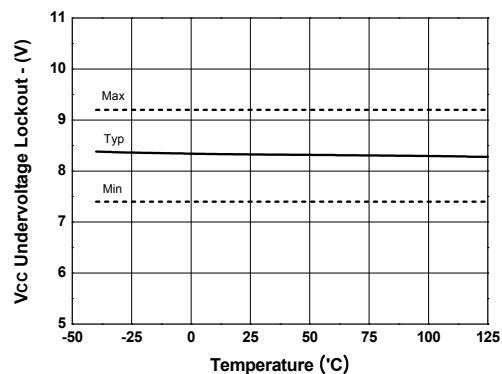


Figure 25b. VCC Undervoltage(-) vs Temperature

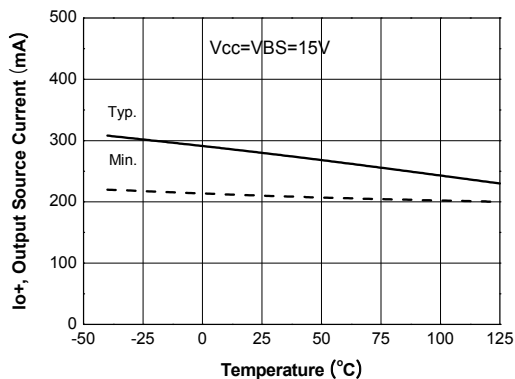


Figure 26a. Output Source Current vs Temperature

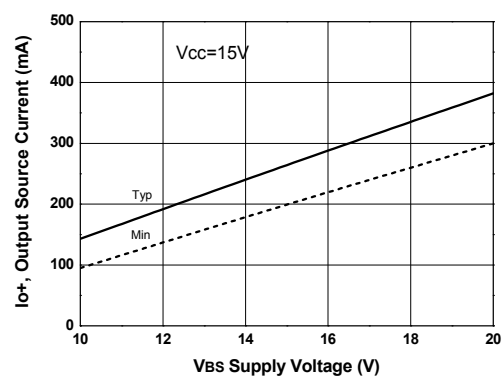


Figure 26b. Output Source Current vs Voltage

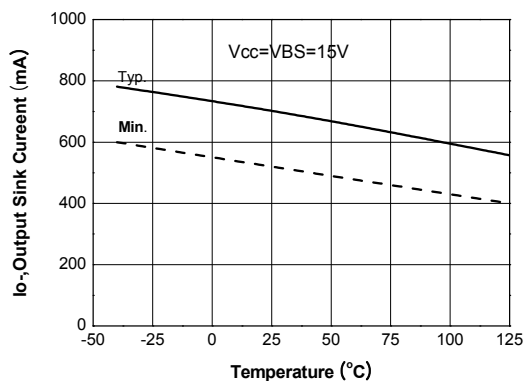


Figure 27a. Output Sink Current vs Temperature

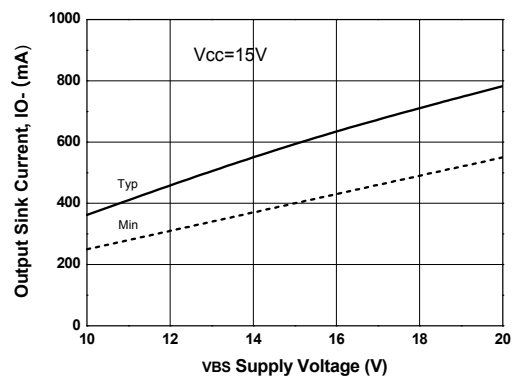


Figure 27b. Output Sink Current vs Voltage

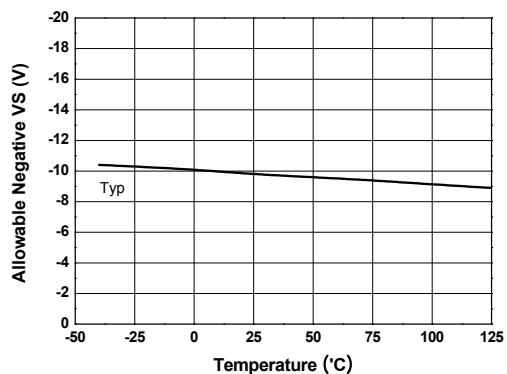


Figure 28a. Negative Allowable Offset vs Temperature

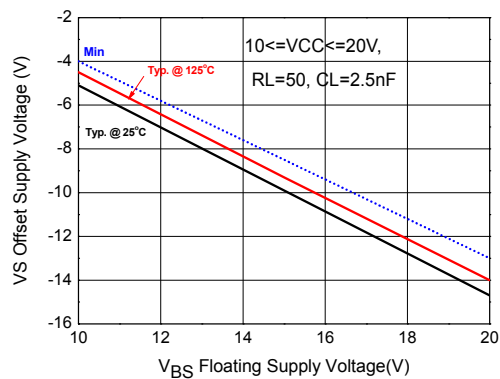
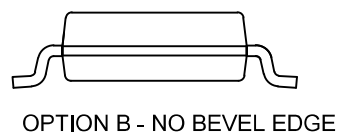
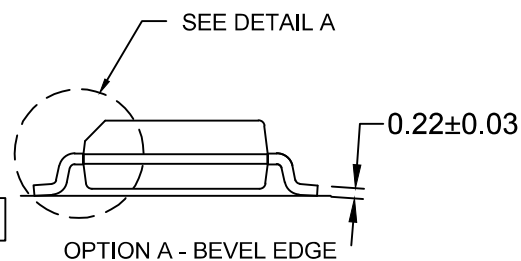
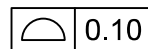
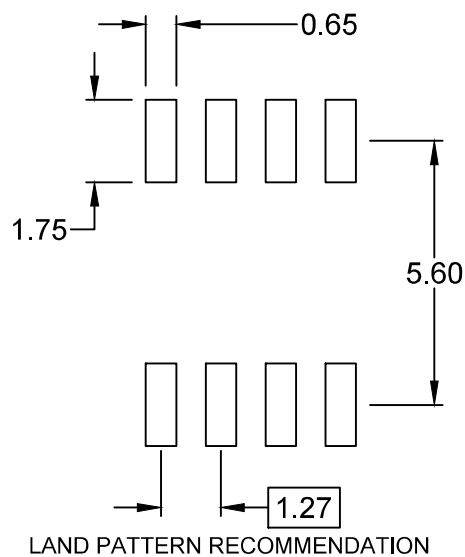


Figure 28b. Negative Allowable Offset vs Voltage



- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M
- E) DRAWING FILENAME: M08Arev16



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