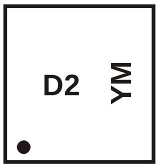
Marking Information

Site 1



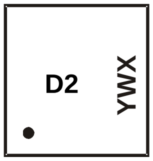
D2 = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: H = 2020)
M = Month (ex: 9 = September)

Date Code Key

Year	**2012**	**…**	**2020**	**2021**	**2022**	**2023**	**2024**	**2025**	**2026**	**2027**	**2028**	**2029**
Code	Z	…	H	I	J	K	L	M	N	O	P	R

Month	**Jan**	**Feb**	**Mar**	**Apr**	**May**	**Jun**	**Jul**	**Aug**	**Sep**	**Oct**	**Nov**	**Dec**
Code	1	2	3	4	5	6	7	8	9	O	N	D

Site 2



D2 = Product Type Marking Code
YWX = Date Code Marking
Y = Year (ex: 0 = 2020)
W = Week (ex: a = Week 27; z Represents Week 52 and 53)
X = Internal Code (ex: U = Monday)

Date Code Key

Year	**2012**	**…**	**2020**	**2021**	**2022**	**2023**	**2024**	**2025**	**2026**	**2027**	**2028**	**2029**
Code	2	…	0	1	2	3	4	5	6	7	8	9

Week	**1-26**	**27-52**	**53**
Code	A-Z	a-z	z

Internal Code	**Sun**	**Mon**	**Tue**	**Wed**	**Thu**	**Fri**	**Sat**
Code	T	U	V	W	X	Y	Z

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Q1 N-Channel	Q2 P-Channel	Unit
Drain-Source Voltage			V_{DSS}	12	-12	V
Gate-Source Voltage			V_{GSS}	±8	±8	V
Continuous Drain Current (Note 5) V_{GS} = 4.5V	Steady State	T_A = +25°C	I_D	5.6	-3.8	A
		T_A = +70°C		4.4	-3.0	
	t<5s	T_A = +25°C	I_D	7.2	-5.0	A
		T_A = +70°C		5.8	-4.0	
Maximum Continuous Body Diode Forward Current (Note 5)			I_S	1	-1	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	20	-15	A

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	Steady State	P_D	1.4	W
	t<5s		2.2	
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	92	°C/W
	t<5s		55	
Thermal Resistance, Junction to Case (Note 5)		$R_{\theta JC}$	30	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Note: 5. Device mounted on 1" x 1" FR-4 PCB with high coverage 2oz. copper, single sided.

Electrical Characteristics Q1 N-Channel (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)						
Drain-Source Breakdown Voltage	BV_{DSS}	12	—	—	V	V_{GS} = 0V, I_D = 250μA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	1.0	μA	V_{DS} = 12V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±8V, V_{DS} = 0V
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.4	—	1	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	17	29	mΩ	V_{GS} = 4.5V, I_D = 5A
		—	20	34		V_{GS} = 2.5V, I_D = 4.6A
		—	24	44		V_{GS} = 1.8V, I_D = 4.1A
		—	30	65		V_{GS} = 1.5V, I_D = 2A
Forward Transfer Admittance	$\|Y_{fs}\|$	—	6.5	—	s	V_{DS} = 10V, I_D = 5A
Diode Forward Voltage	V_{SD}	—	0.6	1.2	V	V_{GS} = 0V, I_S = 1A
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	C_{iss}	—	914	—	pF	V_{DS} = 6V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	132	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	119	—	pF	
Gate Resistance	R_g	—	1.26	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	10.5	—	nC	V_{DS} = 6V, I_D = 6.5A
Total Gate Charge (V_{GS} = 8V)		—	19.6	—	nC	
Gate-Source Charge	Q_{gs}	—	1.2	—	nC	
Gate-Drain Charge	Q_{gd}	—	1.6	—	nC	
Turn-On Delay Time	$t_{D(on)}$	—	5.0	—	ns	V_{DD} = 6V, V_{GS} = 4.5V, R_L = 1.2Ω, R_G = 1Ω
Turn-On Rise Time	t_r	—	10.5	—	ns	
Turn-Off Delay Time	$t_{D(off)}$	—	16.6	—	ns	
Turn-Off Fall Time	t_f	—	4.1	—	ns	

Electrical Characteristics Q2 P-Channel (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)						
Drain-Source Breakdown Voltage	BV_{DSS}	-12	—	—	V	V_{GS} = 0V, I_D = -250μA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	-1.0	μA	V_{DS} = -12V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±8V, V_{DS} = 0V
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	$V_{GS(TH)}$	-0.4	—	-1	V	V_{DS} = V_{GS}, I_D = -250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	37	61	mΩ	V_{GS} = -4.5V, I_D = -3.6A
		—	47	81		V_{GS} = -2.5V, I_D = -3.2A
		—	63	115		V_{GS} = -1.8V, I_D = -1A
		—	90	170		V_{GS} = -1.5V, I_D = -1A
Forward Transfer Admittance	$\|Y_{fs}\|$	—	5.5	—	s	V_{DS} = -10V, I_D = -3.6A
Diode Forward Voltage	V_{SD}	—	-0.65	-1.2	V	V_{GS} = 0V, I_S = -1A
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	C_{iss}	—	915	—	pF	V_{DS} = -6V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	225	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	183	—	pF	
Gate Resistance	R_g	—	56.9	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = -4.5V)	Q_g	—	10.7	—	nC	V_{DS} = -6V, I_D = -4.3A
Total Gate Charge (V_{GS} = -8V)		—	17.9	—	nC	
Gate-Source Charge	Q_{gs}	—	1.7	—	nC	
Gate-Drain Charge	Q_{gd}	—	3.0	—	nC	
Turn-On Delay Time	$t_{D(on)}$	—	5.7	—	ns	V_{DD} = -6V, V_{GS} = -4.5V, R_L = 1.6Ω, R_G = 1Ω
Turn-On Rise Time	t_r	—	11.5	—	ns	
Turn-Off Delay Time	$t_{D(off)}$	—	27.8	—	ns	
Turn-Off Fall Time	t_f	—	26.4	—	ns	

Notes: 6. Short duration pulse test used to minimize self-heating effect.
7. Guaranteed by design. Not subject to product testing.

Q1 N-CHANNEL

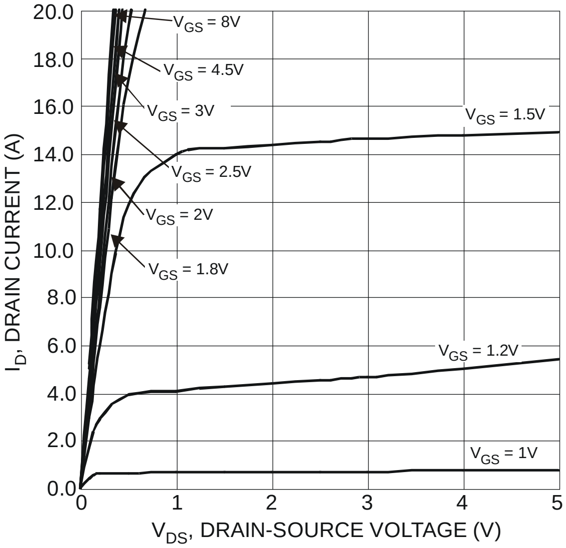


Figure 1 Typical Output Characteristics

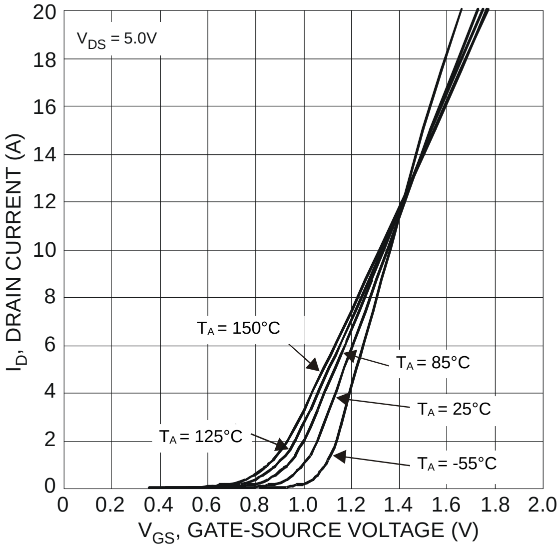


Figure 2 Typical Transfer Characteristics

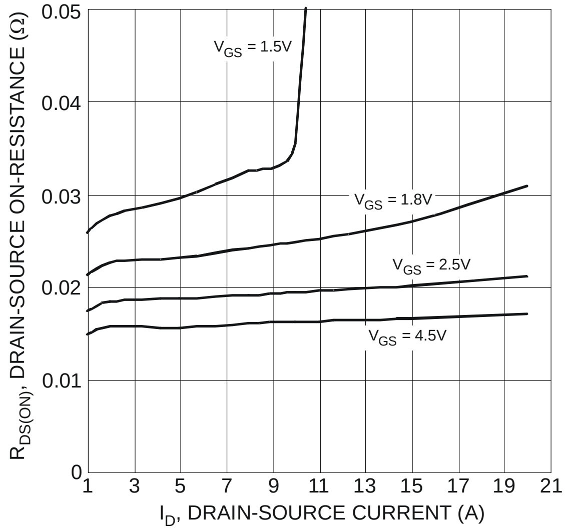


Figure 3 Typical On-Resistance vs.
Drain Current and Gate Voltage

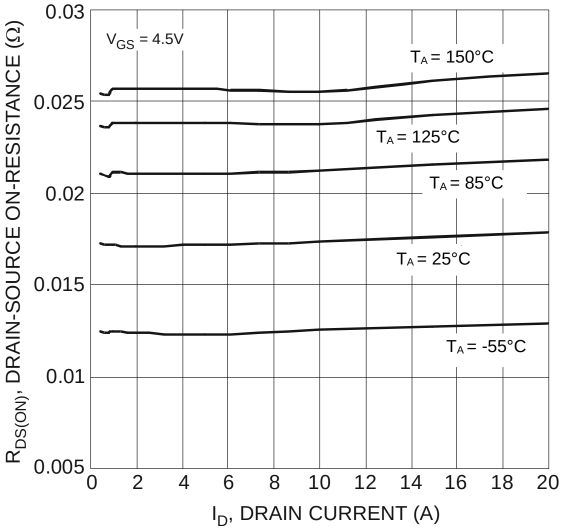


Figure 4 Typical On-Resistance vs.
Drain Current and Temperature

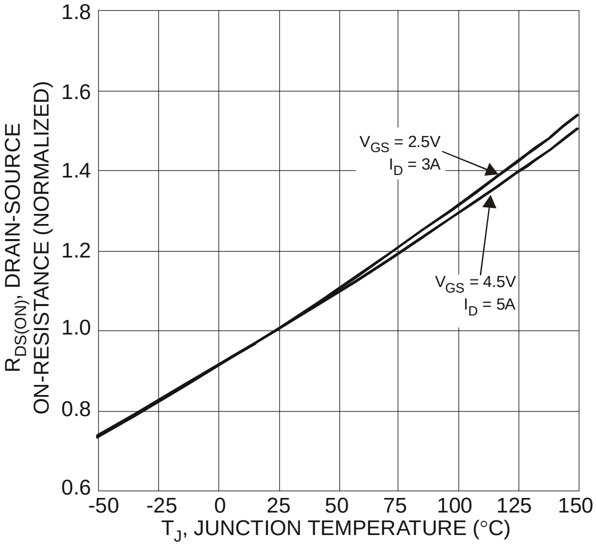


Figure 5 On-Resistance Variation with Temperature

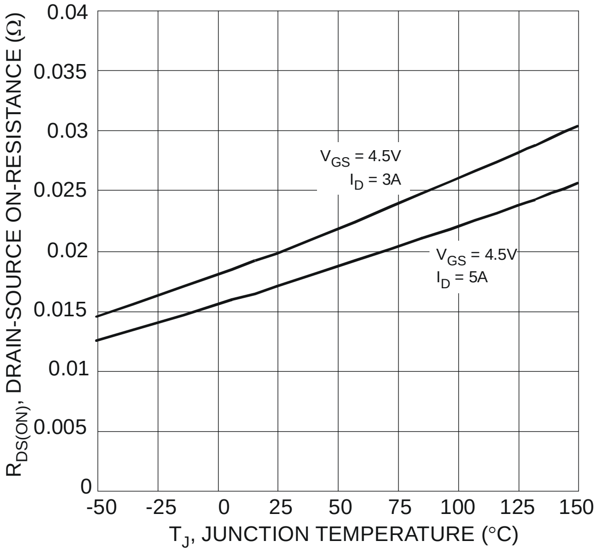


Figure 6 On-Resistance Variation with Temperature

Q1 N-CHANNEL (continued)

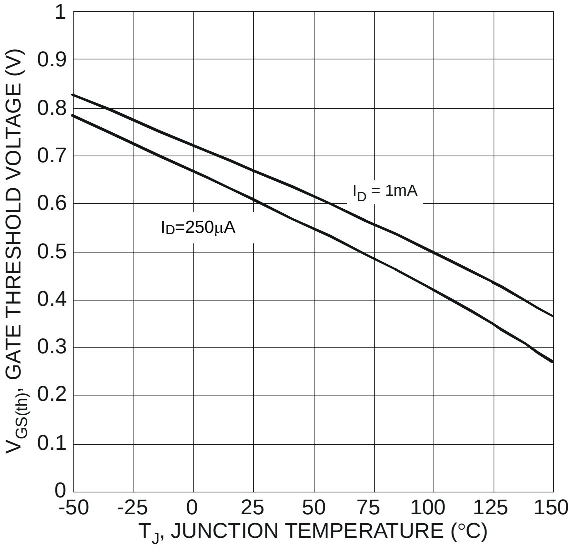


Figure 7 Gate Threshold Variation vs. Junction Temperature

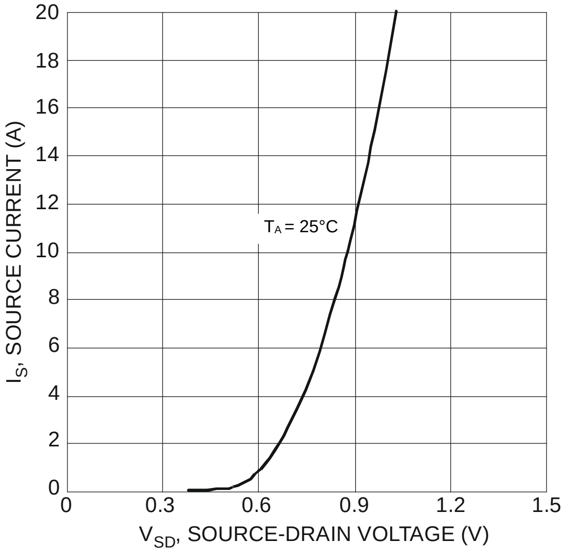


Figure 8 Diode Forward Voltage vs. Current

Q2 P-CHANNEL

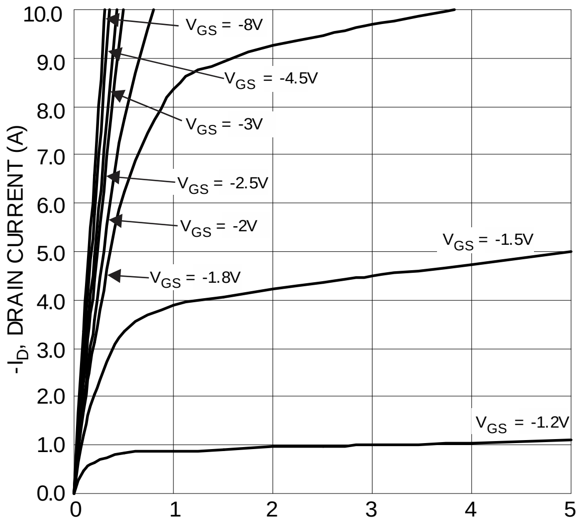


Figure 9 Typical Output Characteristics

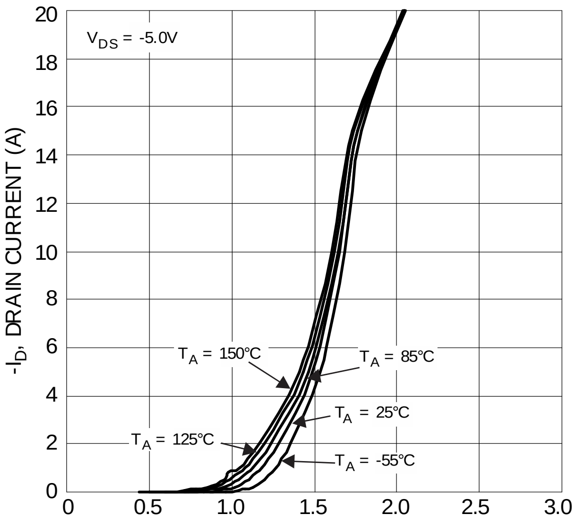


Figure 10 Typical Transfer Characteristics

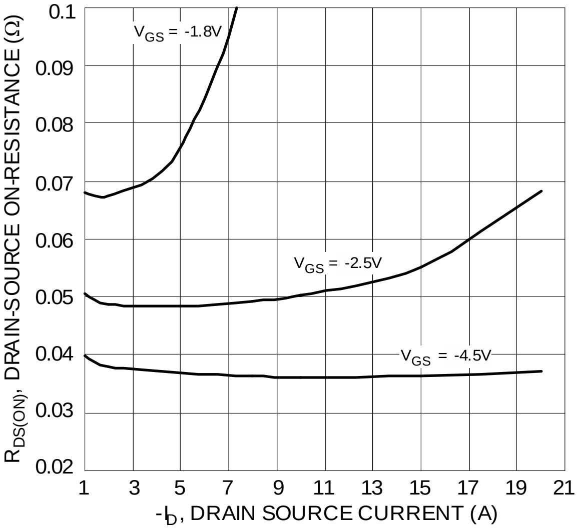


Figure 11 Typical On-Resistance vs.
Drain Current and Gate Voltage

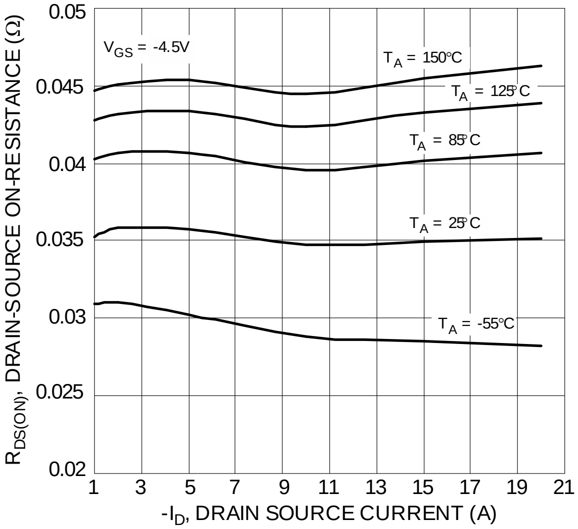


Figure 12 Typical On-Resistance vs.
Drain Current and Temperature

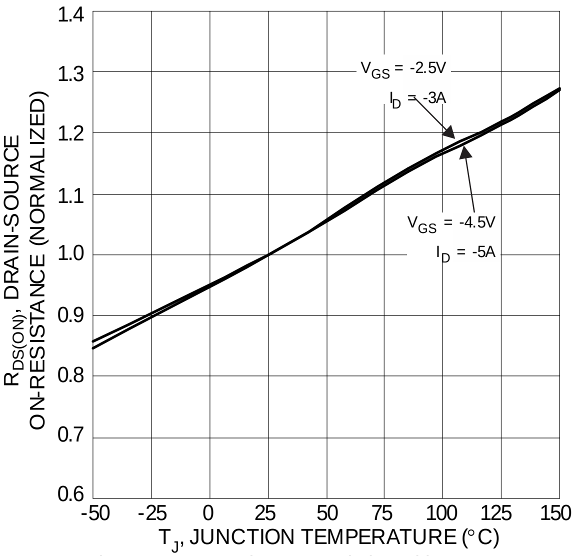


Figure 13 On-Resistance Variation with Temperature

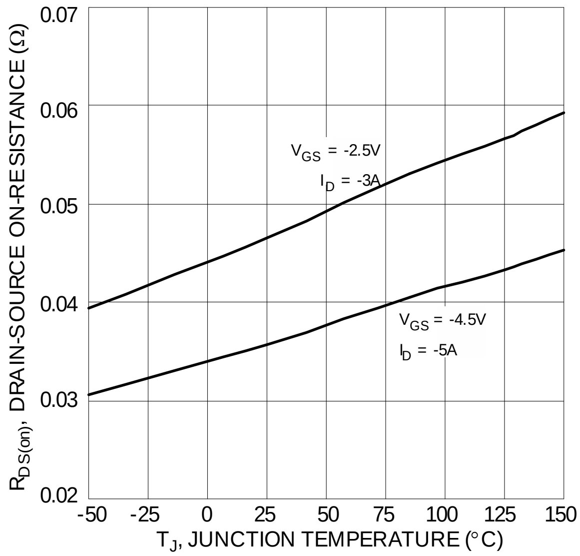


Figure 14 On-Resistance Variation with Temperature

Q2 P-CHANNEL (continued)

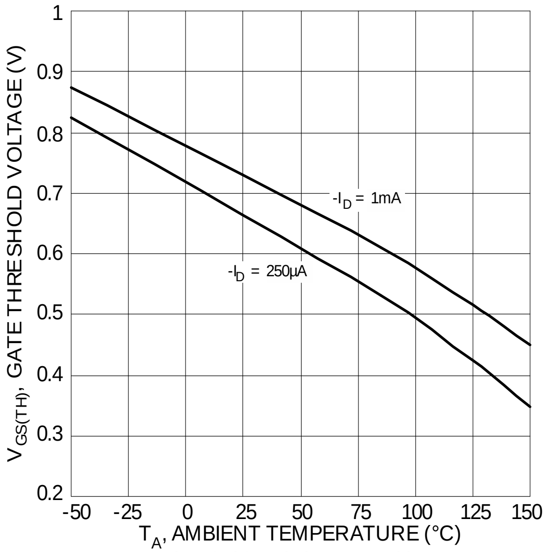


Figure 15 Gate Threshold Variation vs. Ambient Temperature

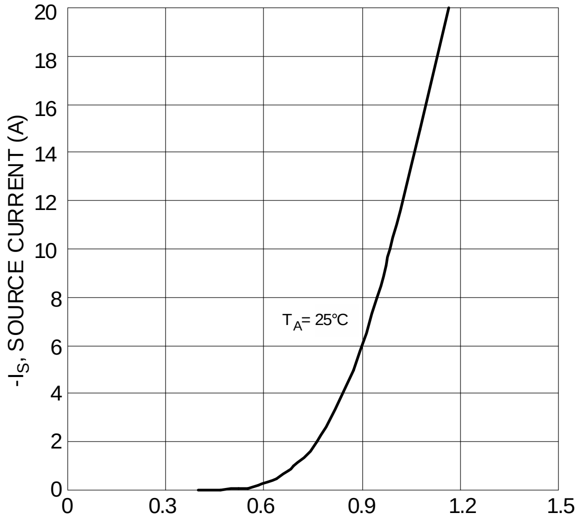


Figure 16 Diode Forward Voltage vs. Current

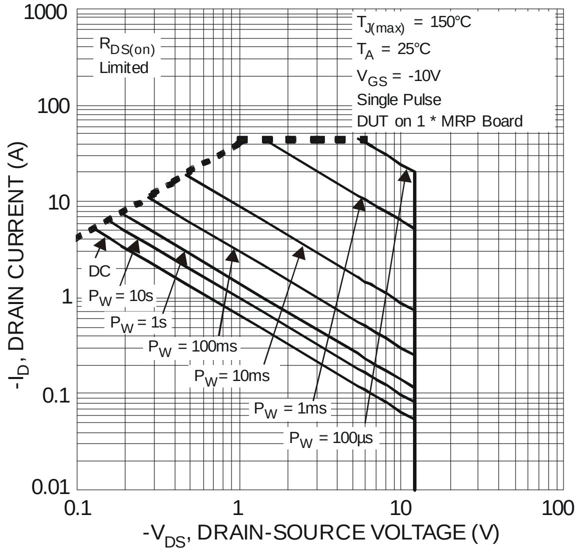


Figure 17 SOA, Safe Operation Area

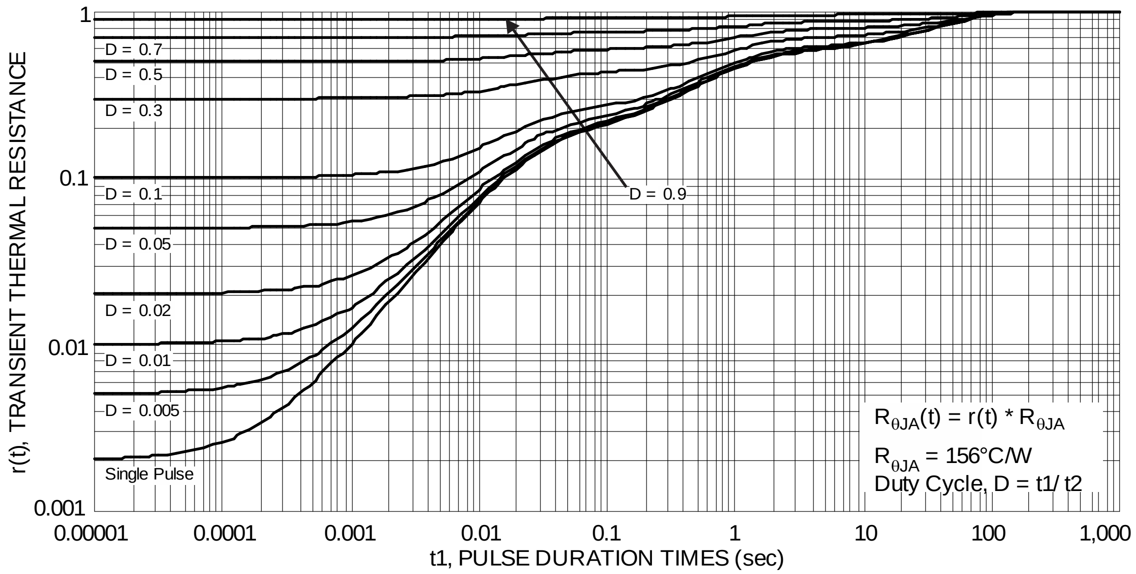
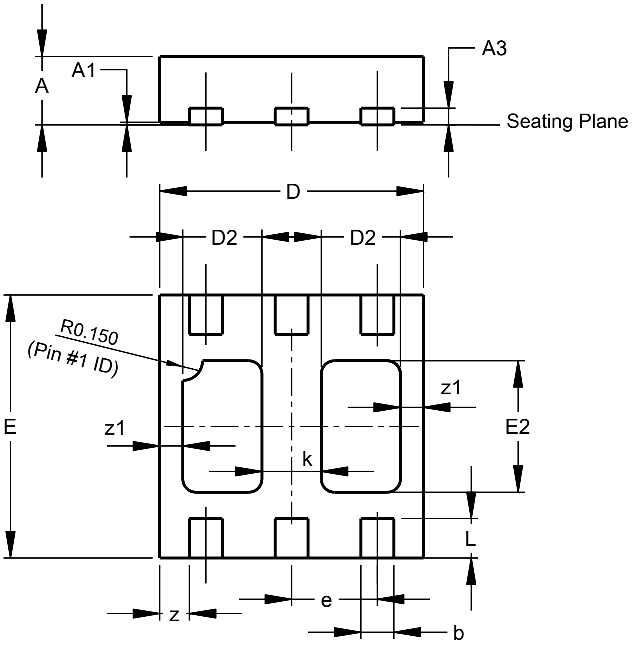


Figure 18 Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6 (Type B)

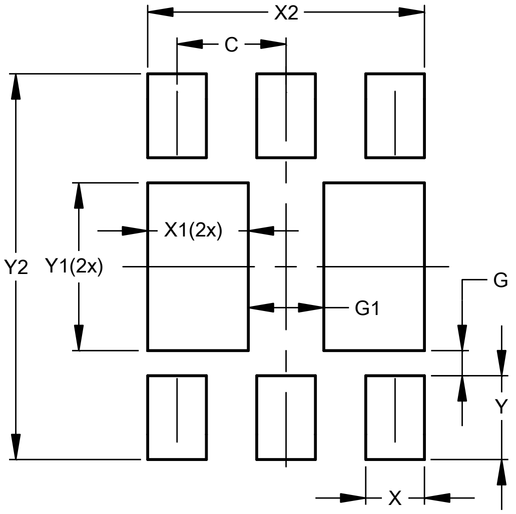


U-DFN2020-6 (Type B)			
Dim	**Min**	**Max**	**Typ**
A	0.545	0.605	0.575
A1	0.00	0.05	0.02
A3	-	-	0.13
b	0.20	0.30	0.25
D	1.95	2.075	2.00
D2	0.50	0.70	0.60
e	-	-	0.65
E	1.95	2.075	2.00
E2	0.90	1.10	1.00
k	-	-	0.45
L	0.25	0.35	0.30
z	-	-	0.225
z1	-	-	0.175
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6 (Type B)



Dimensions	Value (in mm)
C	0.650
G	0.150
G1	0.450
X	0.350
X1	0.600
X2	1.650
Y	0.500
Y1	1.000
Y2	2.300

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