Application with Other Bus Architectures

The CY7C964A is optimized for applications requiring wide buffers and high-performance multiplexing operations. The architecture can be configured to provide functions such as 16-bit bidirectional three-state latch and 16-bit comparator with mask register, or more complex functions such as 16-to-8 pipelined bidirectional multiplexer with address counter/comparator circuitry. The device can be cascaded to generate counters and comparators suitable for multiple byte address/data buses. The on-chip 48 mA drivers can be directly connected to many standard backplane buses.

Ordering Information

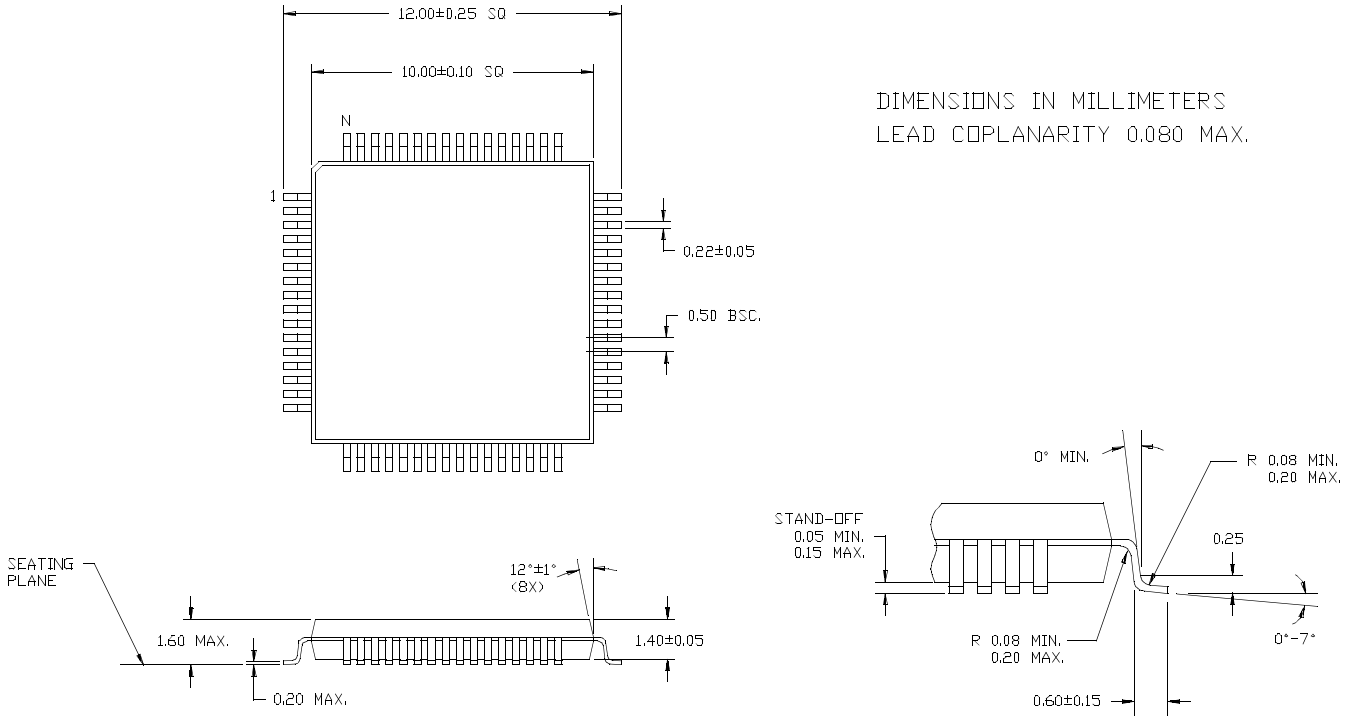
Ordering Code	Package Name	Package Type	Operating Range
CY7C964A–ASC	A64	64-Pin Thin Quad Flatpack	Commercial
CY7C964A–NC	N65	64-Pin Plastic Quad Flatpack	
CY7C964A–UM	U65	64-Pin Ceramic Quad Flatpack	Military
CY7C964A–UMB	U65	64-Pin Ceramic Quad Flatpack	

Related Documents

VMEbus Interface Handbook

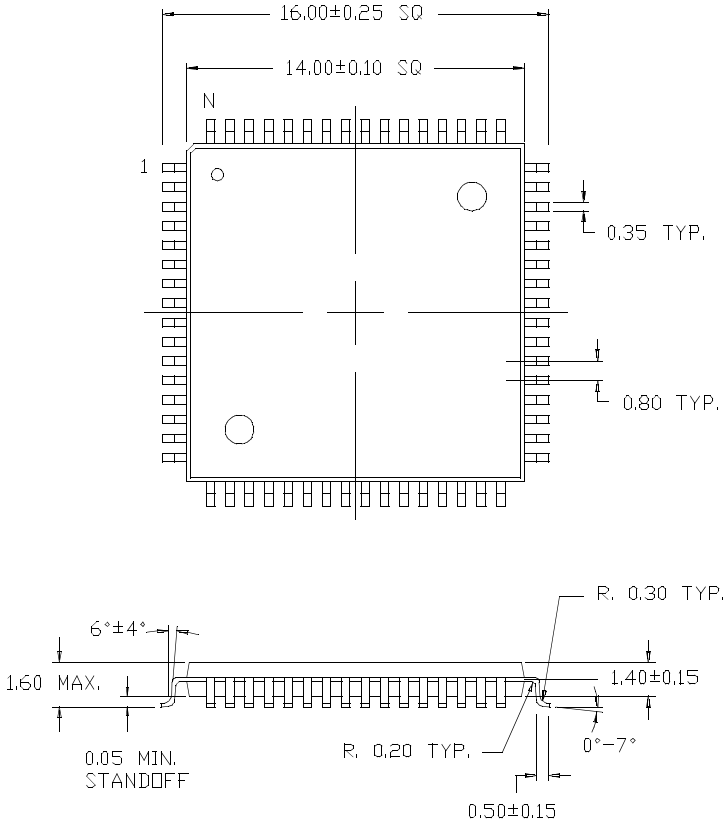
Package Diagrams

64-Pin Thin Quad Flatpack A64



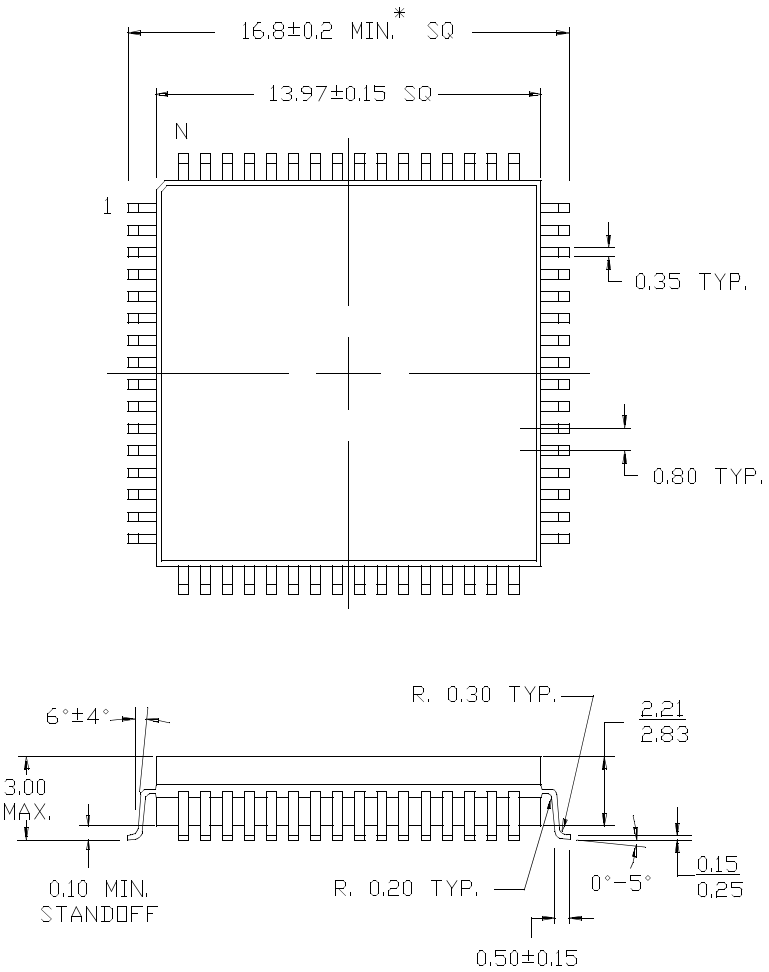
Package Diagrams (continued)

64-Lead Plastic Thin Quad Flatpack N65



Package Diagrams (continued)

64-Lead Ceramic Quad Flatpack (Cavity Up) U65



DIMENSIONS IN MILLIMETERS

LEAD COPLANARITY 0.102 MAX.

DIMENSION	MIN. / MAX.

Document Title: CY7C964A Bus Interface Logic Circuit Document Number: 38-09001				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106236	04/20/01	SZV	Change from Spec number: 38-00197 to 38-09001
*A	107043	06/12/01	KBN	Change from CY7C964 to CY7C964A; removed GMB and GM packages