CY14E256LA

256-Kbit (32 K × 8) nvSRAM

Features

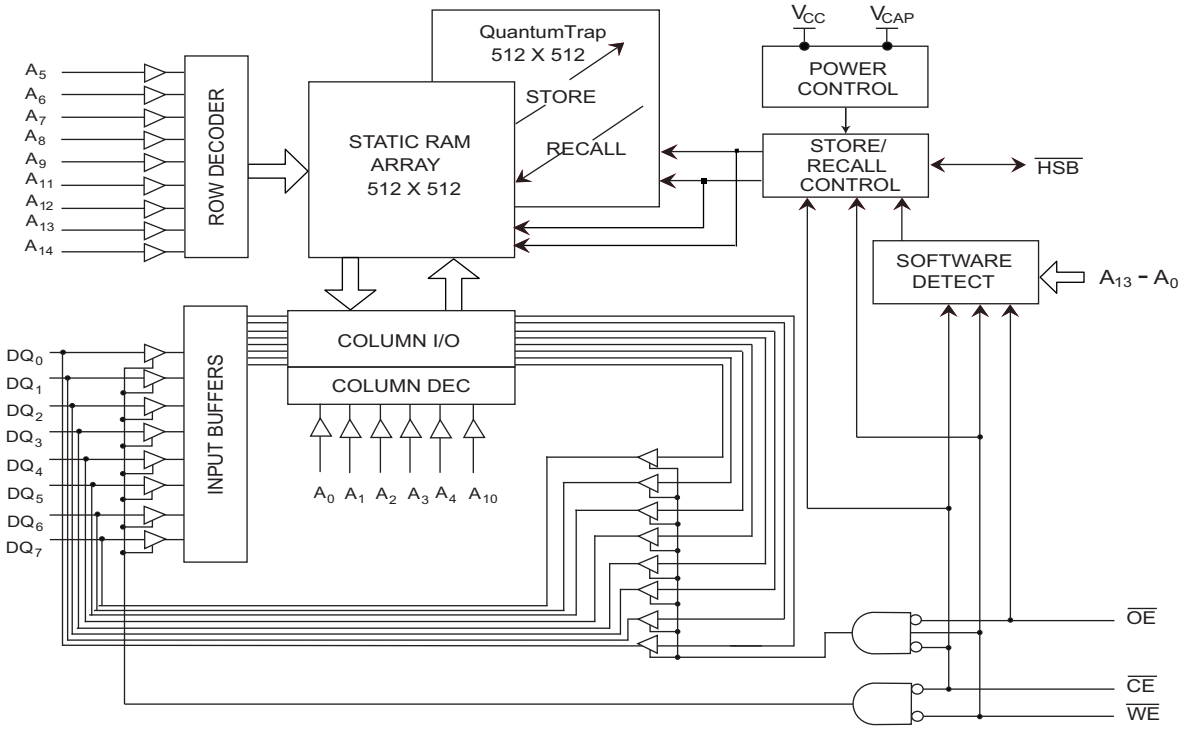
- 25 ns and 45 ns access times
- Internally organized as 32 K × 8 (CY14E256LA)
- Hands-off automatic STORE on power-down with only a small capacitor
- STORE to QuantumTrap nonvolatile elements initiated by software, device pin, or autostore on power-down
- RECALL to SRAM initiated by software or power-up
- Infinite read, write, and RECALL cycles
- 1 million STORE cycles to QuantumTrap
- 20-year data retention
- Single 5 V ± 10% operation
- Industrial temperature
- 44-pin thin small-outline package (TSOP) Type II and 32-pin small-outline integrated circuit (SOIC) package
- Pb-free and restriction of hazardous substances (RoHS) compliant

Functional Description

The Cypress CY14E256LA is a fast static RAM, with a nonvolatile element in each memory cell. The memory is organized as 32 KB. The embedded nonvolatile elements incorporate QuantumTrap technology, producing the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, while independent nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power-down. On power-up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

For a complete list of related documentation, click here.

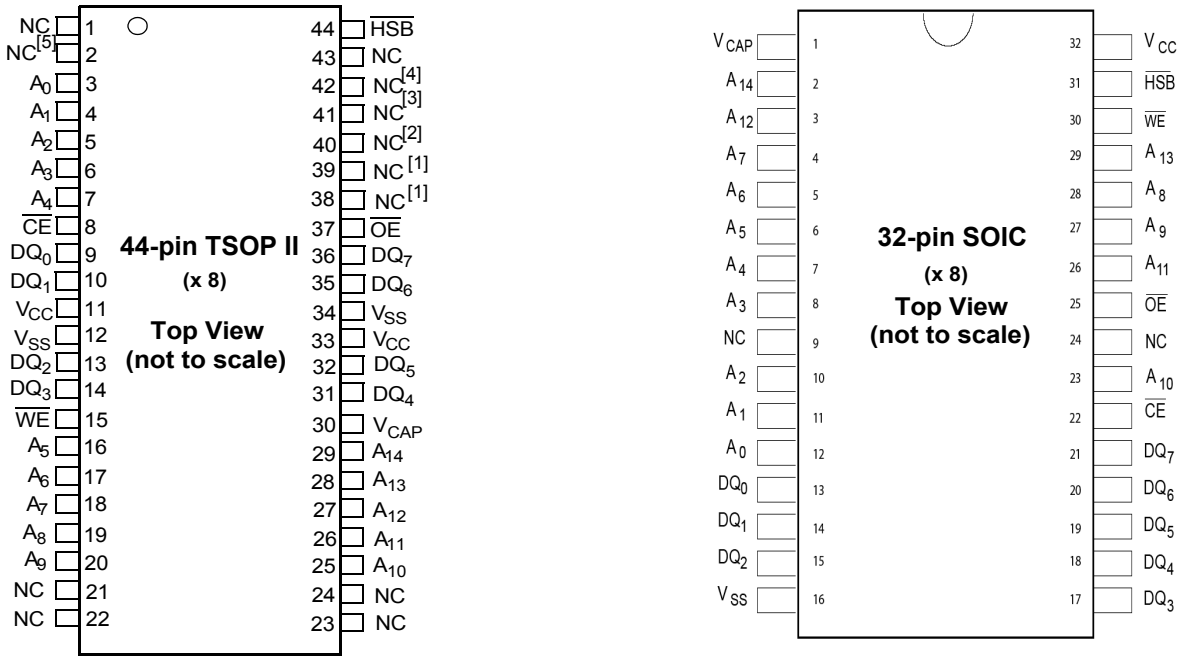
Logic Block Diagram



Contents

Pinouts

Figure 1. 44-pin TSOP II / 32-pin SOIC pinout



Pin Definitions

Pin Name	I/O Type	Description
A_0–A_{14}	Input	Address inputs. Used to select one of the 32,768 bytes of the nvSRAM.
DQ_0–DQ_7	Input/Output	Bidirectional data I/O Lines. Used as input or output lines depending on operation.
$\overline{WE}$	Input	Write Enable input, Active LOW. When the chip is enabled and $\overline{WE}$ is LOW, data on the I/O pins is written to the specific address location.
$\overline{CE}$	Input	Chip Enable input, Active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	Input	Output Enable, Active LOW. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. I/O pins are tri-stated on deasserting $\overline{OE}$ HIGH.
V_{SS}	Ground	Ground for the device. Must be connected to the ground of the system.
V_{CC}	Power supply	Power supply inputs to the device.
$\overline{HSB}$	Input/Output	Hardware STORE Busy ($\overline{HSB}$). When LOW, this output indicates that a Hardware STORE is in progress. When pulled LOW, external to the chip, it initiates a nonvolatile STORE operation. After each Hardware and Software STORE operation $\overline{HSB}$ is driven HIGH for a short time (t_{HHHD}) with standard output high current and then a weak internal pull-up resistor keeps this pin HIGH (external pull-up resistor connection is optional).
V_{CAP}	Power supply	AutoStore capacitor. Supplies power to the nvSRAM during power loss to store data from SRAM to nonvolatile elements.
NC	No connect	No connect. This pin is not connected to the die.

Notes
1. Address expansion for 1-Mbit. NC pin not connected to die.
2. Address expansion for 2-Mbit. NC pin not connected to die.
3. Address expansion for 4-Mbit. NC pin not connected to die.
4. Address expansion for 8-Mbit. NC pin not connected to die.
5. Address expansion for 16-Mbit. NC pin not connected to die.

Device Operation

The CY14E256LA nvSRAM is made up of two functional components paired in the same physical cell. They are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to the SRAM (the RECALL operation). Using this unique architecture, all cells are stored and recalled in parallel. During the STORE and RECALL operations, SRAM read and write operations are inhibited. The CY14E256LA supports infinite reads and writes similar to a typical SRAM. In addition, it provides infinite RECALL operations from the nonvolatile cells and up to 1 million STORE operations. Refer to the Truth Table For SRAM Operations on page 15 for a complete description of read and write modes.

SRAM Read

The CY14E256LA performs a read cycle when $\overline{CE}$ and $\overline{OE}$ are LOW and $\overline{WE}$ and $\overline{HSB}$ are HIGH. The address specified on pins A_{0-14} determines which of the 32,768 data bytes each are accessed. When the read is initiated by an address transition, the outputs are valid after a delay of t_{AA} (read cycle 1). If the read is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at t_{ACE} or at t_{DOE}, whichever is later (read cycle 2). The data output repeatedly responds to address changes within the t_{AA} access time without the need for transitions on any control input pins. This remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ or $\overline{HSB}$ is brought LOW.

SRAM Write

A write cycle is performed when $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{HSB}$ is HIGH. The address inputs must be stable before entering the write cycle and must remain stable until $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common I/O pins DQ_{0-7} are written into the memory if the data is valid t_{SD} before the end of a $\overline{WE}$-controlled write or before the end of a $\overline{CE}$-controlled write. Keep $\overline{OE}$ HIGH during the entire write cycle to avoid data bus contention on common I/O lines. If $\overline{OE}$ is left LOW, internal circuitry turns off the output buffers t_{HZWE} after $\overline{WE}$ goes LOW.

AutoStore Operation

The CY14E256LA stores data to the nvSRAM using one of the following three storage operations: Hardware STORE activated by $\overline{HSB}$; Software STORE activated by an address sequence; AutoStore on device power-down. The AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14E256LA.

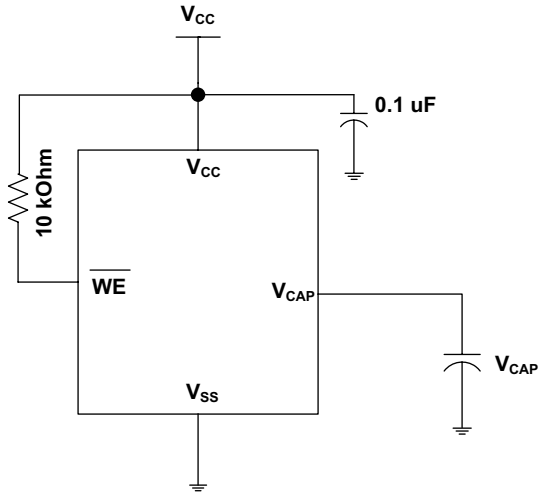
During a normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC}. A STORE operation is initiated with power provided by the V_{CAP} capacitor.

Note If the capacitor is not connected to V_{CAP} pin, AutoStore must be disabled using the soft sequence specified in Preventing AutoStore on page 6. In case AutoStore is enabled without a capacitor on V_{CAP} pin, the device attempts an AutoStore operation without sufficient charge to complete the Store. This corrupts the data stored in nvSRAM.

Figure 2 shows the proper connection of the storage capacitor (V_{CAP}) for automatic STORE operation. Refer to DC Electrical Characteristics on page 7 for the size of V_{CAP}. The voltage on the V_{CAP} pin is driven to V_{CC} by a regulator on the chip. Place a pull-up on $\overline{WE}$ to hold it inactive during power-up. This pull-up is only effective if the $\overline{WE}$ signal is tristate during power-up. Many MPUs tristate their controls on power-up. This must be verified when using the pull-up. When the nvSRAM comes out of power-on-RECALL, the MPU must be active or the $\overline{WE}$ held inactive until the MPU comes out of reset.

To reduce unnecessary nonvolatile stores, AutoStore and Hardware STORE operations are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a write operation has taken place. The $\overline{HSB}$ signal is monitored by the system to detect if an AutoStore cycle is in progress.

Figure 2. AutoStore Mode



Hardware STORE Operation

The CY14E256LA provides the $\overline{HSB}$ pin to control and acknowledge the STORE operations. Use the $\overline{HSB}$ pin to request a Hardware STORE cycle. When the $\overline{HSB}$ pin is driven LOW, the CY14E256LA conditionally initiates a STORE operation after t_{DELAY}. An actual STORE cycle only begins if a write to the SRAM has taken place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin also acts as an open drain driver (internal 100 kΩ weak pull-up resistor) that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

Note After each Hardware and Software STORE operation $\overline{HSB}$ is driven HIGH for a short time (t_{HHHD}) with standard output high current and then remains HIGH by internal 100 kΩ pull-up resistor.

SRAM write operations that are in progress when $\overline{HSB}$ is driven LOW by any means are given time (t_{DELAY}) to complete before the STORE operation is initiated. However, any SRAM write cycles requested after $\overline{HSB}$ goes LOW are inhibited until $\overline{HSB}$ returns HIGH. In case the write latch is not set, $\overline{HSB}$ is not driven LOW by the CY14E256LA. But any SRAM read and write cycles are inhibited until $\overline{HSB}$ is returned HIGH by MPU or other external source.

During any STORE operation, regardless of how it is initiated, the CY14E256LA continues to drive the HSB pin LOW, releasing it only when the STORE is complete. Upon completion of the STORE operation, the nvSRAM memory access is inhibited for t_{LZHSB} time after HSB pin returns HIGH. Leave the HSB unconnected if it is not used.

Hardware RECALL (Power-up)

During power-up or after any low power condition (V_{CC}< V_{SWITCH}), an internal RECALL request is latched. When V_{CC} again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete. During this time, HSB is driven low by the HSB driver.

Software STORE

Data is transferred from SRAM to the nonvolatile memory by a software address sequence. The CY14E256LA Software STORE cycle is initiated by executing sequential $\overline{CE}$ or $\overline{OE}$ controlled read cycles from six specific address locations in exact order. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. After a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence, or the sequence is aborted and no STORE or RECALL takes place.

To initiate the Software STORE cycle, the following read sequence must be performed:

1. Read address 0x0E38 Valid READ
2. Read address 0x31C7 Valid READ
3. Read address 0x03E0 Valid READ
4. Read address 0x3C1F Valid READ
5. Read address 0x303F Valid READ
6. Read address 0x0FC0 Initiate STORE cycle

The software sequence may be clocked with $\overline{CE}$ controlled reads or $\overline{OE}$ controlled reads, with $\overline{WE}$ kept HIGH for all the six READ sequences. After the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. HSB is driven LOW. After the t_{STORE} cycle time is fulfilled, the SRAM is activated again for the read and write operation.

Software RECALL

Data is transferred from nonvolatile memory to the SRAM by a software address sequence. A Software RECALL cycle is initiated with a sequence of read operations in a manner similar to the Software STORE initiation. To initiate the RECALL cycle, the following sequence of $\overline{CE}$ or $\overline{OE}$ controlled read operations must be performed:

1. Read address 0x0E38 Valid READ
2. Read address 0x31C7 Valid READ
3. Read address 0x03E0 Valid READ
4. Read address 0x3C1F Valid READ
5. Read address 0x303F Valid READ
6. Read address 0x0C63 Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared. Next, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is again ready for read and write operations. The RECALL operation does not alter the data in the nonvolatile elements.

Table 1. Mode Selection

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	A_{14}–A_0[6]	Mode	I/O	Power
H	X	X	X	Not selected	Output high Z	Standby
L	H	L	X	Read SRAM	Output data	Active
L	L	X	X	Write SRAM	Input data	Active
L	H	L	0x0E38 0x31C7 0x03E0 0x3C1F 0x303F 0x0B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore disable	Output data Output data Output data Output data Output data Output data	Active[7]

Notes
6. While there are 15 address lines on the CY14E256LA, only the lower 14 are used to control software modes.
7. The six consecutive address locations must be in the order listed. $\overline{WE}$ must be HIGH during all six cycles to enable a nonvolatile cycle.

Table 1. Mode Selection (continued)

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	A_{14}–A_0[6]	Mode	I/O	Power
L	H	L	0x0E38 0x31C7 0x03E0 0x3C1F 0x303F 0x0B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore enable	Output data Output data Output data Output data Output data Output data	Active[8]
L	H	L	0x0E38 0x31C7 0x03E0 0x3C1F 0x303F 0x0FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output data Output data Output data Output data Output data Output high Z	Active I_{CC2}[8]
L	H	L	0x0E38 0x31C7 0x03E0 0x3C1F 0x303F 0x0C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output data Output data Output data Output data Output data Output high Z	Active[8]

Preventing AutoStore

The AutoStore function is disabled by initiating an AutoStore disable sequence. A sequence of read operations is performed in a manner similar to the Software STORE initiation. To initiate the AutoStore disable sequence, the following sequence of $\overline{CE}$ or $\overline{OE}$ controlled read operations must be performed:

1. Read address 0x0E38 Valid READ
2. Read address 0x31C7 Valid READ
3. Read address 0x03E0 Valid READ
4. Read address 0x3C1F Valid READ
5. Read address 0x303F Valid READ
6. Read address 0x0B45 AutoStore Disable

The AutoStore is reenabled by initiating an AutoStore enable sequence. A sequence of read operations is performed in a manner similar to the Software RECALL initiation. To initiate the AutoStore enable sequence, the following sequence of $\overline{CE}$ or $\overline{OE}$ controlled read operations must be performed:

1. Read address 0x0E38 Valid READ
2. Read address 0x31C7 Valid READ
3. Read address 0x03E0 Valid READ
4. Read address 0x3C1F Valid READ
5. Read address 0x303F Valid READ
6. Read address 0x0B46 AutoStore Enable

If the AutoStore function is disabled or reenabled, a manual STORE operation (Hardware or Software) must be issued to save the AutoStore state through subsequent power-down cycles. The part comes from the factory with AutoStore enabled and 0x00 written in all cells.

Data Protection

The CY14E256LA protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and write operations. The low voltage condition is detected when V_{CC} is less than V_{SWITCH}. If the CY14E256LA is in a write mode (both $\overline{CE}$ and $\overline{WE}$ are LOW) at power-up, after a RECALL or STORE, the write is inhibited until the SRAM is enabled after t_{LZHSB} ($\overline{HSB}$ to output active). This protects against inadvertent writes during power-up or brown out conditions.

Note
8. The six consecutive address locations must be in the order listed. $\overline{WE}$ must be HIGH during all six cycles to enable a nonvolatile cycle.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Maximum accumulated storage time:

At 150 °C ambient temperature ..... 1000 h

At 85 °C ambient temperature ..... 20 Years

Maximum junction temperature ..... 150 °C

Supply voltage on V_{CC} relative to V_{SS} .....–0.5 V to 7.0 V

Voltage applied to outputs in high Z state ..... –0.5 V to V_{CC} + 0.5 V

Input voltage ..... –0.5 V to V_{CC} + 0.5 V

Transient voltage (< 20 ns) on any pin to ground potential ..... –2.0 V to V_{CC} + 2.0 V

Package power dissipation capability (T_A = 25 °C) ..... 1.0 W

Surface mount Pb soldering temperature (3 seconds) ..... +260 °C

DC output current (1 output at a time, 1 s duration) ... 15 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	4.5 V to 5.5 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	Min	Typ [9]	Max	Unit
V_{CC}	Power supply		4.5	5.0	5.5	V
I_{CC1}	Average V_{CC} current	t_{RC} = 25 ns t_{RC} = 45 ns Values obtained without output loads (I_{OUT} = 0 mA)	–	–	70 52	mA mA
I_{CC2}	Average V_{CC} current during STORE	All inputs don't care, V_{CC} = Max Average current for duration t_{STORE}	–	–	10	mA
I_{CC3}	Average V_{CC} current at t_{RC}= 200 ns, $V_{CC(Typ)}$, 25 °C	All inputs cycling at CMOS levels. Values obtained without output loads (I_{OUT} = 0 mA).	–	35	–	mA
I_{CC4}	Average V_{CAP} current during AutoStore cycle	All inputs don't care. Average current for duration t_{STORE}	–	–	8	mA
I_{SB}	V_{CC} standby current	$\overline{CE} \geq (V_{CC} – 0.2\ V)$. $V_{IN} \leq 0.2$ V or $\geq (V_{CC} – 0.2\ V)$. Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.	–	–	8	mA
I_{IX}[10]	Input leakage current (except HSB)	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$	–1	–	+1	µA
	Input leakage current (for $\overline{HSB}$)	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$	–100	–	+1	µA
I_{OZ}	Off-state output leakage current	V_{CC} = Max, $V_{SS} \leq V_{OUT} \leq V_{CC}$, $\overline{CE}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$	–1	–	+1	µA
V_{IH}	Input HIGH voltage		2.0	–	V_{CC} + 0.5	V
V_{IL}	Input LOW voltage		V_{SS} – 0.5	–	0.8	V
V_{OH}	Output HIGH voltage	I_{OUT} = –2 mA	2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OUT} = 4 mA	–	–	0.4	V

Notes

9. Typical values are at 25 °C, V_{CC} = $V_{CC(Typ)}$. Not 100% tested.
10. The $\overline{HSB}$ pin has I_{OUT} = –2 µA for V_{OH} of 2.4 V when both active high and low drivers are disabled. When they are enabled standard V_{OH} and V_{OL} are valid. This parameter is characterized but not tested.

DC Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions	Min	Typ [9]	Max	Unit
V_{CAP}[11]	Storage capacitor	Between V_{CAP} pin and V_{SS}	61	68	180	µF
V_{VCAP}[12, 13]	Maximum voltage driven on V_{CAP} pin by the device	V_{CC} = Max	–	–	V_{CC} – 0.5	V

Data Retention and Endurance

Over the Operating Range

Parameter	Description	Min	Unit
$DATA_R$	Data retention	20	Years
NV_C	Nonvolatile STORE operations	1,000	K

Capacitance

Parameter[13]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance (except $\overline{HSB}$)	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(Typ)}$	7	pF
	Input capacitance (for $\overline{HSB}$)		8	pF
C_{OUT}	Output capacitance (except $\overline{HSB}$)		7	pF
	Output capacitance (for $\overline{HSB}$)		8	pF

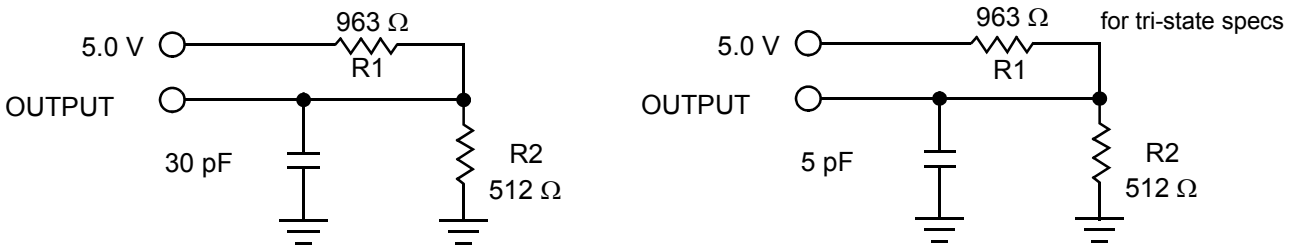
Thermal Resistance

Parameter[13]	Description	Test Conditions	44-pin TSOP II	32-pin SOIC	Unit
Θ_{JA}	Thermal resistance (Junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	41.74	41.55	°C/W
Θ_{JC}	Thermal resistance (Junction to case)		11.90	24.43	°C/W

Notes
11. Min V_{CAP} value guarantees that there is a sufficient charge available to complete a successful AutoStore operation. Max V_{CAP} value guarantees that the capacitor on V_{CAP} is charged to a minimum voltage during a Power-Up RECALL cycle so that an immediate power-down cycle can complete a successful AutoStore. Therefore it is always recommended to use a capacitor within the specified min and max limits. Refer application note AN43593 for more details on V_{CAP} options.
12. Maximum voltage on V_{CAP} pin (V_{VCAP}) is provided for guidance when choosing the V_{CAP} capacitor. The voltage rating of the V_{CAP} capacitor across the operating temperature range should be higher than the V_{VCAP} voltage.
13. These parameters are guaranteed by design and are not tested

AC Test Loads

Figure 3. AC Test Loads



AC Test Conditions

Input Pulse Levels ..... 0 V to 3 V
Input Rise and Fall Times (10% to 90%) ..... ≤ 3 ns
Input and Output Timing Reference Levels ..... 1.5 V

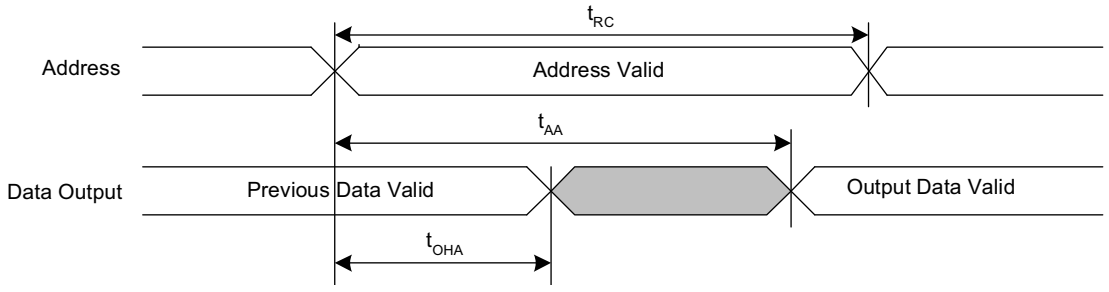
AC Switching Characteristics

Over the Operating Range

Parameters [14]		Description	25 ns		45 ns		Unit
Cypress Parameter	Alt Parameter		Min	Max	Min	Max	
SRAM Read Cycle							
t_{ACE}	t_{ACS}	Chip enable access time	–	25	–	45	ns
t_{RC}[15]	t_{RC}	Read cycle time	25	–	45	–	ns
t_{AA}[16]	t_{AA}	Address access time	–	25	–	45	ns
t_{DOE}	t_{OE}	Output enable to data valid	–	12	–	20	ns
t_{OHA}[16]	t_{OH}	Output hold after address change	3	–	3	–	ns
t_{LZCE}[17, 18]	t_{LZ}	Chip enable to output active	3	–	3	–	ns
t_{HZCE}[17, 18]	t_{HZ}	Chip disable to output inactive	–	10	–	15	ns
t_{LZOE}[17, 18]	t_{OLZ}	Output enable to output active	0	–	0	–	ns
t_{HZOE}[17, 18]	t_{OHZ}	Output disable to output inactive	–	10	–	15	ns
t_{PU}[17]	t_{PA}	Chip enable to power active	0	–	0	–	ns
t_{PD}[17]	t_{PS}	Chip disable to power standby	–	25	–	45	ns
SRAM Write Cycle							
t_{WC}	t_{WC}	Write cycle time	25	–	45	–	ns
t_{PWE}	t_{WP}	Write pulse width	20	–	30	–	ns
t_{SCE}	t_{CW}	Chip enable to end of write	20	–	30	–	ns
t_{SD}	t_{DW}	Data setup to end of write	10	–	15	–	ns
t_{HD}	t_{DH}	Data hold after end of write	0	–	0	–	ns
t_{AW}	t_{AW}	Address setup to end of write	20	–	30	–	ns
t_{SA}	t_{AS}	Address setup to start of write	0	–	0	–	ns
t_{HA}	t_{WR}	Address hold after end of write	0	–	0	–	ns
t_{HZWE}[17, 18, 19]	t_{WZ}	Write enable to output disable	–	10	–	15	ns
t_{LZWE}[17, 18]	t_{OW}	Output active after end of write	3	–	3	–	ns

Switching Waveforms

Figure 4. SRAM Read Cycle #1 (Address Controlled) [15, 16, 20]



Notes

14. Test conditions assume signal transition time of 3 ns or less, timing reference levels of $V_{CC}/2$, input pulse levels of 0 to V_{CC} (typ), and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in Figure .
15. WE must be HIGH during SRAM read cycles.
16. Device is continuously selected with CE and OE LOW.
17. These parameters are guaranteed by design and are not tested.
18. Measured ±200 mV from steady state output voltage.
19. If WE is low when CE goes low, the outputs remain in the high impedance state.
20. HSB must remain HIGH during READ and WRITE cycles.

Switching Waveforms (continued)

Figure 5. SRAM Read Cycle #2 ($\overline{CE}$ and $\overline{OE}$ Controlled) [21, 22]

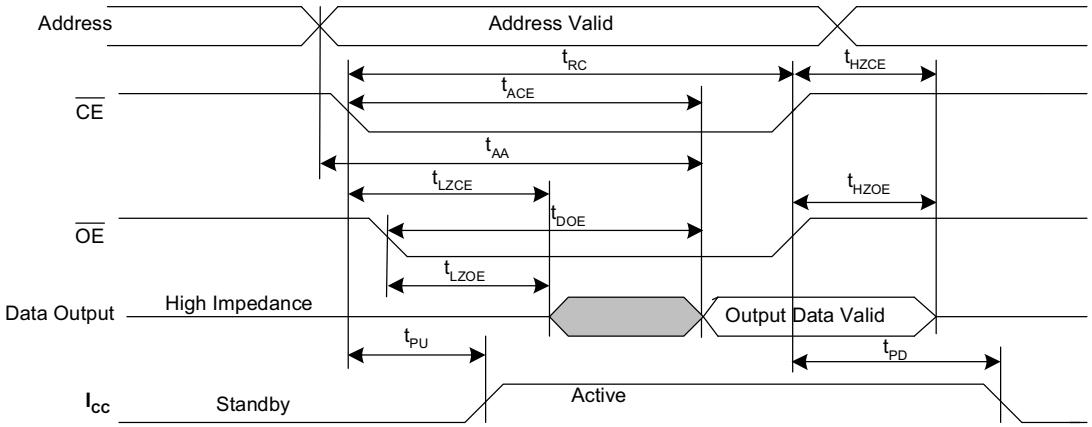


Figure 6. SRAM Write Cycle #1 ($\overline{WE}$ Controlled) [22, 23, 24]

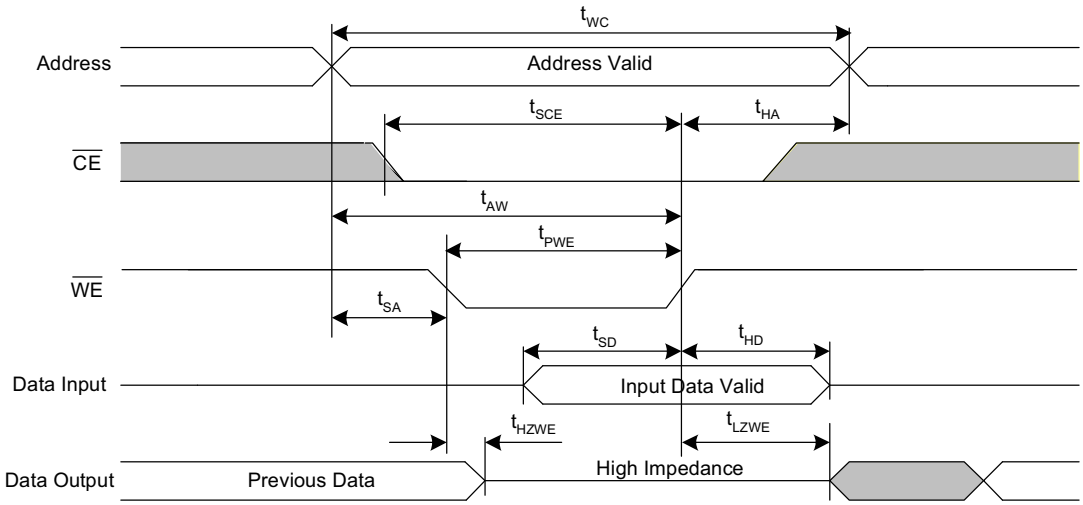
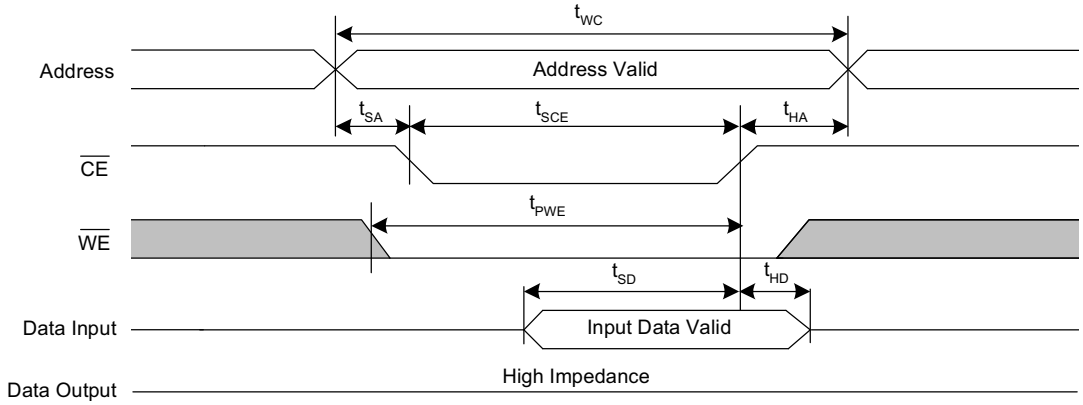


Figure 7. SRAM Write Cycle #2 ($\overline{CE}$ Controlled) [22, 23, 24]



Note
21. $\overline{WE}$ must be HIGH during SRAM read cycles.
22. $\overline{HSB}$ must remain HIGH during READ and WRITE cycles.
23. If $\overline{WE}$ is low when $\overline{CE}$ goes low, the outputs remain in the high impedance state.
24. $\overline{CE}$ or $\overline{WE}$ must be $\geq V_{IH}$ during address transitions.

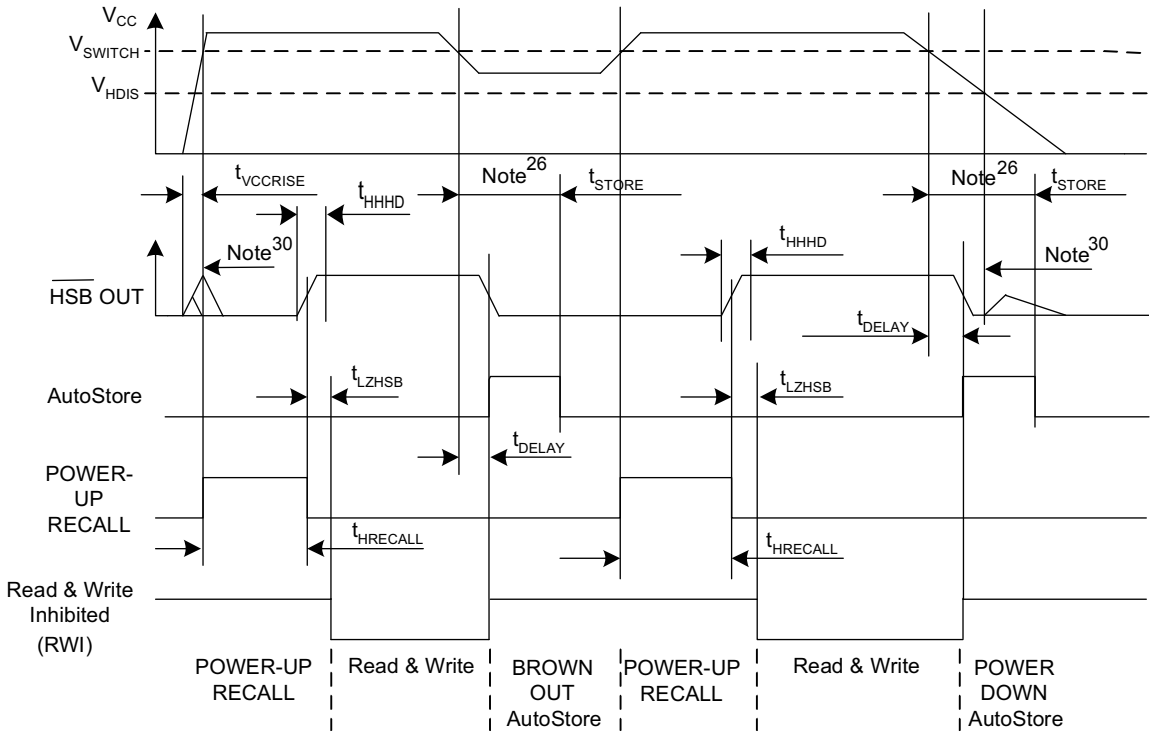
AutoStore/Power-up RECALL

Over the Operating Range

Parameter	Description	CY14E256LA		Unit
		Min	Max	
$t_{HRECALL}$[25]	Power-up RECALL duration	–	20	ms
t_{STORE}[26]	STORE cycle duration	–	8	ms
t_{DELAY}[27]	Time allowed to complete SRAM write cycle	–	25	ns
V_{SWITCH}	Low voltage trigger level	–	4.4	V
$t_{VCCRISE}$[28]	V_{CC} rise time	150	–	µs
V_{HDIS}[28]	$\overline{HSB}$ output disable voltage	–	1.9	V
t_{LZHSB}[28]	$\overline{HSB}$ to output active time	–	5	µs
t_{HHHD}[28]	$\overline{HSB}$ high active time	–	500	ns

Switching Waveforms

Figure 8. AutoStore or Power-up RECALL [29]



Notes

25. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.
26. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
27. On a Hardware STORE and AutoStore initiation, SRAM write operation continues to be enabled for time t_{DELAY}.
28. These parameters are guaranteed by design and are not tested.
29. Read and Write cycles are ignored during STORE, RECALL, and while V_{CC} is less than V_{SWITCH}.
30. During power-up and power-down, $\overline{HSB}$ glitches when $\overline{HSB}$ pin is pulled up through an external resistor.

Software Controlled STORE/RECALL Cycle

Over the Operating Range

Parameter [31, 32]	Description	25 ns		45 ns		Unit
		Min	Max	Min	Max	
t_{RC}	STORE/RECALL initiation cycle time	25	–	45	–	ns
t_{SA}	Address setup time	0	–	0	–	ns
t_{CW}	Clock pulse width	20	–	30	–	ns
t_{HA}	Address hold time	0	–	0	–	ns
t_{RECALL}	RECALL duration	–	200	–	200	µs

Switching Waveforms

Figure 9. $\overline{CE}$ and $\overline{OE}$ Controlled Software STORE/RECALL Cycle [32]

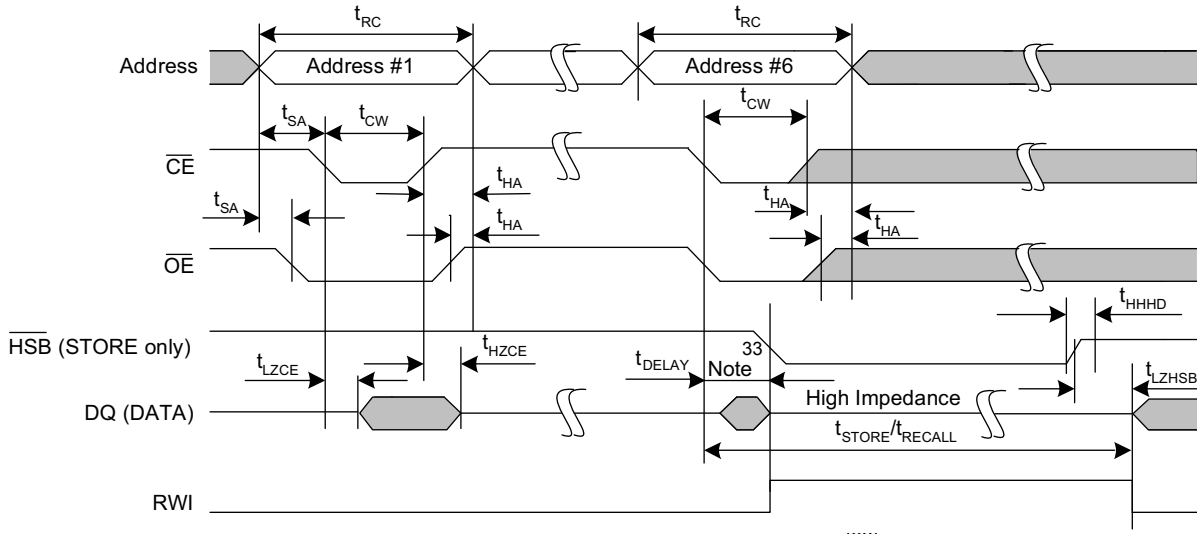
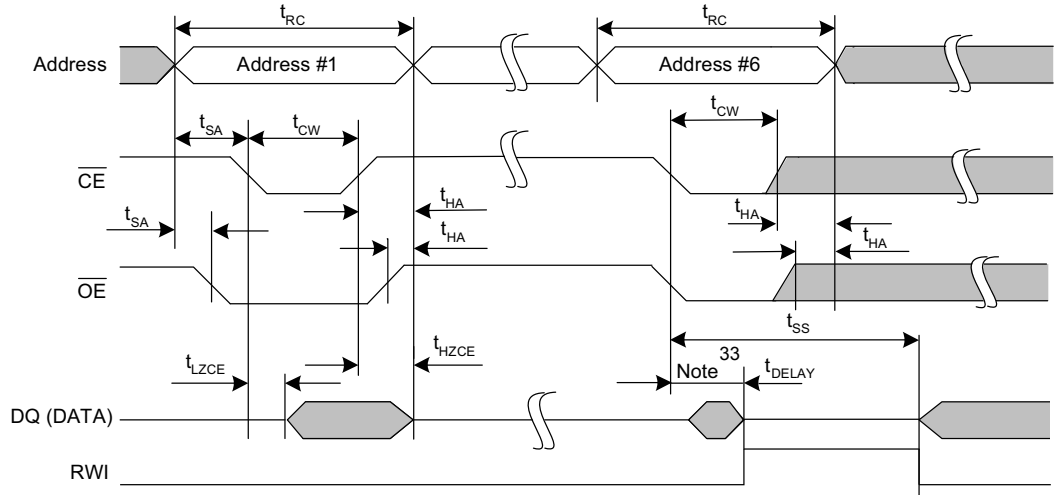


Figure 10. AutoStore Enable / Disable Cycle [32]



Notes

31. The software sequence is clocked with $\overline{CE}$ controlled or $\overline{OE}$ controlled reads.
32. The six consecutive addresses must be read in the order listed in Table 1 on page 5. $\overline{WE}$ must be HIGH during all six consecutive cycles.
33. DQ output data at the sixth read may be invalid since the output is disabled at t_{DELAY} time.

Hardware STORE Cycle

Over the Operating Range

Parameter	Description	CY14E256LA		Unit
		Min	Max	
t_{DHSB}	$\overline{HSB}$ to output active time when write latch not set	–	25	ns
t_{PHSB}	Hardware STORE pulse width	15	–	ns
t_{SS} [34, 35]	Soft sequence processing time	–	100	µs

Switching Waveforms

Figure 11. Hardware STORE Cycle [36]

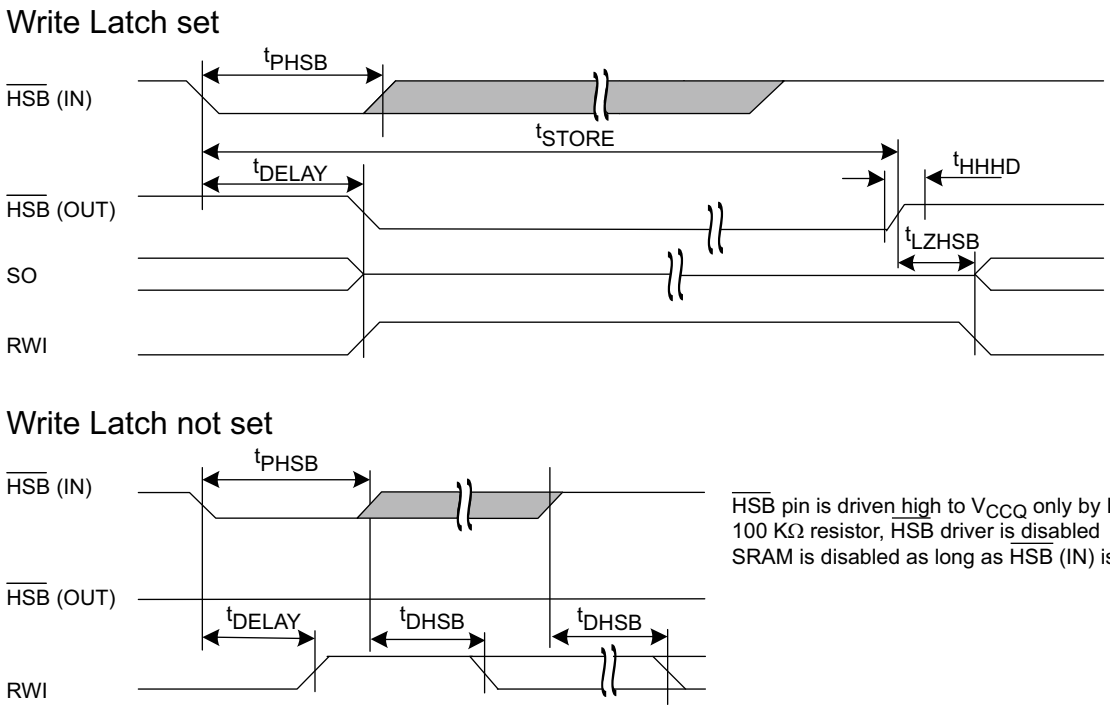
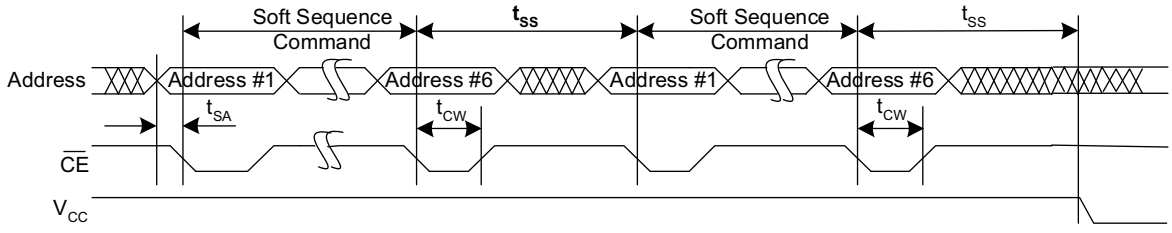


Figure 12. Soft Sequence Processing [34, 35]



Notes
34. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain HIGH to effectively register command.
35. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.
36. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.

Truth Table For SRAM Operations

$\overline{HSB}$ must remain HIGH for SRAM operations.

Table 2. Truth Table

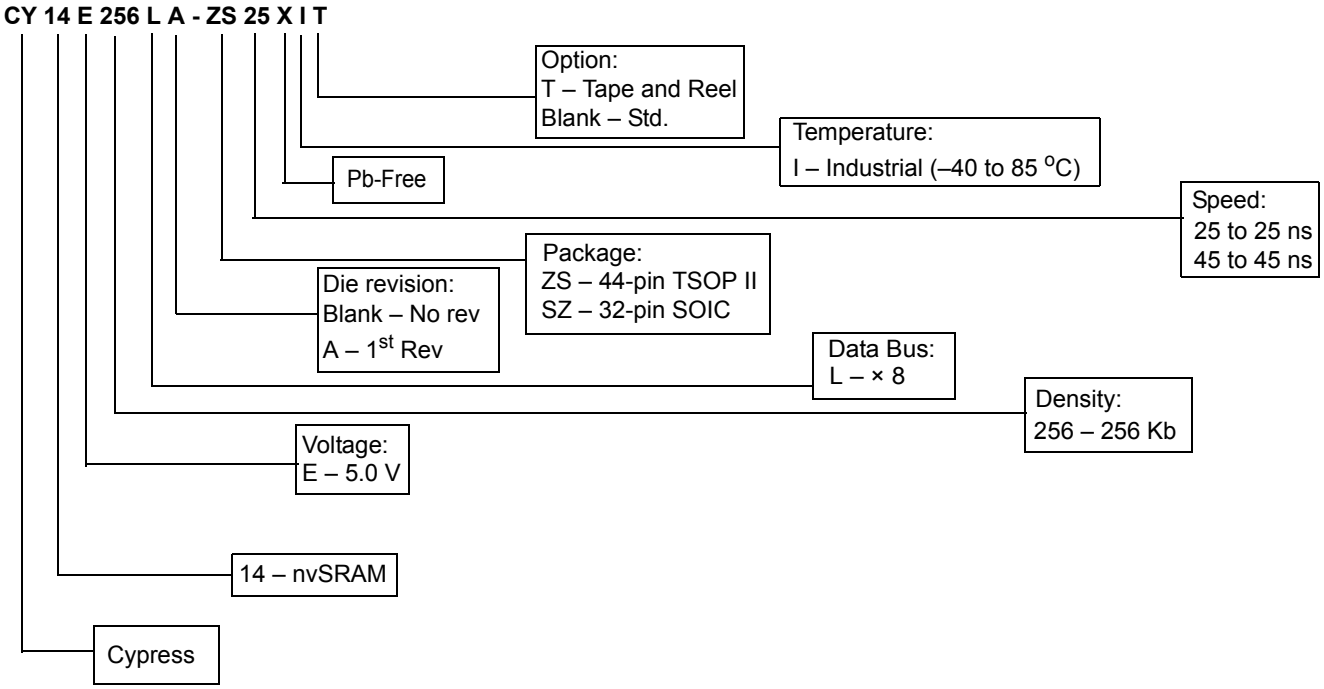
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/power-down	Standby
L	H	L	Data out (DQ_0–DQ_7)	Read	Active
L	H	H	High Z	Output disabled	Active
L	L	X	Data in (DQ_0–DQ_7)	Write	Active

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY14E256LA-SZ25XIT	51-85127	32-pin SOIC	Industrial
	CY14E256LA-SZ25XI			
45	CY14E256LA-SZ45XIT			
	CY14E256LA-SZ45XI			

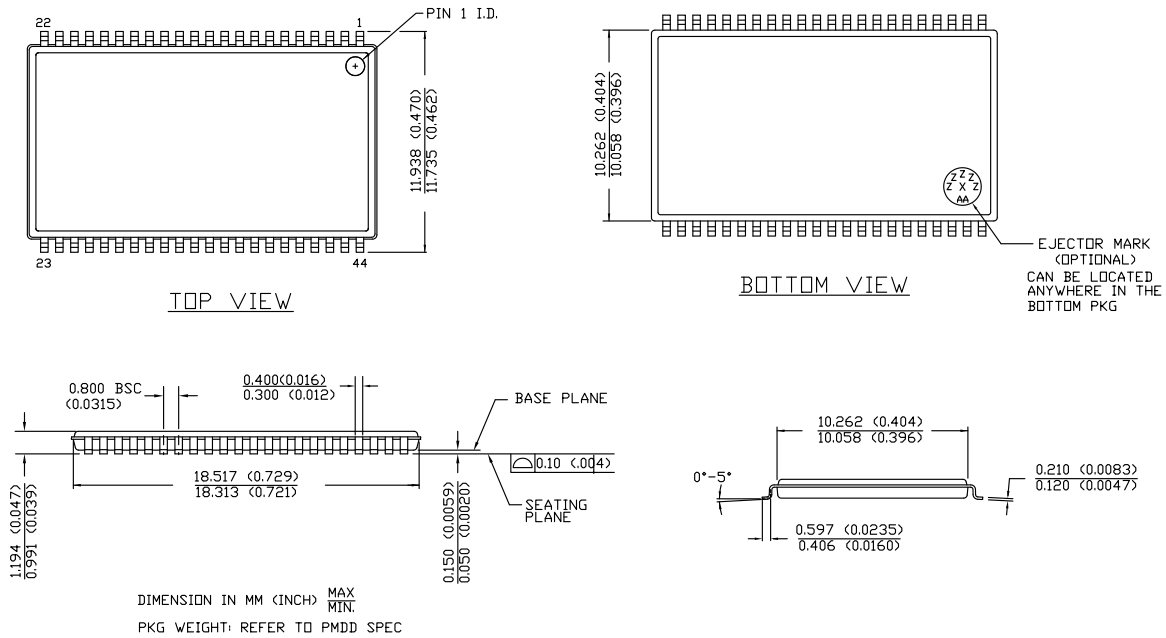
All the mentioned parts are Pb-free.

Ordering Code Definitions



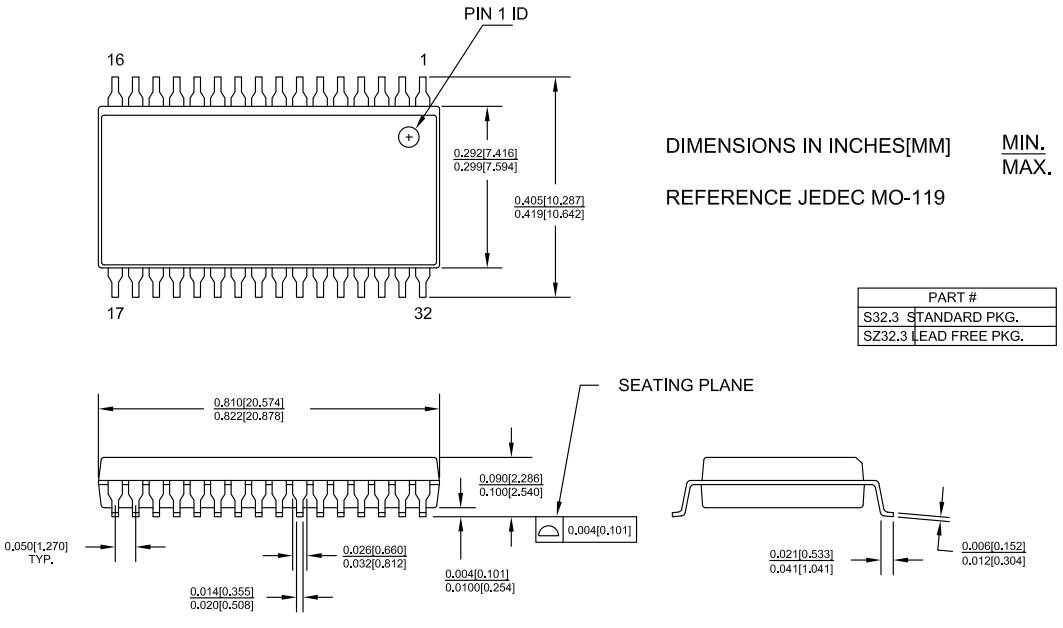
Package Diagrams

Figure 13. 44-pin TSOP II Package Outline, 51-85087



51-85087 *E

Figure 14. 32-pin SOIC (300 Mil) Package Outline, 51-85127



51-85127 *C

Acronyms

Acronym	Description
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
EIA	electronic industries alliance
$\overline{HSB}$	hardware store busy
I/O	input/output
JEDEC	joint electron devices engineering council
nvSRAM	non-volatile static random access memory
$\overline{OE}$	output enable
RoHS	restriction of hazardous substances
RWI	read and write inhibited
SOIC	small outline integrated circuit
SRAM	static random access memory
TSOP	thin small outline package
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY14E256LA, 256-Kbit (32 K × 8) nvSRAM Document Number: 001-54952				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2748216	GVCH / PYRS	08/04/09	New Datasheet
*A	2772059	GVCH	09/30/09	Updated Software STORE, RECALL and Autostore Enable, Disable soft sequence
*B	2829117	GVCH	12/16/09	Updated STORE cycles to QuantumTrap from 200K to 1 Million Added Contents. Moved to external web.
*C	2891356	GVCH	03/12/10	Removed inactive parts from Ordering Information table. Updated links in Sales, Solutions, and Legal Information.
*D	2922858	GVCH	04/26/10	Table 1: Added more clarity on $\overline{HSB}$ pin operation Hardware STORE Operation: Added more clarity on $\overline{HSB}$ pin operation Updated $\overline{HSB}$ pin operation in Figure 8 and updated footnote 21 Updated package diagram 51-85087
*E	3030490	GVCH	09/15/10	Change: I_{SB} and I_{CC4} max value from 5 mA to 8 mA. Areas affected: DC Electrical Characteristics on page 7. Change: Template and styles update. Areas affected: Entire datasheet
*F	3143330	GVCH	01/17/2011	Fixed typo in Figure 8.
*G	3219793	GVCH	04/08/2011	Logic Block Diagram: Fixed typo
*H	3315247	GVCH	07/15/2011	Updated DC Electrical Characteristics (Added Note 11 and referred the same note in V_{CAP} parameter). Updated Capacitance (Included Input capacitance (for $\overline{HSB}$) and Output capacitance (for $\overline{HSB}$)). Updated AC Switching Characteristics (Added Note 14 and referred the same note in Parameters).
*I	3660776	GVCH	06/29/2012	Updated DC Electrical Characteristics (Added V_{VCAP} parameter and its details, added Note 12 and referred the same note in V_{VCAP} parameter, also referred Note 13 in V_{VCAP} parameter). Updated Package Diagrams (spec 51-85127 (Changed revision from *B to *C)).
*J	3759425	GVCH	09/28/2012	Updated Maximum Ratings (Removed “Ambient temperature with power applied” and included “Maximum junction temperature”). Updated Package Diagrams (spec 51-85087 (Changed revision from *D to *E)).
*K	4568935	GVCH	11/14/2014	Added documentation related hyperlink in page 1

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