

CAT661

Typical Application

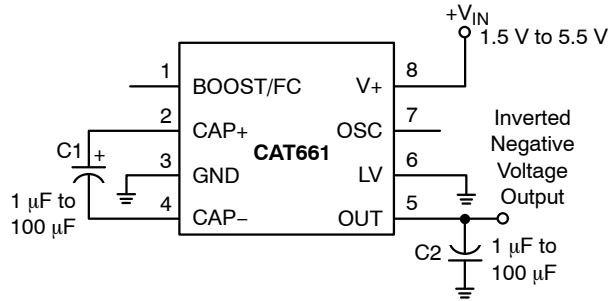


Figure 1. Voltage Inverter

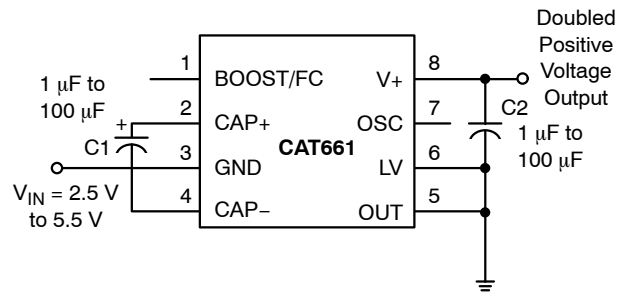


Figure 2. Positive Voltage Doubler

Table 1. PIN DESCRIPTIONS

| Pin Number | Name | Circuit Configuration | |
|------------|----------|--|---|
| | | Inverter Mode | Doubler Mode |
| 1 | Boost/FC | Frequency Control for the internal oscillator. With an external oscillator BOOST/FC has no effect. | |
| | | Boost/FC | Oscillator Frequency |
| | | Open | 25 kHz typical, 10 kHz minimum |
| | | V+ | 135 kHz typical, 80 kHz minimum |
| 2 | CAP+ | Charge Pump Capacitor. Positive terminal. | Same as inverter. |
| 3 | GND | Power Supply Ground. | Power supply. Positive voltage input. |
| 4 | CAP- | Charge pump capacitor. Negative terminal. | Same as inverter. |
| 5 | OUT | Output for negative voltage. | Power supply ground. |
| 6 | LV | Low-Voltage selection pin. When the input voltage is less than 3 V, connect LV to GND. For input voltages above 3 V, LV may be connected to GND or left open. If OSC is driven externally, connect LV to GND. | LV must be tied to OUT for all input voltages. |
| 7 | OSC | Oscillator control input. An external capacitor can be connected to lower the oscillator frequency. An external oscillator can drive OSC and set the chip operating frequency. The charge-pump frequency is one-half the frequency at OSC. | Same as inverter. Do not overdrive OSC in doubling mode. Standard logic levels will not be suitable. See the applications section for additional information. |
| 8 | V+ | Power supply. Positive voltage input. | Positive voltage output. |

Table 2. ABSOLUTE MAXIMUM RATINGS

| Parameters | Ratings | Units |
|--|---|---------------|
| V+ to GND | 6 | V |
| Input Voltage (Pins 1, 6 and 7) | -0.3 to (V+ + 0.3) | V |
| BOOST/FC and OSC Input Voltage | The least negative of (Out - 0.3 V) or (V+ - 6 V) to (V+ + 0.3 V) | V |
| Output Short-circuit Duration to GND (OUT may be shorted to GND for 1 sec without damage but shorting OUT to V+ should be avoided.) | 1 | sec. |
| Continuous Power Dissipation (T _A = 70°C) Plastic DIP SO TDFN | 730 500 1 | mW mW W |
| Storage Temperature | -65 to +160 | °C |
| Lead Soldering Temperature (10 sec) | 300 | °C |
| ESD Rating - Human Body Model | 2000 | V |
| Operating Ambient Temperature Range | -40 to +85 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: T_A = Ambient Temperature

Table 3. ELECTRICAL CHARACTERISTICS (V+ = 5 V, C1 = C2 = 100 µF, Boost/FC = Open, C_{OSC} = 0 pF, and Test Circuit is Figure 3 unless otherwise noted. Temperature is T_A = T_{AMIN} to T_{AMAX} unless otherwise noted.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|----------------------------------|--------|---|-----|-----------|-----|-------|
| Supply Voltage | VS | Inverter: LV = Open, R _L = 1 kΩ | 3.0 | | 5.5 | V |
| | | Inverter: LV = GND, R _L = 1 kΩ | 1.5 | | 5.5 | |
| | | Doubler: LV = OUT, R _L = 1 kΩ | 2.5 | | 5.5 | |
| Supply Current | IS | BOOST/FC = open, LV = Open | | 0.2 | 0.5 | mA |
| | | BOOST/FC = V+, LV = Open | | 1 | 3 | |
| Output Current | IOUT | OUT is more negative than -4 V | 100 | | | mA |
| Output Resistance | RO | C1 = C2 = 10 µF BOOST/FC = V+ (C1, C2 ESR ≤ 0.5 Ω) | | 3.5 | 10 | Ω |
| | | C1 = C2 = 100 µF (Note 2) | | 3.5 | 10 | |
| Oscillator Frequency (Note 3) | FOSC | BOOST/FC = Open | 10 | 25 | | kHz |
| | | BOOST/FC = V+ | 80 | 135 | | |
| OSC Input Current | IOSC | BOOST/FC = Open BOOST/FC = V+ | | ±2 ±10 | | µA |
| Power Efficiency | PE | R _L = 1 kΩ connected between V+ and OUT, T _A = 25°C (Doubler) | 96 | 98 | | % |
| | | R _L = 500 Ω connected between GND and OUT, T _A = 25°C (Inverter) | 92 | 96 | | |
| | | I _L = 100 mA to GND, T _A = 25°C (Inverter) | | 88 | | |
| Voltage Conversion Efficiency | VEFF | No load, T _A = 25°C | 99 | 99.9 | | % |

1. In Figure 3, test circuit electrolytic capacitors C1 and C2 are 100 µF and have 0.2 Ω maximum ESR. Higher ESR levels may reduce efficiency and output voltage.
2. The output resistance is a combination of the internal switch resistance and the external capacitor ESR. For maximum voltage and efficiency keep external capacitor ESR under 0.2 Ω.
3. FOSC is tested with C_{OSC} = 100 pF to minimize test fixture loading. The test is correlated back to C_{OSC} = 0 pF to simulate the capacitance at OSC when the device is inserted into a test socket without an external C_{OSC}.

CAT661

Voltage Inverter

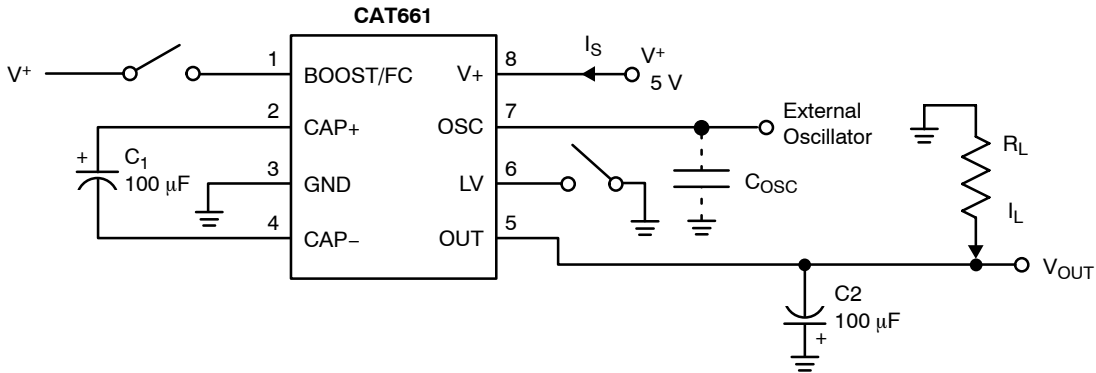


Figure 3. Test Circuit Voltage Inverter

TYPICAL OPERATING CHARACTERISTICS

(Typical characteristic curves are generated using the test circuit in Figure 3. Inverter test conditions are: $V_+ = 5\text{ V}$, $LV = \text{GND}$, $\text{BOOST/FC} = \text{Open}$ and $T_A = 25^\circ\text{C}$ unless otherwise indicated. Note that the charge-pump frequency is one-half the oscillator frequency.)

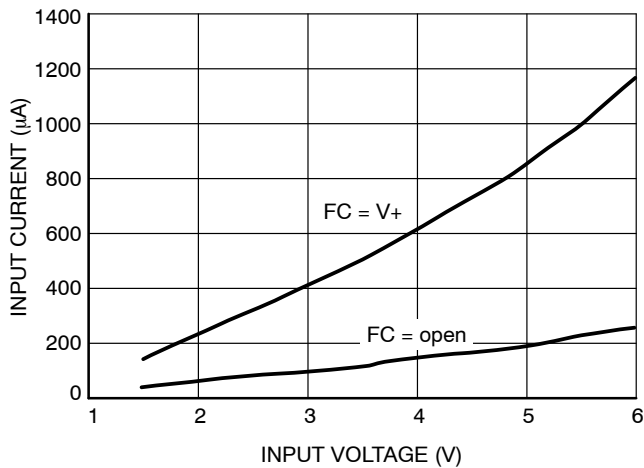


Figure 4. Supply Current vs. Input Voltage

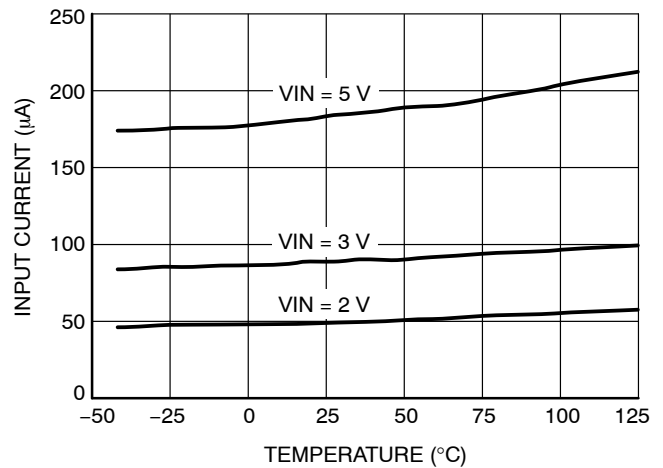


Figure 5. Supply Current vs. Temperature (No Load)

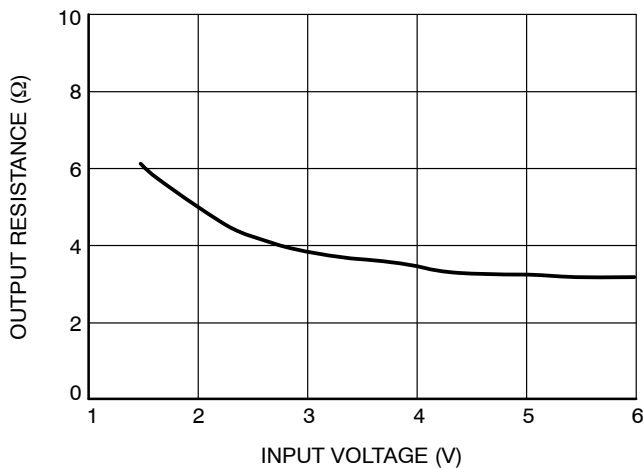


Figure 6. Output Resistance vs. Input Voltage

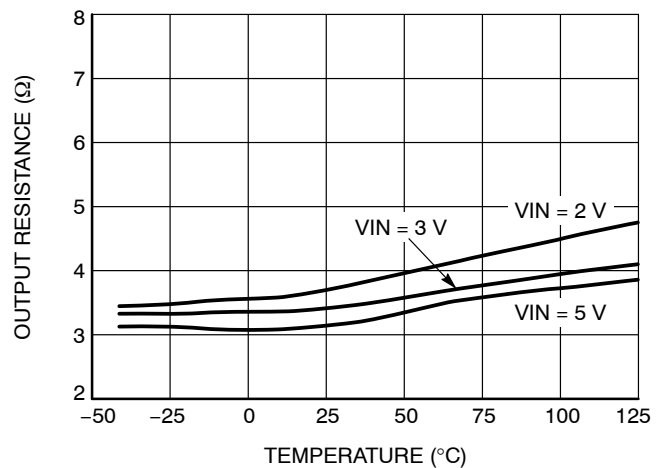


Figure 7. Output Resistance vs. Temperature (50 Ω Load)

TYPICAL OPERATING CHARACTERISTICS

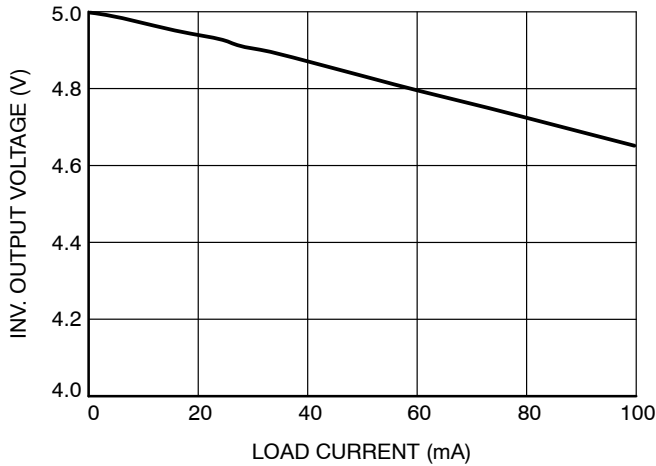


Figure 8. Inverted Output Voltage vs. Load, $V_+ = 5\text{ V}$

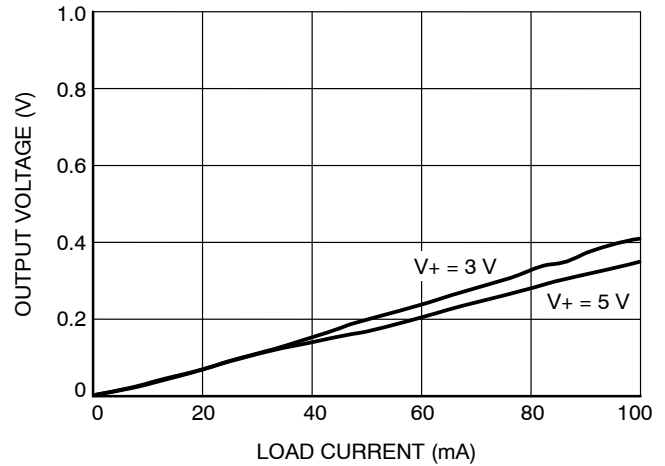


Figure 9. Output Voltage Drop vs. Load Current

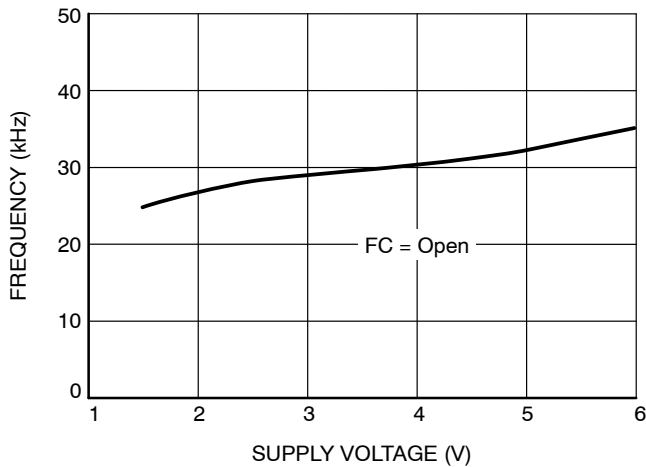


Figure 10. Oscillator Frequency vs. Supply Voltage

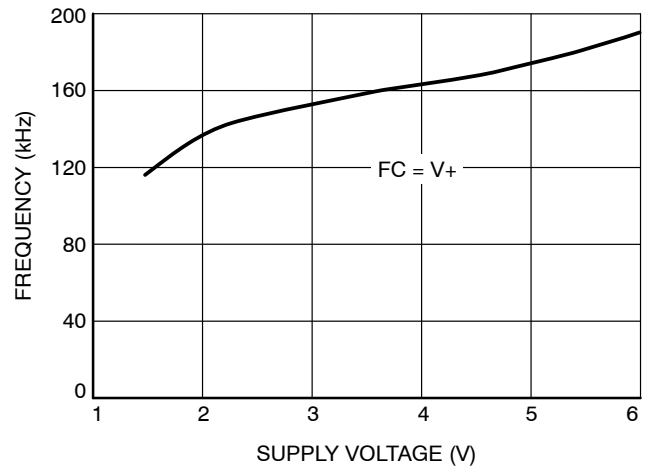


Figure 11. Oscillator Frequency vs. Supply Voltage

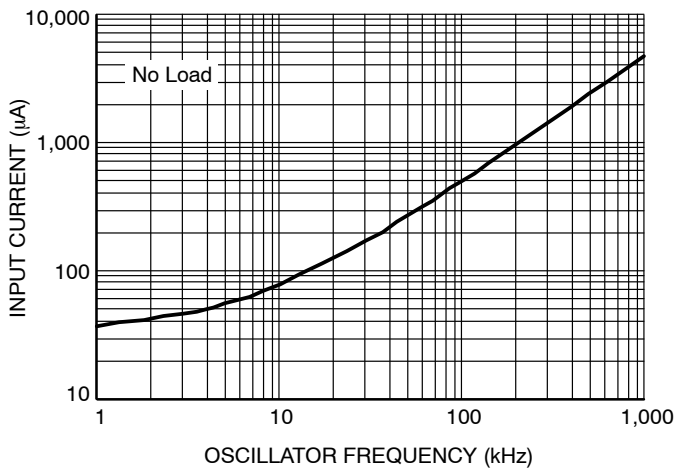


Figure 12. Supply Current vs. Oscillator Frequency

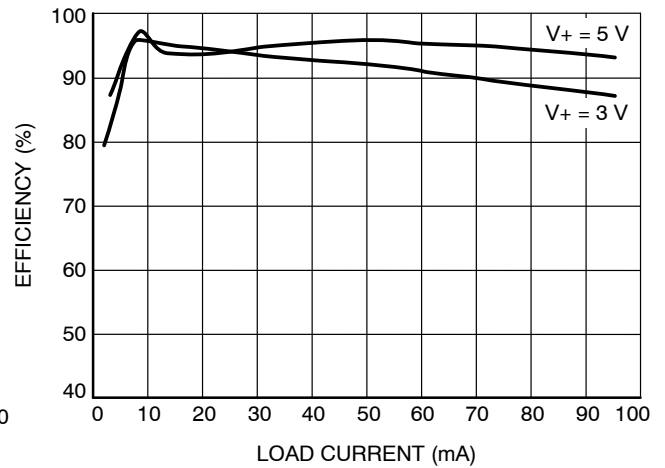


Figure 13. Efficiency vs. Load Current

CAT661

Voltage Doubler

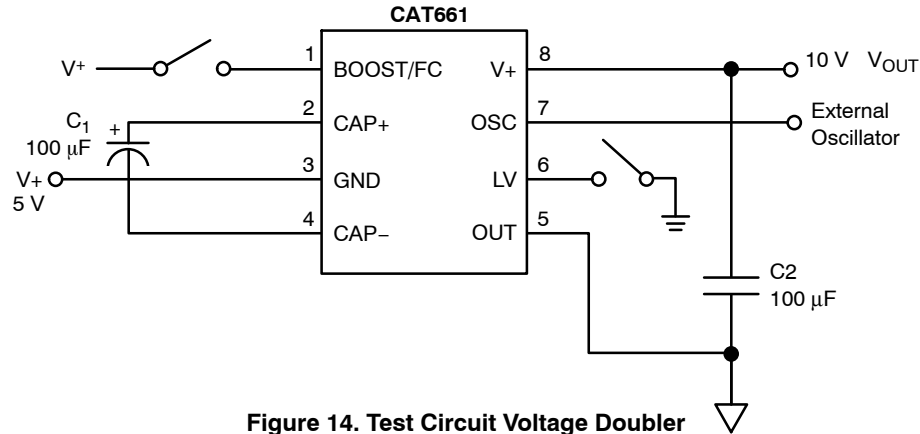


Figure 14. Test Circuit Voltage Doubler

TYPICAL OPERATING CHARACTERISTICS

(Typical characteristic curves are generated using the circuit in Figure 14. Doubler test conditions are: $V_+ = 5\text{ V}$, $LV = \text{GND}$, $\text{BOOST/FC} = \text{Open}$ and $T_A = 25^\circ\text{C}$ unless otherwise indicated.)

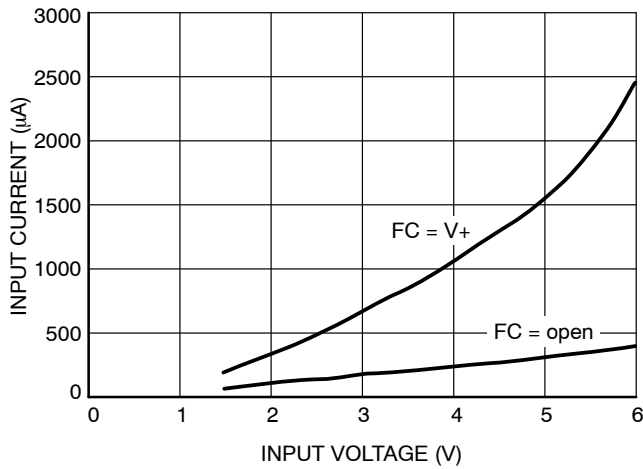


Figure 15. Supply Current vs. Input Voltage (No Load)

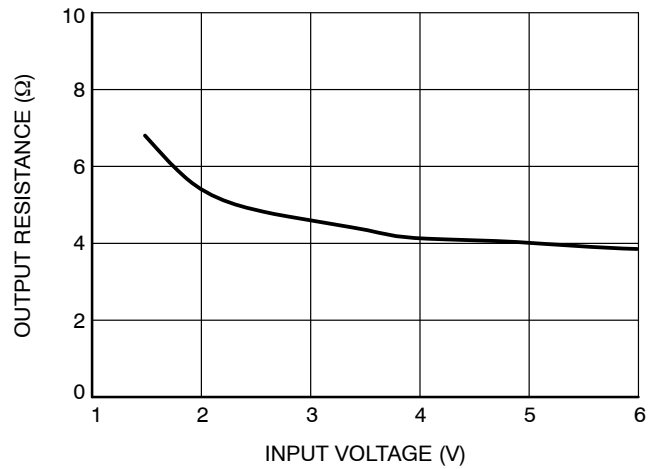


Figure 16. Output Resistance vs. Input Voltage

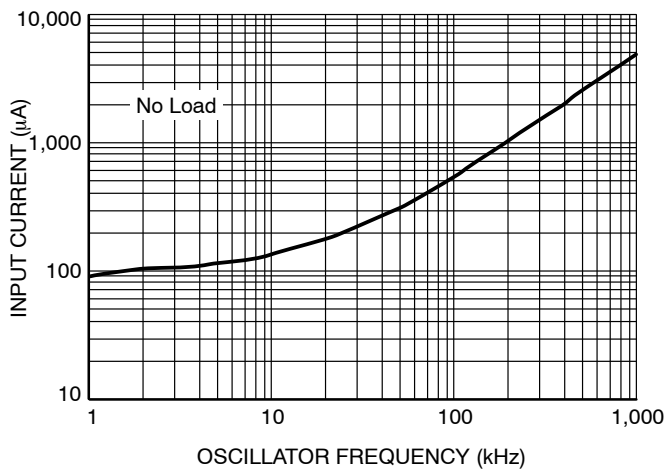


Figure 17. Supply Current vs. Oscillator Frequency

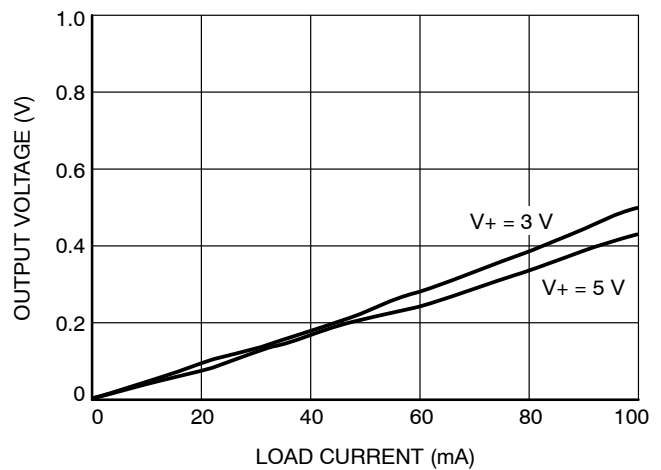


Figure 18. Output Voltage Drop vs. Load Current

Application Information

Circuit Description and Operating Theory

The CAT661 switches capacitors to invert or double an input voltage.

Figure 19 shows a simple switch capacitor circuit. In position 1 capacitor C1 is charged to voltage V1. The total charge on C1 is $Q1 = C1V1$. When the switch moves to position 2, the input capacitor C1 is discharged to voltage V2. After discharge, the charge on C1 is $Q2 = C1V2$.

The charge transferred is:

$$\Delta Q = Q1 - Q2 = C1 \times (V1 - V2)$$

If the switch is cycled “F” times per second, the current (charge transfer per unit time) is:

$$I = F \times \Delta Q = F \times C1 (V1 - V2)$$

Rearranging in terms of impedance:

$$I = \frac{(V1 - V2)}{(1/FC1)} = \frac{V1 - V2}{REQ}$$

The $1/FC1$ term can be modeled as an equivalent impedance REQ. A simple equivalent circuit is shown in

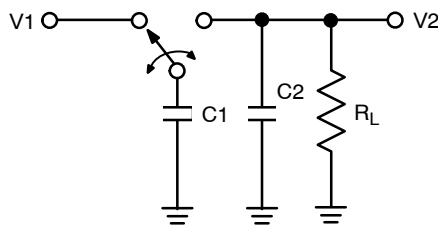


Figure 19. Switched-Capacitor Building Block

Figure 20. This circuit does not include the switch resistance nor does it include output voltage ripple. It does allow one to understand the switch-capacitor topology and make prudent engineering tradeoffs.

For example, power conversion efficiency is set by the output impedance, which consists of REQ and switch resistance. As switching frequency is decreased, REQ, the $1/FC1$ term, will dominate the output impedance, causing higher voltage losses and decreased efficiency. As the frequency is increased quiescent current increases. At high frequency this current becomes significant and the power efficiency degrades.

The oscillator is designed to operate where voltage losses are a minimum. With external 150 μ F capacitors, the internal switch resistances and the Equivalent Series Resistance (ESR) of the external capacitors determine the effective output impedance.

A block diagram of the CAT661 is shown in Figure 21.

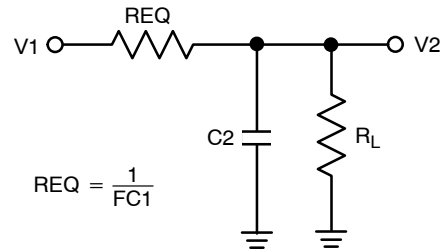


Figure 20. Switched-Capacitor Equivalent Circuit

Oscillator Frequency Control

The switching frequency can be raised, lowered or driven from an external source. Figure 22 shows a functional diagram of the oscillator circuit.

The CAT661 oscillator has four control modes:

Table 4.

| BOOST/FC Pin Connection | OSC Pin Connection | Nominal Oscillator Frequency |
|------------------------------------|-------------------------------|---|
| Open | Open | 25 kHz |
| BOOST/FC = V+ | Open | 135 kHz |
| Open or BOOST/FC = V+ | External Capacitor | – |
| Open | External Clock | Frequency of external clock |

If BOOST/FC and OSC are left floating (Open), the nominal oscillator frequency is 25 kHz. The pump frequency is one-half the oscillator frequency.

By connecting the BOOST/FC pin to V+, the charge and discharge currents are increased, and the frequency is increased by approximately 6 times. Increasing the frequency will decrease the output impedance and ripple currents. This can be an advantage at high load currents. Increasing the frequency raises quiescent current but allows smaller capacitance values for C1 and C2.

If pin 7, OSC, is loaded with an external capacitor the frequency is lowered. By using the BOOST/FC pin and an external capacitor at OSC, the operating frequency can be set.

Note that the frequency appearing at CAP+ or CAP- is one-half that of the oscillator.

Driving the CAT661 from an external frequency source can be easily achieved by driving Pin 7 and leaving the BOOST pin open, as shown in Figure 22. The output current from Pin 7 is small, typically 1 μA to 8 μA , so a CMOS can drive the OSC pin. For 5 V applications, a TTL logic gate can be used if an external 100 k Ω pull-up resistor is used as shown in Figure 23.

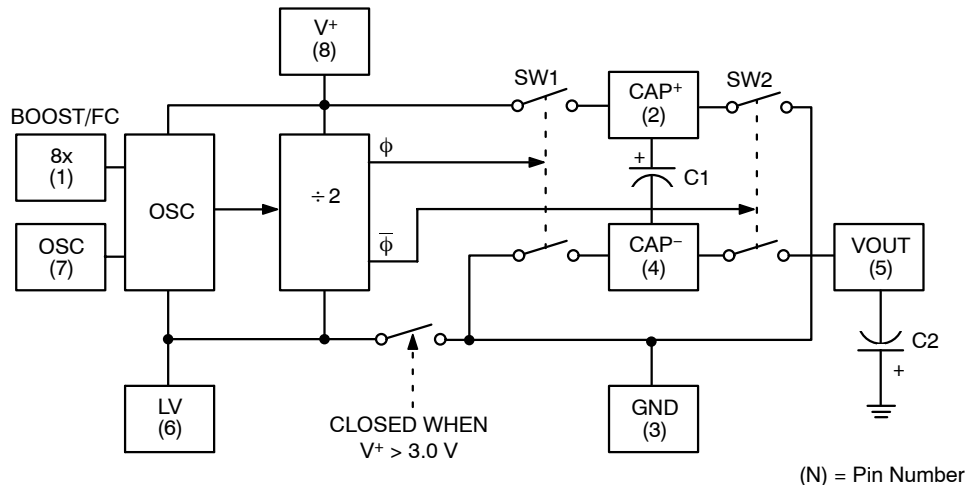


Figure 21. CAT661 Block Diagram

Capacitor Selection

Low ESR capacitors are necessary to minimize voltage losses, especially at high load currents. The exact values of C1 and C2 are not critical but low ESR capacitors are necessary.

The ESR of capacitor C1, the pump capacitor, can have a pronounced effect on the output. C1 currents are approximately twice the output current and losses occur on both the charge and discharge cycle. The ESR effects are thus multiplied by four. A 0.5 Ω ESR for C1 will have the same effect as a 2 Ω increase in CAT661 output impedance.

Output voltage ripple is determined by the value of C2 and the load current. C2 is charged and discharged at a current roughly equal to the load current. The internal switching frequency is one-half the oscillator frequency.

$$VRIPPLE = I_{OUT} / (F_{OSC} \times C2) + I_{OUT} \times ESR_{C2}$$

For example, with a 25 kHz oscillator frequency (12.5 kHz switching frequency), a 150 μ F C2 capacitor with an ESR of 0.2 Ω and a 100 mA load peak-to-peak ripple voltage is 45 mV.

Table 5. VRIPPLE vs. FOSC

| VRIPPLE (mV) | IOUT (mA) | FOSC (kHz) | C2 (μ F) | C2 ESR (Ω) |
|--------------|-----------|------------|---------------|---------------------|
| 45 | 100 | 25 | 150 | 0.2 |
| 25 | 100 | 135 | 150 | 0.2 |

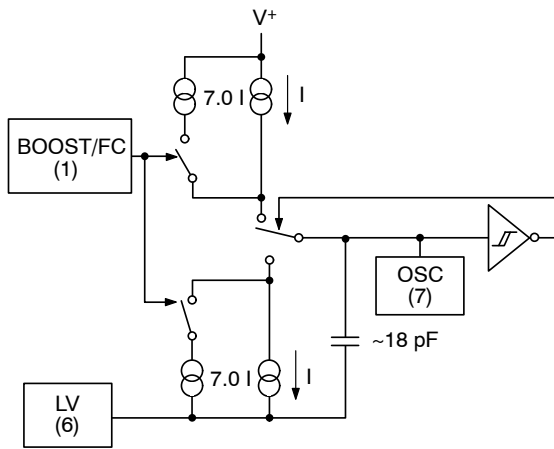


Figure 22. Oscillator

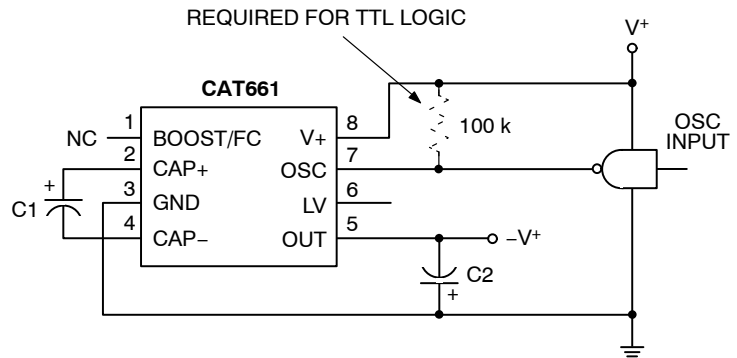


Figure 23. External Clocking

CAT661

Capacitor Suppliers

The following manufacturers supply low-ESR capacitors:

Table 6. CAPACITOR SUPPLIERS

| Manufacturer | Capacitor Type | Phone | WEB | Email | Comments |
|----------------|----------------|--------------|---------------------|--------------------|----------|
| AVX/Kyocera | TPS/TPS3 | 843-448-9411 | www.avxcorp.com | avx@avxcorp.com | Tantalum |
| Vishay/Sprague | 595 | 402-563-6866 | www.vishay.com | - | Aluminum |
| Sanyo | MV-AX, UGX | 619-661-6835 | www.sanyo.com | Svcsales@sanyo.com | Aluminum |
| Nichicon | F55 | 847-843-7500 | www.nichicon-us.com | - | Tantalum |
| | HC/HD | | | | Aluminum |

Capacitor manufacturers continually introduce new series and offer different package styles. It is recommended that before a design is finalized capacitor manufacturers should be surveyed for their latest product offerings.

Controlling Loss in CAT661 Applications

There are three primary sources of voltage loss:

1. Output resistance:

$V_{LOSS} = I_{LOAD} \times R_{OUT}$, where R_{OUT} is the CAT661 output resistance and I_{LOAD} is the load current.

2. Charge pump (C1) capacitor ESR:

$V_{LOSSC1} \approx 4 \times E_{SRC1} \times I_{LOAD}$, where E_{SRC1} is the ESR of capacitor C1.

3. Output or reservoir (C2) capacitor ESR:

$V_{LOSSC2} = E_{SRC2} \times I_{LOAD}$, where E_{SRC2} is the ESR of capacitor C2.

Increasing the value of C2 and/or decreasing its ESR will reduce noise and ripple.

The effective output impedance of a CAT661 circuit is approximately:

$$R_{circuit} \approx R_{out\ 661} + (4 \times E_{SRC1}) + E_{SRC2}$$

CAT661

Typical Applications

Voltage Inversion Positive-to-Negative

The CAT661 easily provides a negative supply voltage from a positive supply in the system. Figure 24 shows a typical circuit. The LV pin may be left floating for positive input voltages at or above 3.3 V.

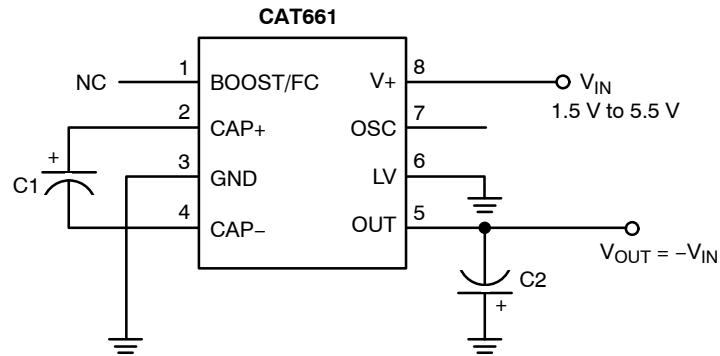
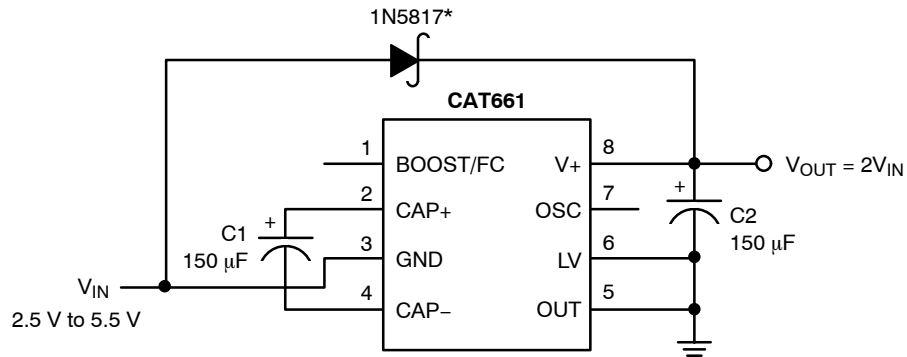


Figure 24. Voltage Inverter

Positive Voltage Doubler

The voltage doubler circuit shown in Figure 25 gives $V_{OUT} = 2 \times V_{IN}$ for input voltages from 2.5 V to 5.5 V.



*SCHOTTKY DIODE IS FOR START-UP ONLY

Figure 25. Voltage Doubler

CAT661

Precision Voltage Divider

A precision voltage divider is shown in Figure 26. With load currents under 100 nA, the voltage at pin 2 will be within 0.002% of $V^+/2$.

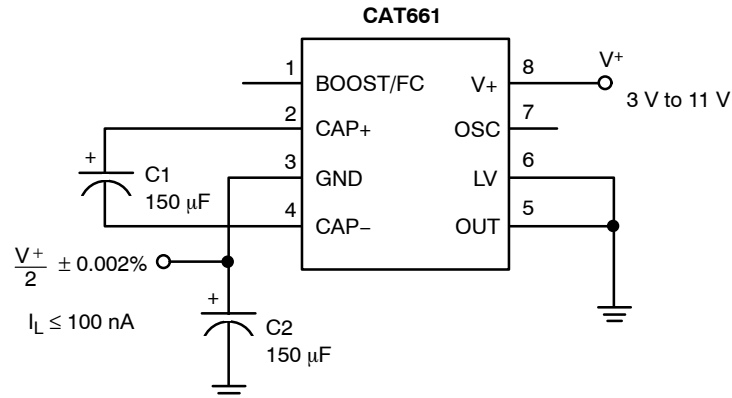


Figure 26. Precision Voltage Divider (Load ≤ 100 nA)

Battery Voltage Splitter

Positive and negative voltages that track each other can be obtained from a battery. Figure 27 shows how a 9 V battery can provide symmetrical positive and negative voltages equal to one-half the battery voltage.

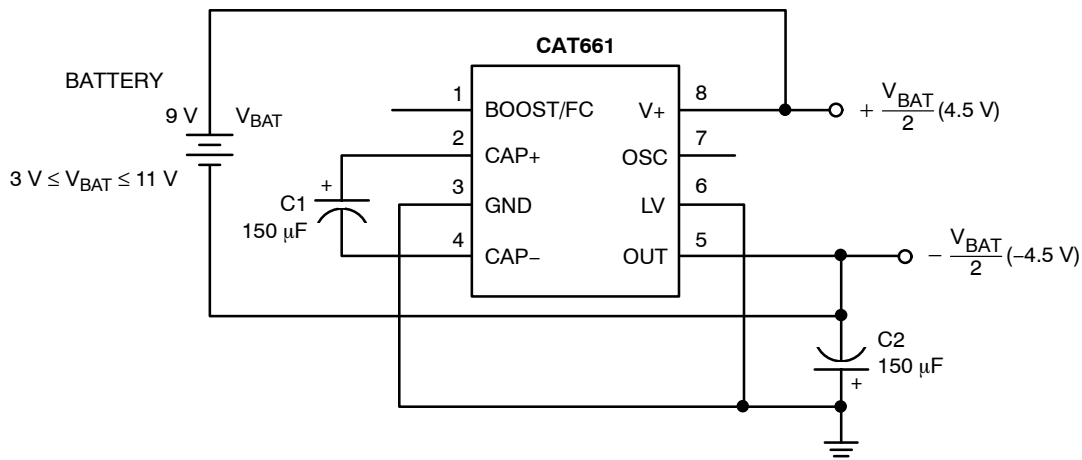


Figure 27. Battery Splitter

CAT661

Cascade Operation for Higher Negative Voltages

The CAT661 can be cascaded as shown in Figure 28 to generate more negative voltage levels. The output resistance is approximately the sum of the individual CAT661 output resistance.

$V_{OUT} = -N \times V_{IN}$, where N represents the number of cascaded devices.

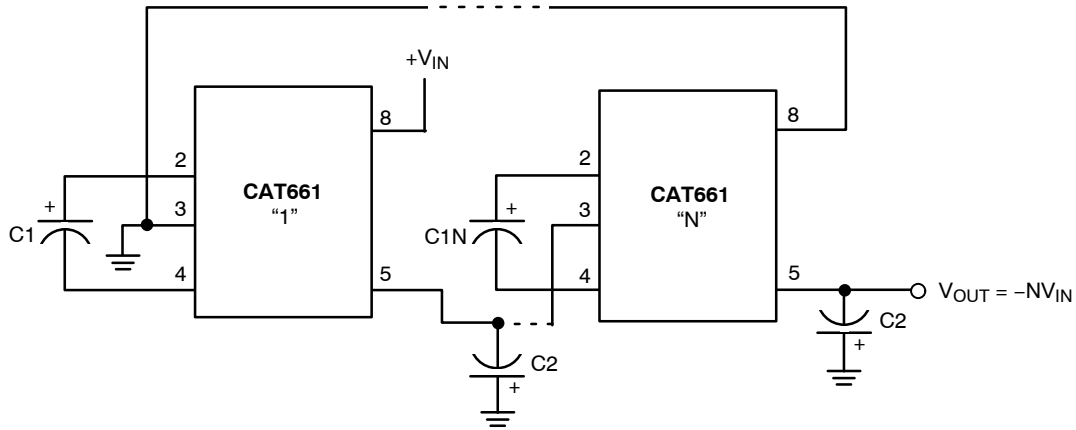


Figure 28. Cascading to Increase Output Voltage

Parallel Operation

Paralleling CAT661 devices will lower output resistance. As shown in Figure 29, each device requires its own pump capacitor, $C2$, but the output reservoir capacitor is shared with all devices. The value of $C2$ should be increased by a factor of N, where N is the number of devices.

$$R_{OUT} = \frac{R_{OUT} \text{ (of CAT661)}}{N \text{ (NUMBER OF DEVICES)}}$$

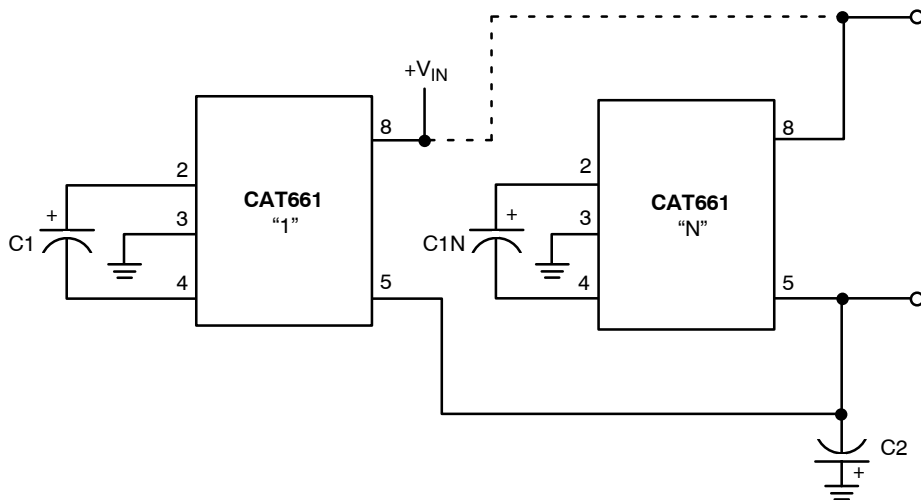
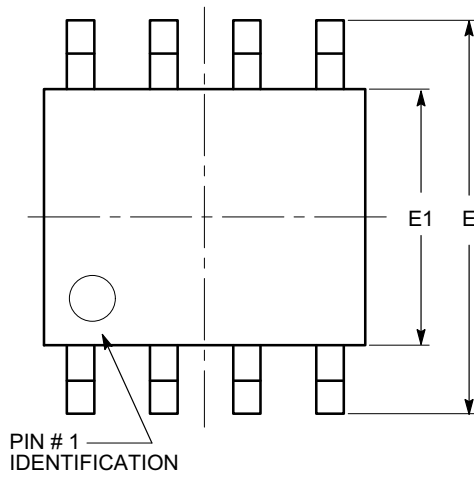


Figure 29. Reduce Output Resistance BY Paralleling Devices

CAT661

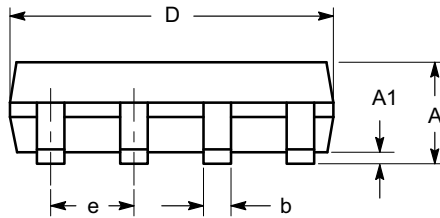
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD-01
ISSUE O

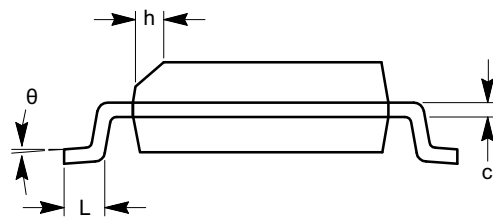


TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|----------|----------|-----|------|
| A | 1.35 | | 1.75 |
| A1 | 0.10 | | 0.25 |
| b | 0.33 | | 0.51 |
| c | 0.19 | | 0.25 |
| D | 4.80 | | 5.00 |
| E | 5.80 | | 6.20 |
| E1 | 3.80 | | 4.00 |
| e | 1.27 BSC | | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| θ | 0° | | 8° |



SIDE VIEW



END VIEW

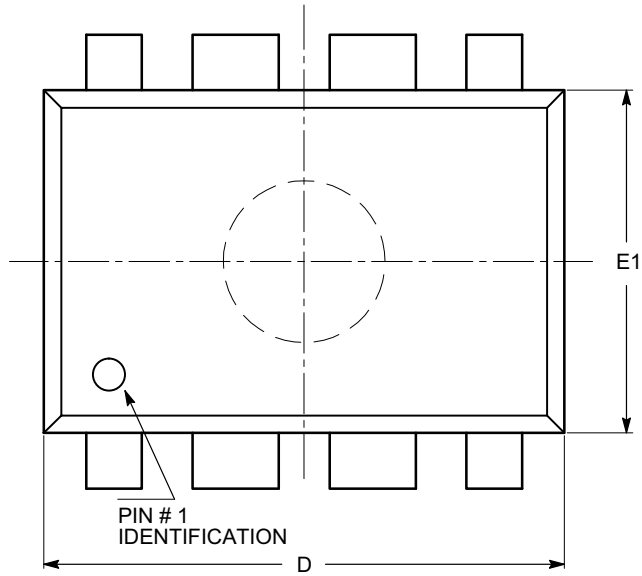
Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

CAT661

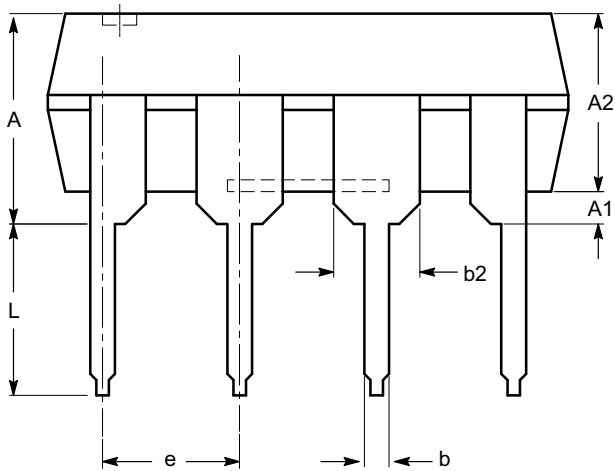
PACKAGE DIMENSIONS

PDIP-8, 300 mils
CASE 646AA-01
ISSUE A

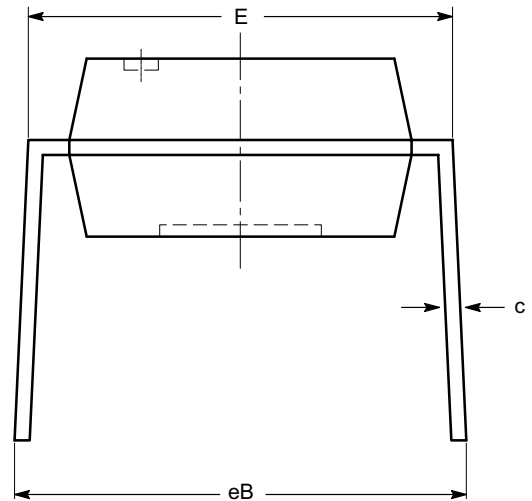


TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|--------|----------|------|-------|
| A | | | 5.33 |
| A1 | 0.38 | | |
| A2 | 2.92 | 3.30 | 4.95 |
| b | 0.36 | 0.46 | 0.56 |
| b2 | 1.14 | 1.52 | 1.78 |
| c | 0.20 | 0.25 | 0.36 |
| D | 9.02 | 9.27 | 10.16 |
| E | 7.62 | 7.87 | 8.25 |
| E1 | 6.10 | 6.35 | 7.11 |
| e | 2.54 BSC | | |
| eB | 7.87 | | 10.92 |
| L | 2.92 | 3.30 | 3.80 |



SIDE VIEW



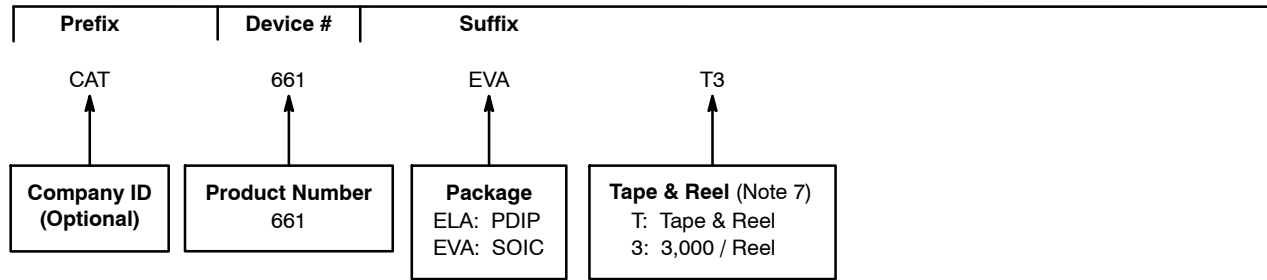
END VIEW

Notes:


- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MS-001.

CAT661

Example of Ordering Information (Note 6)



4. All packages are RoHS-compliant (Lead-free, Halogen-free).
5. The standard lead finish is Matte-Tin.
6. The device used in the above example is a CAT661EVA-T3 (SOIC, Tape & Reel, 3,000/Reel).
7. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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