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REVISION HISTORY

12/11—Rev. A to Rev. B

Changes to Features Section ... 1
Changes to Rate Sensitive Axis Section ... 4
Deleted Endnote 1, Table 3 ... 4
Deleted Figure 5; Renumbered Sequentially ... 6
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Deleted Figure 36 ... 26

6/11—Rev. 0 to Rev. A

Changes to Bit 30 and Bit 31 in Table 9 ... 14
Updated Outline Dimensions ... 29
Changes to Ordering Guide ... 30

1/11—Revision 0: Initial Version

SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, P_{DD} = 5 V, angular rate = 0°/sec, bandwidth = $f_0/200$ (~77.5 Hz), ±1 *g*, continuous self-test on.

Table 1.

Parameter	Test Conditions/Comments	Symbol	Min	Typ	Max	Unit
MEASUREMENT RANGE	Full-scale range	FSR	±300		±400	°/sec
SENSITIVITY	See Figure 2					
Nominal Sensitivity				80		LSB/°/sec
Sensitivity Tolerance	T_A = −40°C to +105°C		−3		+3	%
Nonlinearity[1]	Best fit straight line			0.05		% FSR rms
Cross-Axis Sensitivity[2]			−3		+3	%
NULL ACCURACY	T_A = 25°C			±0.4		°/sec
	T_A = −40°C to +105°C			±0.5		°/sec
NOISE PERFORMANCE						
Rate Noise Density	T_A = 25°C			0.015		°/sec/√Hz
	T_A = 105°C			0.023		°/sec/√Hz
LOW-PASS FILTER						
Cutoff (−3 dB) Frequency	$f_0/200$	f_{LP}		77.5		Hz
Group Delay[3]	f = 0 Hz	t_{LP}	3.25	4	4.75	ms
SENSOR RESONANT FREQUENCY		f_0	13	15.5	19	kHz
SHOCK AND VIBRATION IMMUNITY						
Sensitivity to Linear Acceleration	DC to 5 kHz			0.01		°/sec/*g*
Vibration Rectification				0.0002		°/sec/g^2
SELF-TEST	See the Continuous Self-Test section					
Magnitude				2559		LSB
Fault Register Threshold	Compared to LOCSTx register data		2239		2879	LSB
Sensor Data Status Threshold	Compared to LOCSTx register data		1279		3839	LSB
Frequency	$f_0/32$	f_{ST}		485		Hz
ST Low-Pass Filter						
Cutoff (−3 dB) Frequency	$f_0/8000$			1.95		Hz
Group Delay[3]			52	64	76	ms
SPI COMMUNICATIONS						
Clock Frequency					8.08	MHz
Voltage Input High	MOSI, $\overline{CS}$, SCLK		0.85 × P_{DD}		P_{DD} + 0.3	V
Voltage Input Low	MOSI, $\overline{CS}$, SCLK		−0.3		P_{DD} × 0.15	V
Voltage Output Low	MISO, current = 3 mA				0.5	V
Voltage Output High	MISO, current = −2 mA		P_{DD} − 0.5			V
Pull-Up Current	$\overline{CS}$, P_{DD} = 3.3 V, $\overline{CS}$ = P_{DD} × 0.15			60	200	µA
	$\overline{CS}$, P_{DD} = 5 V, $\overline{CS}$ = P_{DD} × 0.15			80	300	µA
MEMORY REGISTERS	See the Memory Register Definitions section					
Temperature Register						
Value at 45°C				0		LSB
Scale Factor				5		LSB/°C
Quadrature, Self-Test, and Rate Registers						
Scale Factor				80		LSB/°/sec
POWER SUPPLY						
Supply Voltage		P_{DD}	3.15		5.25	V
Quiescent Supply Current		I_{DD}		6.0	8.0	mA
Turn-On Time	Power-on to 0.5°/sec of final value			100		ms

[1] Maximum limit is guaranteed by Analog Devices, Inc., characterization.
[2] Cross-axis sensitivity specification does not include effects due to device mounting on a printed circuit board (PCB).
[3] Minimum and maximum limits are guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Acceleration (Any Axis, 0.5 ms)	
Unpowered	2000 *g*
Powered	2000 *g*
Supply Voltage (P_{DD})	−0.3 V to +6.0 V
Output Short-Circuit Duration (Any Pin to Ground)	Indefinite
Operating Temperature Range	
LCC_V Package	−55°C to +125°C
SOIC_CAV Package	−40°C to +125°C
Storage Temperature Range	
LCC_V Package	−65°C to +150°C
SOIC_CAV Package	−40°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, for a device soldered in a printed circuit board (PCB) for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
16-Lead SOIC_CAV (RG-16-1)	191.5	25	°C/W
14-Lead Ceramic LCC_V (EY-14-1)	185.5	23	°C/W

RATE SENSITIVE AXIS

The ADXRS453 is available in two package options.

- The SOIC_CAV package is for applications that require z-axis (yaw) rate sensing.
- The LCC_V (vertical mount) package is for applications that require x-axis or y-axis (pitch or roll) rate sensing. The package has terminals on two faces. However, the terminals on the back are for internal evaluation only and should not be used in the end application. The terminals on the bottom of the package incorporate metallization bumps that ensure a minimum solder thickness for improved solder joint reliability. These bumps are not present on the back terminals and, therefore, poor solder joint reliability can be encountered if the back terminals are used in the end application. For the outline dimensions of this package, see Figure 38.

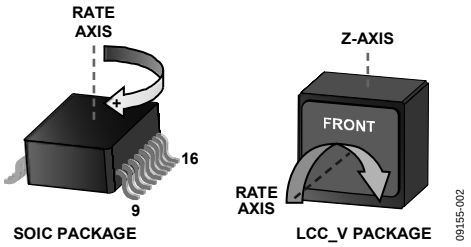


Figure 2. Rate Signal Increases with Clockwise Rotation

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

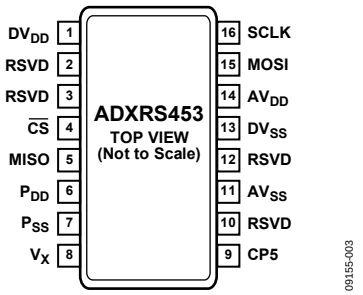
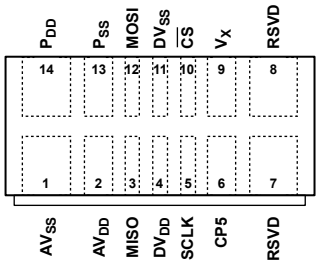


Figure 3. Pin Configuration, 16-Lead SOIC_CAV

Table 4. Pin Function Descriptions, 16-Lead SOIC_CAV

Pin No.	Mnemonic	Description
1	DV_{DD}	Digital Regulated Voltage. See Figure 25 for the application circuit diagram.
2	RSVD	Reserved. This pin must be connected to DV_{SS}.
3	RSVD	Reserved. This pin must be connected to DV_{SS}.
4	$\overline{CS}$	Chip Select.
5	MISO	Master In/Slave Out.
6	P_{DD}	Supply Voltage.
7	P_{SS}	Switching Regulator Ground.
8	V_X	High Voltage Switching Node. See Figure 25 for the application circuit diagram.
9	CP5	High Voltage Supply. See Figure 25 for the application circuit diagram.
10	RSVD	Reserved. This pin must be connected to DV_{SS}.
11	AV_{SS}	Analog Ground.
12	RSVD	Reserved. This pin must be connected to DV_{SS}.
13	DV_{SS}	Digital Signal Ground.
14	AV_{DD}	Analog Regulated Voltage. See Figure 25 for the application circuit diagram.
15	MOSI	Master Out/Slave In.
16	SCLK	SPI Clock.



NOTES
1. THE PACKAGE HAS TERMINALS ON TWO FACES. HOWEVER, THE TERMINALS ON THE BACK ARE FOR INTERNAL EVALUATION ONLY AND SHOULD NOT BE USED IN THE END APPLICATION. THE TERMINALS ON THE BOTTOM OF THE PACKAGE INCORPORATE METALLIZATION BUMPS THAT ENSURE A MINIMUM SOLDER THICKNESS FOR IMPROVED SOLDER JOINT RELIABILITY. THESE BUMPS ARE NOT PRESENT ON THE BACK TERMINALS AND, THEREFORE, POOR SOLDER JOINT RELIABILITY CAN BE ENCOUNTERED IF THE BACK TERMINALS ARE USED IN THE END APPLICATION. FOR THE OUTLINE DIMENSIONS OF THIS PACKAGE, SEE FIGURE 38.

09155-004

Figure 4. Pin Configuration, 14-Terminal LCC_V

Table 5. Pin Function Descriptions, 14-Terminal LCC_V

Pin No.	Mnemonic	Description
1	AV_{SS}	Analog Ground.
2	AV_{DD}	Analog Regulated Voltage. See Figure 26 for the application circuit diagram.
3	MISO	Master In/Slave Out.
4	DV_{DD}	Digital Regulated Voltage. See Figure 26 for the application circuit diagram.
5	SCLK	SPI Clock.
6	CP5	High Voltage Supply. See Figure 26 for the application circuit diagram.
7	RSVD	Reserved. This pin must be connected to DV_{SS}.
8	RSVD	Reserved. This pin must be connected to DV_{SS}.
9	V_X	High Voltage Switching Node. See Figure 26 for the application circuit diagram.
10	$\overline{CS}$	Chip Select.
11	DV_{SS}	Digital Signal Ground.
12	MOSI	Master Out/Slave In.
13	P_{SS}	Switching Regulator Ground.
14	P_{DD}	Supply Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

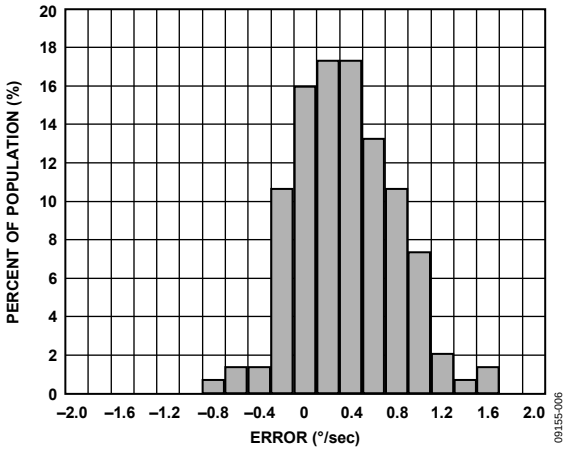


Figure 5. SOIC_CAV Null Accuracy at 25°C

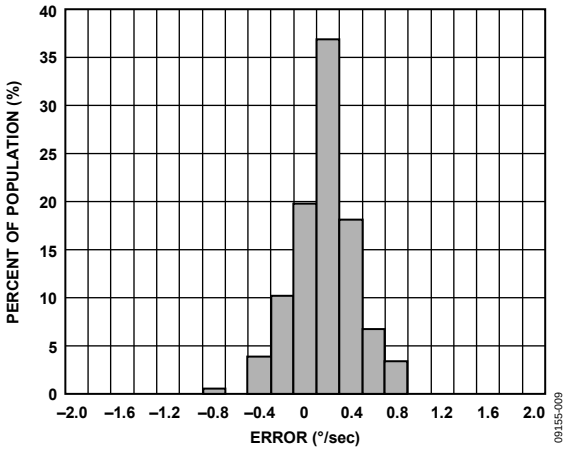


Figure 8. LCC_V Null Accuracy at 25°C

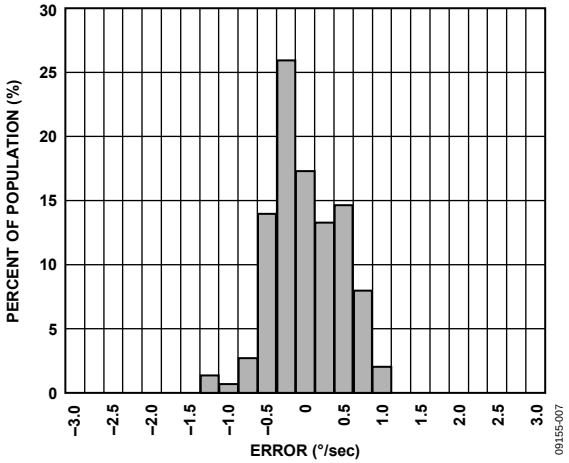


Figure 6. SOIC_CAV Null Drift over Temperature

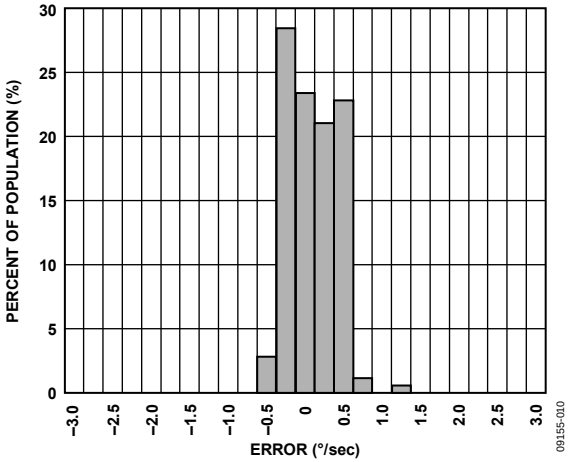


Figure 9. LCC_V Null Drift over Temperature

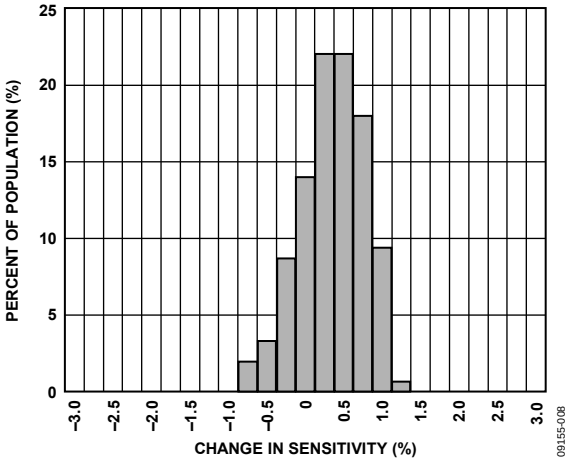


Figure 7. SOIC_CAV Sensitivity Error at 25°C

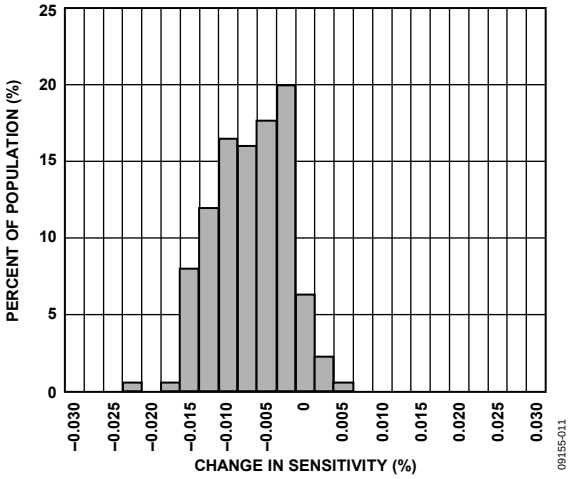


Figure 10. LCC_V Sensitivity Error at 25°C

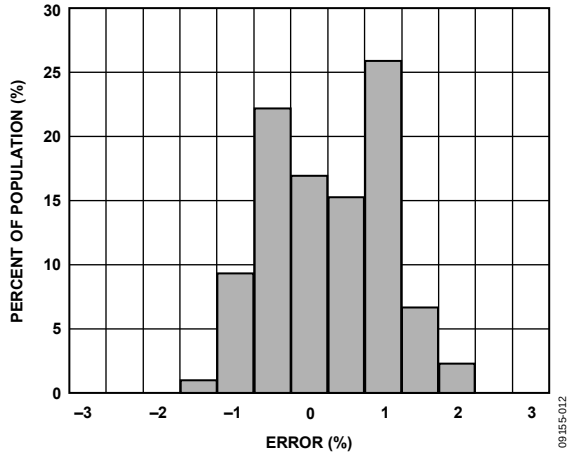


Figure 11. SOIC_CAV Sensitivity Drift over Temperature

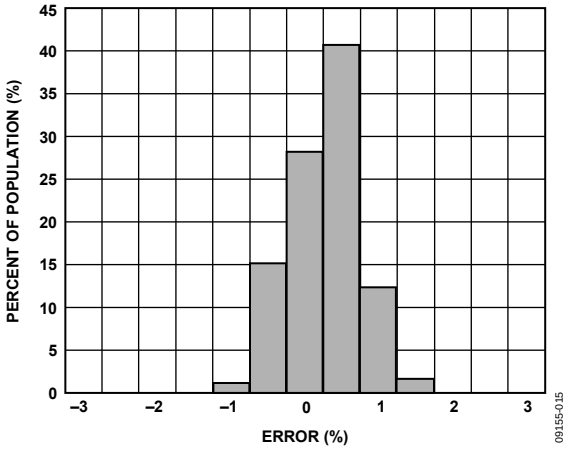


Figure 14. LCC_V Sensitivity Drift over Temperature

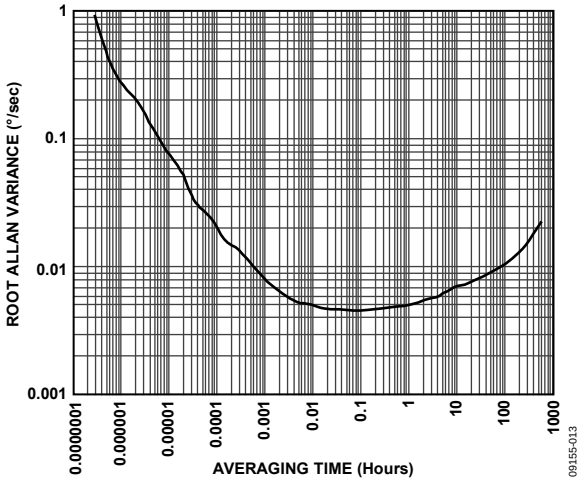


Figure 12. Typical Root Allan Variance at 40°C

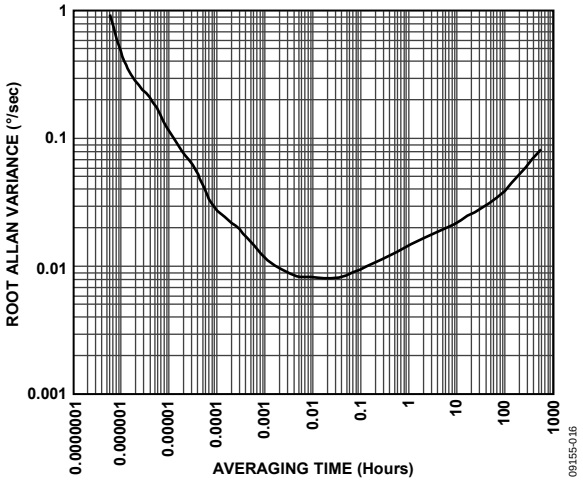


Figure 15. Typical Root Allan Variance at 105°C

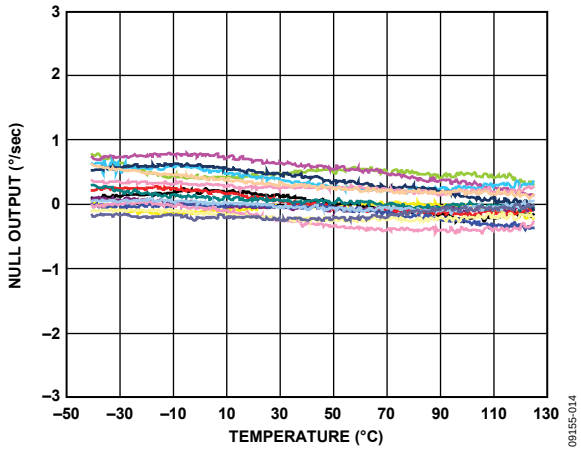


Figure 13. Null Output over Temperature, 16 Devices Soldered on PCB

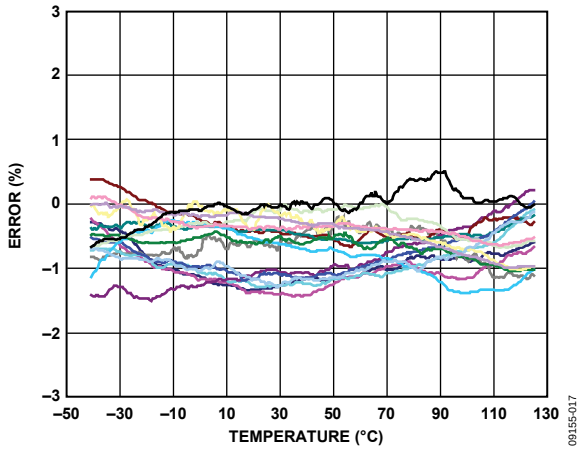


Figure 16. Sensitivity over Temperature, 16 Devices Soldered on PCB

THEORY OF OPERATION

The ADXRS453 operates on the principle of a resonator gyroscope. Figure 17 shows a simplified version of one of four polysilicon sensing structures. Each sensing structure contains a dither frame that is electrostatically driven to resonance. This produces the necessary velocity element to produce a Coriolis force when the device experiences angular rate. In the SOIC_CAV package, the ADXRS453 is designed to sense a z-axis (yaw) angular rate; the LCC_V vertical mount package orients the device such that it can sense pitch or roll angular rate on the same PCB.

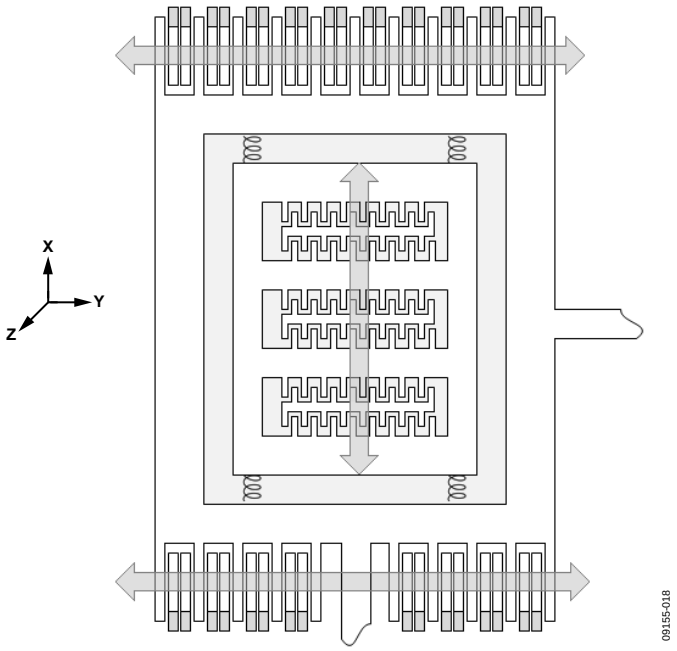


Figure 17. Simplified Gyroscope Sensing Structure

When the sensing structure is exposed to angular rate, the resulting Coriolis force couples into an outer sense frame, which contains movable fingers that are placed between fixed pickoff fingers. This forms a capacitive pickoff structure that senses Coriolis motion. The resulting signal is fed to a series of gain and demodulation stages that produce the electrical rate signal output. The quad sensor design rejects linear and angular acceleration, including external *g*-forces and vibration. This is achieved by mechanically coupling the four sensing structures such that external *g*-forces appear as common-mode signals that can be removed by the fully differential architecture implemented in the ADXRS453.

The resonator requires 22.5 V (typical) for operation. Because only 5 V is typically available in most applications, a switching regulator is included on chip.

CONTINUOUS SELF-TEST

The ADXRS453 gyroscope implements a complete electromechanical self-test. An electrostatic force is applied to the gyroscope frame, resulting in a deflection of the capacitive sense fingers. This deflection is exactly equivalent to deflection that occurs as a result of external rate input. The output from the beam structure is processed by the same signal chain as a true rate output signal, providing complete coverage of both the electrical and mechanical components.

The electromechanical self-test is performed continuously during operation at a rate higher than the output bandwidth of the device. The self-test routine generates equivalent positive and negative rate deflections. This information can then be filtered with no overall effect on the demodulated rate output.

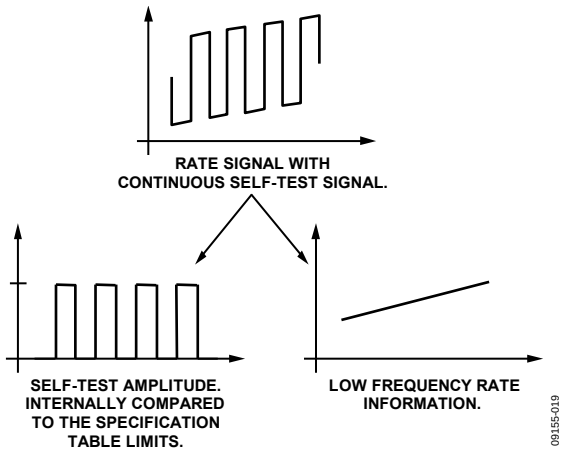


Figure 18. Continuous Self-Test Demodulation

The difference amplitude between the positive and negative self-test deflections is filtered to $f_0/8000$ (~1.95 Hz) and is continuously monitored and compared to hard-coded self-test limits. If the measured amplitude exceeds these limits (listed in Table 1), one of two error conditions is asserted, depending on the magnitude of the self-test error.

- For less severe self-test error magnitudes, the CST bit of the fault register is asserted. However, the status bits (ST[1:0]) in the sensor data response remain set to 01 for valid sensor data.
- For more severe self-test errors, the CST bit of the fault register is asserted and the status bits (ST[1:0]) in the sensor data response are set to 00 for invalid sensor data.

Table 1 lists the thresholds for both of these failure conditions. If desired, the user can access the self-test information by issuing a read command to the self-test memory register (Address 0x04). See the SPI Communication Protocol section for more information about error reporting.

MECHANICAL PERFORMANCE

The ADXRS453 has excellent shock and vibration rejection. Figure 19 shows the output noise response of the ADXRS453 in a vibration free environment. Figure 20 shows the response of the same device to 15 *g* rms random vibration (50 Hz to 5 kHz). As shown in Figure 20, no frequencies are particularly sensitive to vibration. Response to vibration in all axes is similar.

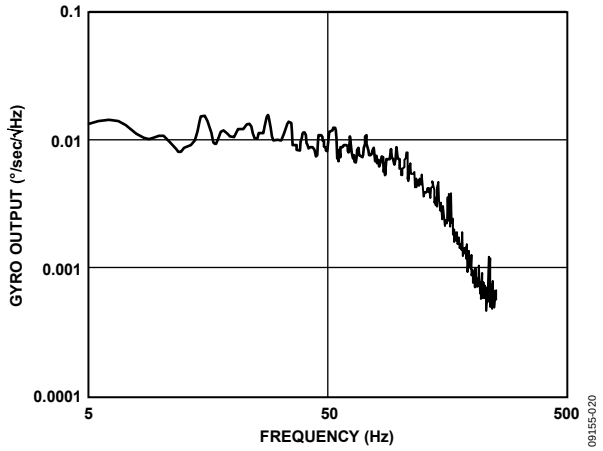


Figure 19. ADXRS453 Output Noise Response with No Vibration Applied

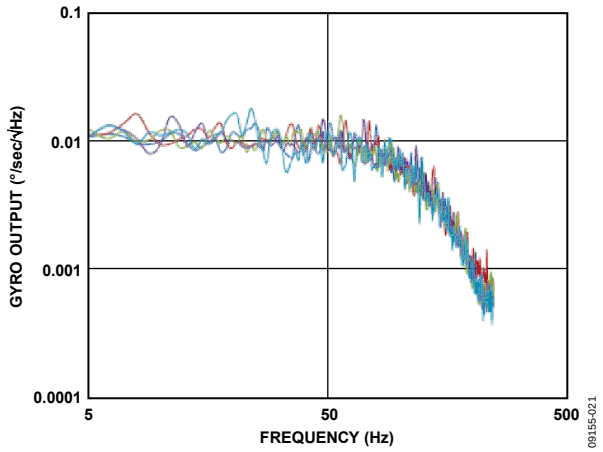


Figure 20. ADXRS453 Output Noise Response with 15 g RMS Random Vibration (50 Hz to 5 kHz) Applied

Shock response is also excellent, as shown in Figure 21 and Figure 22. Figure 21 shows a 99 *g* input stimulus applied to each axis, and Figure 22 shows the typical response to this shock in each axis. Shock response of 0.01°/sec/*g* is apparent.

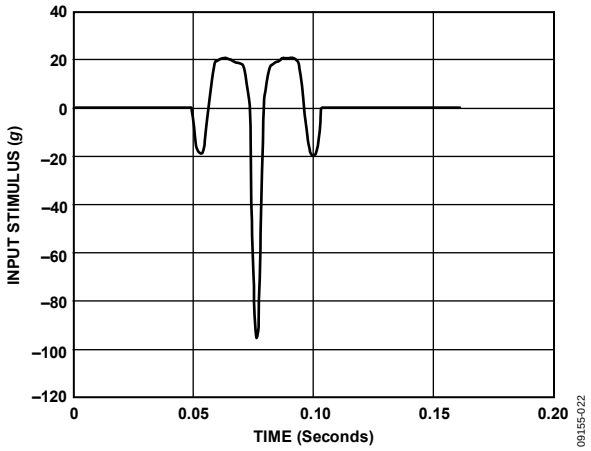


Figure 21. 99 g Shock Input

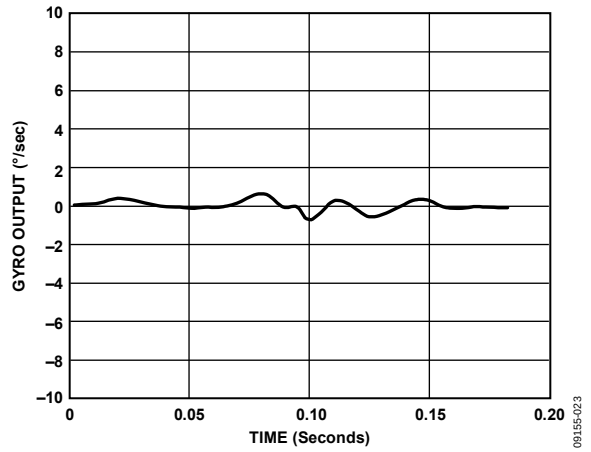


Figure 22. Typical Output Response Due to 99 g Shock (see Figure 21)

NOISE PERFORMANCE

The ADXRS453 noise performance is very consistent from device to device and varies very predictably with temperature. Table 6 contains statistical noise data at three temperature points for a large population of ADXRS453 devices (more than 3000 parts from several manufacturing lots).

Table 6. Statistical Noise Data

	Noise (°/sec/√Hz)	
Temperature	**Mean**	**Standard Deviation**
–40°C	0.0109	0.0012
+25°C	0.0149	0.0015
+105°C	0.0222	0.0019

Noise increases fairly linearly with temperature, as shown in Figure 23.

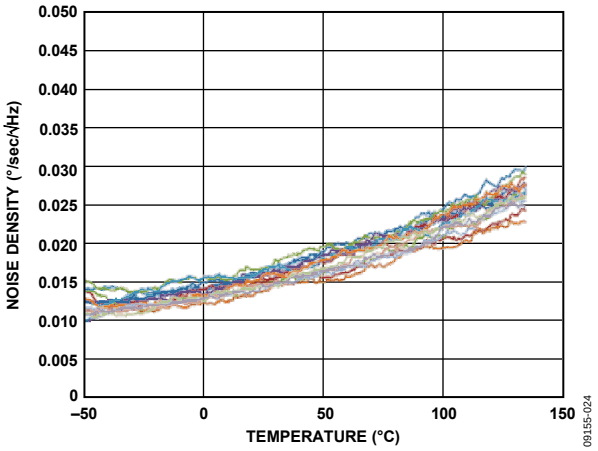


Figure 23. Noise Density vs. Temperature, 16 Devices

APPLICATIONS INFORMATION

CALIBRATED PERFORMANCE

The ADXRS453 gyroscope uses internal EEPROM memory to store its temperature calibration information. The calibration information is encoded into the device during factory test. The calibration data is used to perform offset, gain, and self-test corrections over temperature. By storing this information internally, the ADXRS453 eliminates the need for the customer to perform system level temperature calibration.

MECHANICAL CONSIDERATIONS FOR MOUNTING

Mount the ADXRS453 in a location close to a hard mounting point of the PCB. Mounting the ADXRS453 at an unsupported PCB location (that is, at the end of a lever or in the middle of a trampoline, as shown in Figure 24) can result in apparent measurement errors because the gyroscope is subject to the resonant vibration of the PCB. Locating the gyroscope near a hard mounting point helps to ensure that any PCB resonances at the gyroscope are above the frequency at which harmful aliasing with the internal electronics can occur. To ensure that aliased signals do not couple into the baseband measurement range, design the module so that the first system level resonance occurs at a frequency higher than 800 Hz.

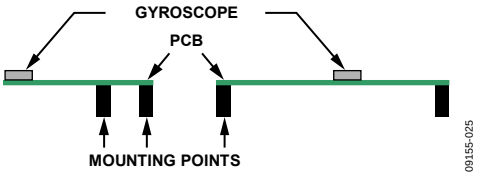


Figure 24. Incorrectly Placed Gyroscope

APPLICATION CIRCUITS

Figure 25 and Figure 26 show the recommended application circuits for the ADXRS453 gyroscope. These application circuits provide a connection reference for the available package types. Note that DV_{DD}, AV_{DD}, and P_{DD} are all individually connected to ground through 1 µF capacitors; do not connect these supplies together. In addition, an external diode and inductor must be connected for proper operation of the internal shunt regulator (see Table 7). These components allow the internal resonator drive voltage to reach its required level.

Table 7. Components for ADXRS453 Application Circuits

Component	Qty	Description
Inductor	1	470 µH
Diode	1	>24 V breakdown voltage
Capacitor	3	1 µF
Capacitor	1	100 nF

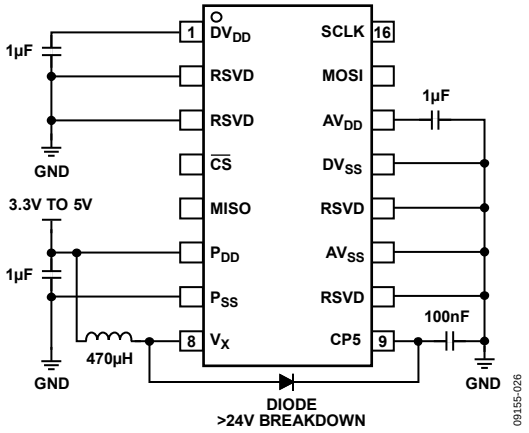


Figure 25. Recommended Application Circuit, SOIC_CAV Package

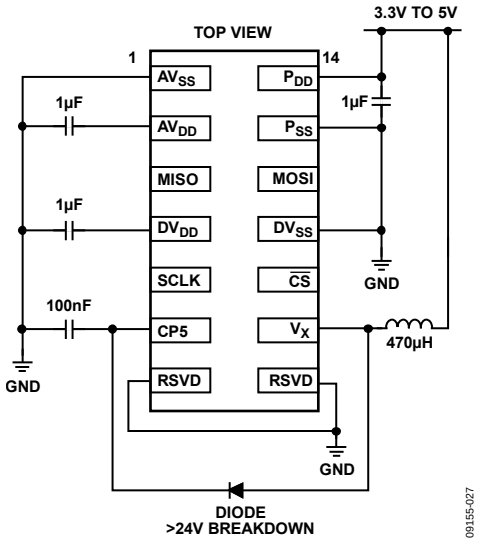


Figure 26. Recommended Application Circuit, LCC_V Package

ADXRS453 SIGNAL CHAIN TIMING

The ADXRS453 primary signal chain is shown in Figure 27. The signal chain is the series of necessary functional circuit blocks through which the rate data is generated and processed. This sequence of electromechanical elements determines how quickly the device can translate an external rate input stimulus to an SPI word that is sent to the master device.

The group delay, which is a function of the filter characteristic, is the time required for the output of the low-pass filter to be within 10% of the external rate input. In Figure 27, the group delay is shown to be ~4 ms. Additional delay can be observed due to the timing of SPI transactions and the population of the rate data into the internal device registers. Figure 27 illustrates this delay through each element of the signal chain.

The transfer function for the rate data LPF is given as

$$\left[\frac{1-Z^{-64}}{1-Z^{-1}}\right]^2$$

where:

$$T = \frac{1}{f_0} = \frac{1}{16\text{ kHz (typ)}}$$

(f_0 is the resonant frequency of the ADXRS453.)

The transfer function for the continuous self-test LPF is given as

$$\frac{1}{64-\left(63 \times Z^{-1}\right)}$$

where:

$$T = \frac{16}{f_0} = 1\text{ ms (typ)}$$

(f_0 is the resonant frequency of the ADXRS453.)

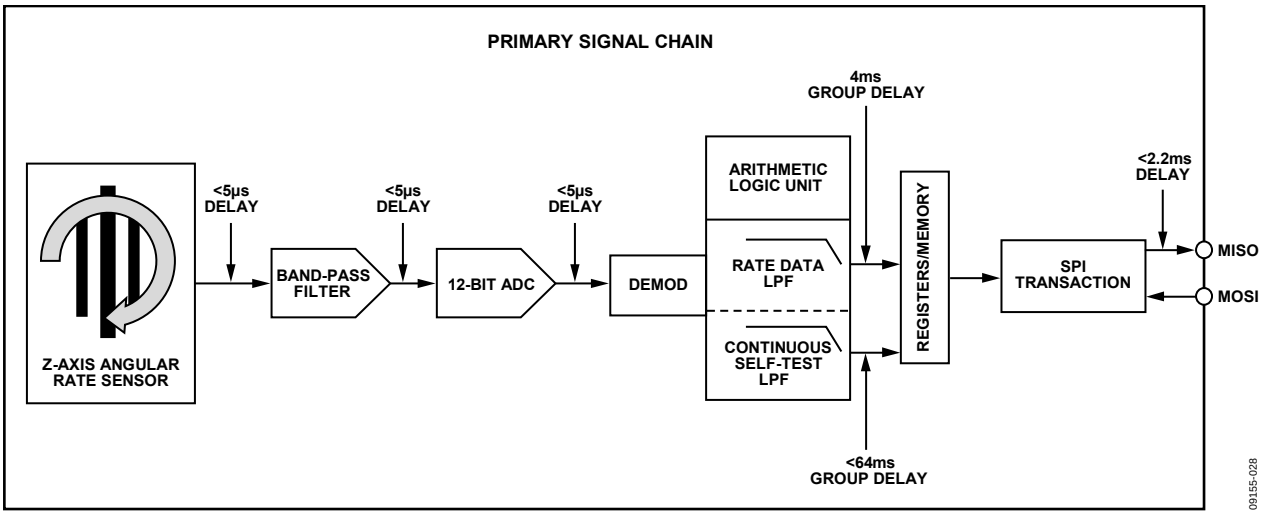


Figure 27. Primary Signal Chain and Associated Delays

SPI COMMUNICATION PROTOCOL

COMMAND/RESPONSE

Input/output is handled through a 32-bit command/response SPI interface. With the command/response SPI interface, the response to a command is issued during the next sequential SPI exchange (see Figure 28).

The format for the interface is defined as follows:

Clock Phase = *Clock Polarity* = 0

Table 9 shows the commands that can be sent from the master device to the gyroscope. Table 10 shows the responses to these commands from the gyroscope. For descriptions of the bits in the commands and responses, see the Command/Response Bit Definitions section and the Fault Register Bit Definitions section.

The device response to the initial command is 0x00000001. This response prevents the transmission of random data to the master device upon the initial command/response exchange.

The SPI interface uses the ADXRS453 pins described in Table 8.

Table 8. SPI Signals

Signal	Pin	Description
Serial Clock	SCLK	Exactly 32 clock cycles during $\overline{CS}$ active
Chip Select	$\overline{CS}$	Active low chip select pin
Master Out/ Slave In	MOSI	Input for data sent to the gyroscope (slave) from the main controller (master)
Master In/ Slave Out	MISO	Output for data sent to the main controller (master) from the gyroscope (slave)

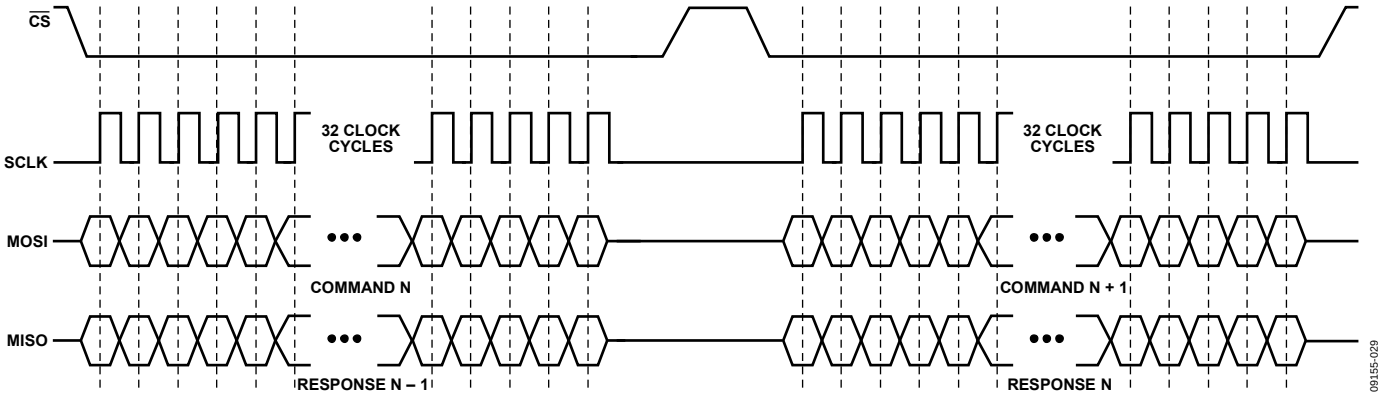


Figure 28. SPI Protocol

Table 9. SPI Commands

	Bit																														
Command	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Sensor Data	SQ1	SQ0	1	SQ2																											CHK	P
Read	1	0	0	SM2	SM1	SM0	A8	A7	A6	A5	A4	A3	A2	A1	A0																	P
Write	0	1	0	SM2	SM1	SM0	A8	A7	A6	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

Table 10. SPI Responses

	Bit																														
Command	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Sensor Data	SQ2	SQ1	SQ0	P0	ST1	ST0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0			PLL	Q	NVM	POR	PWR	CST	CHK	P1
Read	0	1	0	P0	1	1	1	0	SM2	SM1	SM0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0					P1
Write	0	0	1	P0	1	1	1	0	SM2	SM1	SM0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0					P1
R/W Error	0	0	0	P0	1	1	1	0	SM2	SM1	SM0	0	0	SPI	RE	DU									PLL	Q	NVM	POR	PWR	CST	CHK	P1

DEVICE DATA LATCHING

To allow for rapid acquisition of data from the ADXRS453, device data latching is implemented, as shown in Figure 29. When the chip select pin is asserted ($\overline{CS}$ goes low), the data in the device is latched into memory. When the full MOSI command is received and the chip select pin is deasserted ($\overline{CS}$ goes high), the data is shifted into the SPI port registers in preparation for the next sequential command/response exchange. Device data latching allows for an extremely fast sequential transfer delay of 0.1 µs (see Table 11).

Note that the transmitted data is only as recent as the sequential transmission delay implemented by the system. Conditions that result in a sequential transfer delay of several seconds cause the next sequential device response to contain data that is several seconds old.

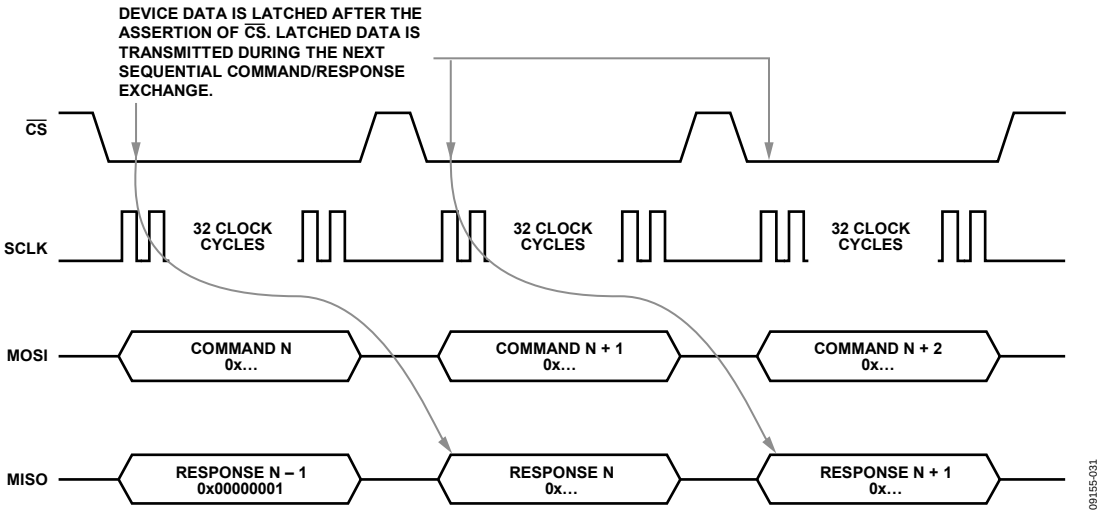


Figure 29. Device Data Latching

SPI TIMING CHARACTERISTICS

The following conditions apply to the SPI command/response timing characteristics in Table 11:

- All timing parameter are guaranteed through characterization.
- All timing is shown with respect to 10% DV_{DD} and 90% of the actual delivered voltage waveform.
- Parameters are valid for 3.0 V ≤ DV_{DD} ≤ 5.5 V.
- Capacitive load for all signals is assumed to be ≤80 pF.
- Ambient temperature is −40°C ≤ T_A ≤ +105°C.
- The MISO pull-up is 47 kΩ or 110 µA.

Table 11. SPI Command/Response Timing Characteristics

Symbol	Min	Max	Unit	Description
f_{OP}		8.08	MHz	SPI operating frequency
t_{SCLKH}	1/2 × t_{SCLK} − 13		ns	SCLK high time
t_{SCLKL}	1/2 × t_{SCLK} − 13		ns	SCLK low time
t_{SCLK}	123.7		ns	SCLK period
t_F	5.5	13	ns	SCLK fall time
t_R	5.5	13	ns	SCLK rise time
t_{SU}	37		ns	Data input (MOSI) setup time
t_{HIGH}	49		ns	Data input (MOSI) hold time
t_A		20	ns	Data output (MISO) access time
t_V		40	ns	Data output (MISO) valid after SCLK
t_{LAG_MISO}	0		ns	Data output (MISO) lag time
t_{DIS}		40	ns	Data output (MISO) disable time
t_{LEAD}	1/2 × t_{SCLK}		ns	Enable ($\overline{CS}$) lead time
$t_{LAG\_\overline{CS}}$	1/2 × t_{SCLK}		ns	Enable ($\overline{CS}$) lag time
t_{TD}	0.1		µs	Sequential transfer delay

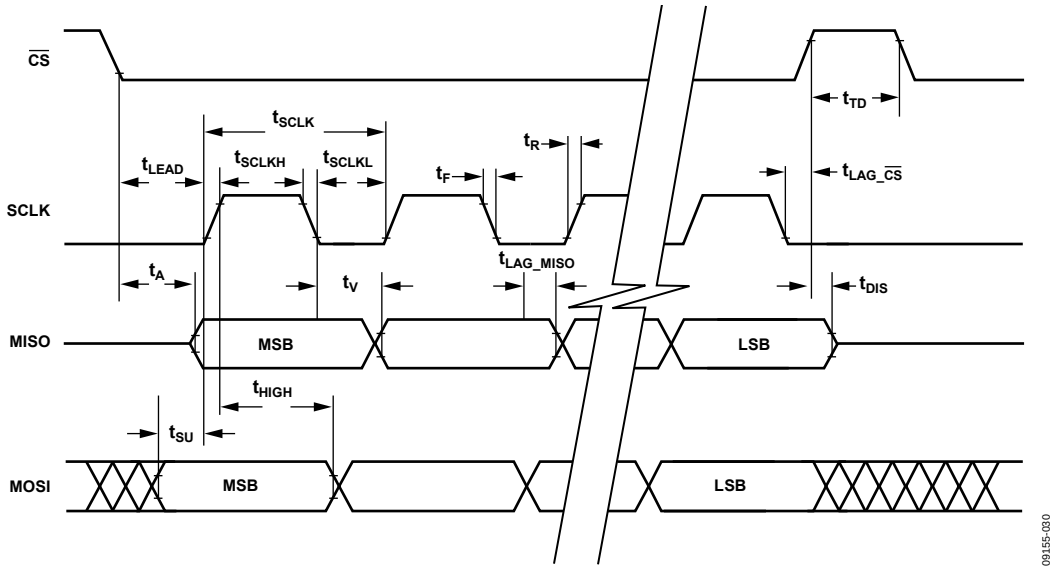


Figure 30. SPI Timings

COMMAND/RESPONSE BIT DEFINITIONS

Table 12. SPI Interface Bit Definitions

Bits	Description
SQ2 to SQ0	Sequence bits (from master)
SM2 to SM0	Sensor module bits (from master)
A8 to A0	Register address
D15 to D0	Data
P	Command odd parity
SPI	SPI command/response
RE	Request error
DU	Data unavailable
ST1, ST0	Status bits
P0	Response, odd parity, Bits[31:16]
P1	Response, odd parity, Bits[31:0]

SQ2 to SQ0 Bits

The SQ2 to SQ0 bits provide the system with a means of synchronizing the data samples that are received from multiple sensors. To facilitate correct synchronization, the ADXRS453 gyroscope includes the SQ[2:0] bits in the response sequence as they were received in the request.

SM2 to SM0 Bits

The SM2 to SM0 bits are the sensor module bits from the master device. These bits are not implemented in the ADXRS453 and are hard-coded to 000 for all occurrences.

A8 to A0 Bits

The A8 to A0 bits represent the memory address for data read or data write. These bits should be supplied by the master when the memory registers are being accessed; these bits are ignored for all sensor data requests. For a complete description of the available memory registers, see the Memory Register Definitions section.

D15 to D0 Bits

The D15 to D0 bits are the 16-bit device data, which can contain any of the following:

- Data from the master to be written to a memory register, as specified by the A8 to A0 bits.
- Sensor rate output data from the slave.
- Device data from the slave read from the memory register specified by the A8 to A0 bits, as well as the data from the next sequential register.
- Following a write command, the 16-bit data that is written to the specified memory register in the ADXRS453 and is reflected back to the master device for correlation.

P Bit

A parity bit (P) is required for all master-to-slave data transmissions. The communication protocol requires one parity bit to achieve odd parity for the entire 32-bit command. "Don't care" bits are also factored into the parity calculation.

SPI Bit

The SPI bit is set when either of the following occurs:

- Too many or not enough bits were transmitted.
- A message from the control module contains a parity error.

A SPI error causes the device to issue a R/W error response regardless of the SPI command type issued by the master device (see Table 10). In addition, any error during a sensor data request results in the device issuing a read/write error.

RE Bit

The request error (RE) bit is the communication error bit transmitted from the ADXRS453 device to the control module. Request errors can occur when

- An invalid command is sent from the control module.
- A read/write command specifies an invalid memory register.
- A write command attempted to write to a nonwritable memory register.

DU Bit

After the chip select pin is deasserted ($\overline{CS}$ goes high), the user must wait 0.1 µs before reasserting the $\overline{CS}$ pin to initiate another command/response frame with the device. Failure to adhere to this timing specification may result in a data unavailable (DU) error.

ST1 and ST0 Bits

The status bits (ST1 and ST0) are used to signal to the master device the type of data contained in the response message (see Table 13).

Table 13. Status Bit Code Definitions

ST[1:0]	Contents of Bits[D15:D0]
00	Invalid data for sensor data response
01	Valid sensor data
10	Sensor self-test data
11	Read/write response

Either of the following conditions can result in the ST[1:0] bits being set to 00 during a sensor data response:

- The self-test response is sufficiently different from its nominal value (see the Specifications section for the appropriate limits).
- The PLL fault bit is active (see the PLL Bit section).

P0 Bit

P0 is the parity bit that establishes odd parity for Bits[31:16] of the device response.

P1 Bit

P1 is the parity bit that establishes odd parity for the entire 32-bit device response.

FAULT REGISTER BIT DEFINITIONS

Table 14 describes the bits available for signaling faults to the user. The individual bits of the fault registers are updated asynchronously, depending on their respective detection criteria; however, it is recommended that the fault registers be read at a rate of at least 250 Hz. When asserted, an individual status bit is not deasserted until it is read by the master device. If the error persists after a fault register read, the status bit is immediately reasserted and remains asserted until the next sequential command/response exchange. The bits in the FAULT0 register are appended to every sensor data response (see Table 10). Both fault registers can be accessed by issuing a read command to Address 0x0A.

Table 14. Fault Register Bit Definitions

Register	Bit Name	Description
FAULT1	Fail	Failure that sets the ST[1:0] bits to 00
	AMP	Amplitude detection failure
	OV	Regulator overvoltage
	UV	Regulator undervoltage
FAULT0	PLL	Phase-locked loop failure
	Q	Quadrature error
	NVM	Nonvolatile memory fault
	POR	Power-on or reset failed to initialize
	PWR	Power regulation failed due to overvoltage or undervoltage condition
	CST	Continuous self-test failure or amplitude detection failed
	CHK	Check: generate faults

Fail Bit

The fail flag is asserted when the ST[1:0] bits are set to 00 (see the ST1 and ST0 Bits section). Assertion of the fail bit indicates that the device has experienced a gross failure and that the sensor data could be invalid.

AMP Bit

The AMP fault bit is asserted when the measured amplitude of the silicon resonator has been significantly reduced. This condition can occur if the voltage supplied to CP5 falls below the requirements of the internal voltage regulator. This fault bit is OR'ed with the CST fault bit; therefore, during a sensor data request, the CST bit position represents either an AMP failure or a CST failure. The full fault register can be read from memory to determine the specific failure.

OV Bit

The OV fault bit is asserted if the internally regulated voltage (nominally 3 V) is observed to exceed 3.3 V. This measurement is low-pass filtered to prevent artifacts such as noise spikes from asserting a fault condition. When an OV fault occurs, the PWR fault bit is asserted simultaneously. Because the OV fault bit is not transmitted as part of a sensor data response, it is recommended that the user read back the FAULT1 and FAULT0 memory registers upon the assertion of a PWR error to determine the specific error condition.

UV Bit

The UV fault bit is asserted if the internally regulated voltage (nominally 3 V) is observed to be less than 2.77 V. This measurement is low-pass filtered to prevent artifacts such as noise spikes from asserting a fault condition. When a UV fault occurs, the PWR fault bit is asserted simultaneously. Because the UV fault bit is not transmitted as part of a sensor data response, it is recommended that the user read back the FAULT1 and FAULT0 memory registers upon the assertion of a PWR error to determine the specific error condition.

PLL Bit

The PLL bit indicates that the device has experienced a failure in the phase-locked loop functional circuit block. This occurs when the PLL fails to achieve synchronization with the resonator structure. If the PLL status flag is active, the ST[1:0] bits of the sensor data response are set to 00, indicating that the response contains potentially invalid rate data.

Q Bit

A Q fault is asserted based on two independent quadrature calculations.

- The quad memory register (Address 0x08) contains a value corresponding to the total instantaneous quadrature present in the device. If this value exceeds 4096 LSB, a Q fault is issued.
- An internal quadrature accumulator records the amount of quadrature correction performed by the ADXRS453. A Q fault is issued when the quadrature error present in the device has contributed to an equivalent of 4°/sec (typical) of rate offset.

NVM Bit

An NVM error is transmitted to the control module when the internal nonvolatile memory data fails a checksum calculation. This check is performed once every 50 µs and does not include the PIDx memory registers.

POR Bit

An internal check is performed on device startup to ensure that the volatile memory of the device is functional. This is accomplished by programming a known value from the device ROM into a volatile memory register. This value is then continuously compared to the known value in ROM every 1 µs for the duration of the device operation. If the value stored in the volatile memory changes or does not match the value stored in ROM, the POR error flag is asserted. The value stored in ROM is rewritten to the volatile memory upon a device power cycle.

PWR Bit

The device performs a continuous check of the internal 3 V regulated voltage level. If either an overvoltage (OV) or undervoltage (UV) fault is asserted, the PWR bit is also asserted. This condition occurs if the regulated voltage is observed to be either above 3.3 V or below 2.77 V. An internal low-pass filter removes high frequency glitching effects to prevent the PWR bit from being asserted unnecessarily. To determine whether the fault is a result of an overvoltage or undervoltage condition, the OV and UV fault bits must be read.

CST Bit

The ADXRS453 is designed with continuous self-test functionality. The measured self-test amplitudes are compared to the limits presented in Table 1. Deviations from these values result in reported self-test errors. The two thresholds for a self-test failure are as follows:

- Self-test value > ±512 LSB from nominal results in the assertion of the self-test flag in the fault register.
- Self-test value > ±1856 LSB from nominal results in the assertion of the self-test flag in the fault register and the setting of the ST[1:0] bits to 00, indicating that the rate data contained in the sensor data response is potentially invalid.

CHK Bit

The CHK bit is transmitted by the control module to the ADXRS453 as a method of generating faults. By asserting the CHK bit, the device creates conditions that result in the generation of all faults represented in the fault registers. For example, the self-test amplitude is deliberately altered to exceed the fault detection threshold, resulting in a self-test error. In this way, the device is capable of checking both its ability to detect a fault condition and its ability to report that fault condition to the control module.

The fault conditions are initiated nearly simultaneously; however, the timing for receiving fault codes when the CHK bit is asserted depends on the time required to generate each unique fault. It takes no more than 50 ms for all internal faults to be generated and the fault register to be updated to reflect the condition of the device. Until the CHK bit is cleared, the status bits (ST[1:0]) are set to 10, indicating that the data should be interpreted by the control module as self-test data. After the CHK bit is deasserted, an additional 50 ms are required for the fault conditions to decay and for the device to return to normal operation. See the Recommended Start-Up Sequence with CHK Bit Assertion section for the proper methodology for asserting the CHK bit.

RECOMMENDED START-UP SEQUENCE WITH CHK BIT ASSERTION

Figure 31 illustrates a recommended start-up sequence that can be implemented by the user. Alternate start-up sequences can be used, but the response from the ADXRS453 must be handled correctly. If the start-up sequence is implemented immediately after power is applied to the device, the total time to implement the following fault detection routine is approximately 200 ms.

As described in the Device Data Latching section, the data present in the device upon the assertion of the $\overline{CS}$ signal is used in the next sequential command/response exchange. This results in an apparent one-transaction delay before the data resulting from the assertion of the CHK bit is reported by the device. For all other read/write interactions with the device, no such delay exists, and the MOSI command is serviced during the next sequential command/response exchange.

Note that if the CHK bit is deasserted and the user tries to obtain data from the device before the CST fault flag clears, the device reports the data as error data.

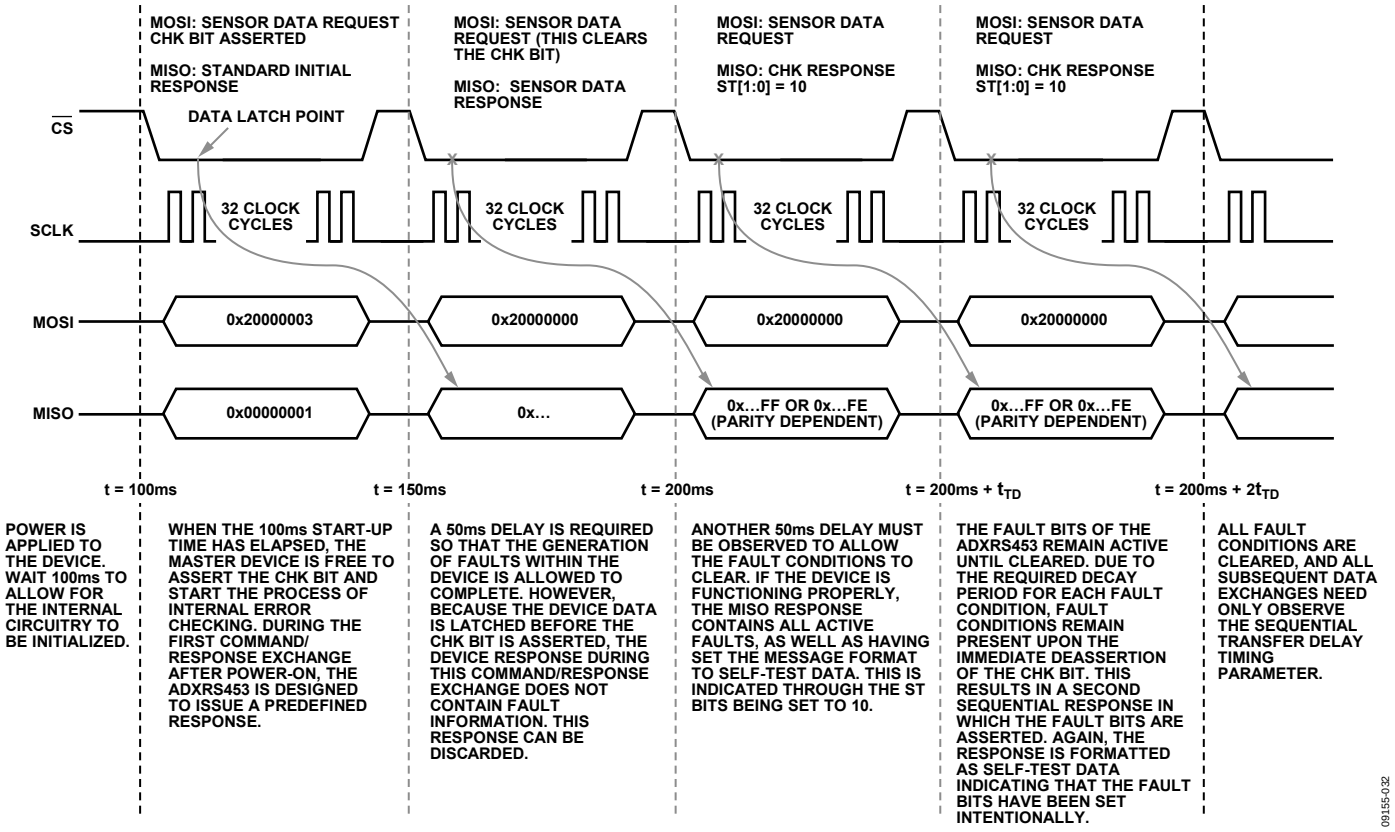


Figure 31. Recommended Start-Up Sequence

RATE DATA FORMAT

The ADXRS453 gyroscope transmits rate data in a 16-bit format as part of a 32-bit SPI data frame. See Table 10 for the full 32-bit format of the sensor data response. The rate data is transmitted MSB first, from D15 to D0.

The data is formatted as a twos complement number with a scale factor of 80 LSB/°/sec. Therefore, the highest obtainable value for positive (clockwise) rotation is 0x7FFF (decimal +32,767), and the highest obtainable value for negative (counterclockwise) rotation is 0x8000 (decimal −32,768). Performance of the device is not guaranteed above ±24,000 LSB (±300°/sec).

Table 15. Rate Data

16-Bit Rate Data		
Decimal (LSBs)	**Hex (D15:D0)**	**Description**
+32,767	0x7FFF	Maximum possible positive data value (not guaranteed)
…	…	…
+24,000	0x5DC0	+300°/sec rotation (positive FSR)
…	…	…
+160	0x00A0	+2°/sec rotation
…	…	…
+80	0x0050	+1°/sec rotation
…	…	…
+40	0x0028	+0.5°/sec rotation
…	…	…
+20	0x0014	+0.025°/sec rotation
…	…	…
0	0x0000	Zero rotation value
…	…	…
−20	0xFFEC	−0.025°/sec rotation
…	…	…
−40	0xFFD8	−0.5°/sec rotation
…	…	…
−80	0xFFB0	−1°/sec rotation
…	…	…
−160	0xFF60	−2°/sec rotation
…	…	…
−24,000	0xA240	−300°/sec rotation (negative FSR)
…	…	…
−32,768	0x8000	Maximum possible negative data value (not guaranteed)

MEMORY MAP AND REGISTERS

MEMORY MAP

Table 16 provides a list of the memory registers that can be read from or written to by the user. See the SPI Communication Protocol section for the proper input sequence to read from or write to a specific memory register. Each memory register has eight bits of data; however, when a read request is performed, the data always returns as a 16-bit message. This is accomplished by appending the data from the next sequential register to the memory address that was specified.

Data is transmitted MSB first. For proper acquisition of data from the memory register, make the read request to the even-numbered register address only; for example, to read the LOCSTx registers, Address Register 0x04, but not Register 0x05. For a description of each memory register listed in Table 16, see the Memory Register Definitions section.

Table 16. Memory Register Map

Address	Register Name	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
0x00	RATE1	RTE15	RTE14	RTE13	RTE12	RTE11	RTE10	RTE9	RTE8
0x01	RATE0	RTE7	RTE6	RTE5	RTE4	RTE3	RTE2	RTE1	RTE0
0x02	TEM1	TEM9	TEM8	TEM7	TEM6	TEM5	TEM4	TEM3	TEM2
0x03	TEM0	TEM1	TEM0	Unused	Unused	Unused	Unused	Unused	Unused
0x04	LOCST1	LCST15	LCST14	LCST13	LCST12	LCST11	LCST10	LCST9	LCST8
0x05	LOCST0	LCST7	LCST6	LCST5	LCST4	LCST3	LCST2	LCST1	LCST0
0x06	HICST1	HCST15	HCST14	HCST13	HCST12	HCST11	HCST10	HCST9	HCST8
0x07	HICST0	HCST7	HCST6	HCST5	HCST4	HCST3	HCST2	HCST1	HCST0
0x08	QUAD1	QAD15	QAD14	QAD13	QAD12	QAD11	QAD10	QAD9	QAD8
0x09	QUAD0	QAD7	QAD6	QAD5	QAD4	QAD3	QAD2	QAD1	QAD0
0x0A	FAULT1	Unused	Unused	Unused	Unused	Fail	AMP	OV	UV
0x0B	FAULT0	PLL	Q	NVM	POR	PWR	CST	CHK	0
0x0C	PID1	PIDB15	PIDB14	PIDB13	PIDB12	PIDB11	PIDB10	PIDB9	PIDB8
0x0D	PID0	PIDB7	PIDB6	PIDB5	PIDB4	PIDB3	PIDB2	PIDB1	PIDB0
0x0E	SN3	SNB31	SNB30	SNB29	SNB28	SNB27	SNB26	SNB25	SNB24
0x0F	SN2	SNB23	SNB22	SNB21	SNB20	SNB19	SNB18	SNB17	SNB16
0x10	SN1	SNB15	SNB14	SNB13	SNB12	SNB11	SNB10	SNB9	SNB8
0x11	SN0	SNB7	SNB6	SNB5	SNB4	SNB3	SNB2	SNB1	SNB0

MEMORY REGISTER DEFINITIONS

The SPI-accessible memory registers are described in this section. As noted in the Memory Map section, when requesting data from a memory register, only the first sequential memory address should be addressed. The data returned by the device contains 16 bits of memory register information. Bits[15:8] contain the MSB of the requested information, and Bits[7:0] contain the LSB.

Rate (RATEx) Registers

Addresses: 0x00 (RATE1)
0x01 (RATE0)

Register update rate: $f_0/32$ (~485 Hz)

Scale factor: 80 LSB/°/sec

The RATEx registers contain the temperature compensated rate output of the device, filtered to $f_0/200$ (~77.5 Hz). This data can also be accessed by issuing a sensor data read request to the device. The data is presented as a 16-bit, twos complement number.

MSB **LSB**

D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
RTE15	RTE14	RTE13	RTE12	RTE11	RTE10	RTE9	RTE8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RTE7	RTE6	RTE5	RTE4	RTE3	RTE2	RTE1	RTE0

Temperature (TEMx) Registers

Addresses: 0x02 (TEM1)
0x03 (TEM0)

Register update rate: $f_0/32$ (~485 Hz)

Scale factor: 5 LSB/°C

The TEMx registers contain a value corresponding to the temperature of the device. The data is presented as a 10-bit, twos complement number. 0 LSB corresponds to a temperature of approximately 45°C (see Table 17).

MSB **LSB**

D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
TEM9	TEM8	TEM7	TEM6	TEM5	TEM4	TEM3	TEM2
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
TEM1	TEM0	Unused					

Table 17. Sample Temperatures and TEMx Register Contents

Temperature	Value of TEM1 and TEM0 Registers[1]
45°C	0000 0000 00XX XXXX
85°C	0011 0010 00XX XXXX
0°C	1100 0111 11XX XXXX

[1] X = don't care.

Low CST (LOCSTx) Registers

Addresses: 0x04 (LOCST1)
0x05 (LOCST0)

Register update rate: $f_0/16$ (~970 Hz)

Scale factor: 80 LSB/°/sec

The LOCSTx registers contain the value of the temperature compensated and low-pass filtered continuous self-test delta. This value is a measure of the difference between the positive and negative self-test deflections and corresponds to the values presented in Table 1. The device issues a CST error if the value of the self-test exceeds the established self-test limits. The self-test data is filtered to $f_0/8000$ (~1.95 Hz) to prevent false triggering of the CST fault bit. The data is presented as a 16-bit, twos complement number, with a scale factor of 80 LSB/°/sec.

MSB **LSB**

D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
LCST15	LCST14	LCST13	LCST12	LCST11	LCST10	LCST9	LCST8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
LCST7	LCST6	LCST5	LCST4	LCST3	LCST2	LCST1	LCST0

High CST (HICSTx) Registers

Addresses: 0x06 (HICST1)
0x07 (HICST0)

Register update rate: $f_0/16$ (~970 Hz)

Scale factor: 80 LSB/°/sec

The HICSTx registers contain the unfiltered self-test information. The HICSTx data can be used to supplement fault diagnosis in safety critical applications because sudden shifts in the self-test response can be detected. However, the CST bit of the fault register is not set when the HICSTx data is observed to exceed the self-test limits. Only the LOCSTx memory registers, which are designed to filter noise and the effects of sudden temporary self-test spiking due to external disturbances, control the assertion of the CST fault bit. The data is presented as a 16-bit, twos complement number.

MSB **LSB**

D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
HCST15	HCST14	HCST13	HCST12	HCST11	HCST10	HCST9	HCST8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
HCST7	HCST6	HCST5	HCST4	HCST3	HCST2	HCST1	HCST0

Quad Memory (QUADx) Registers

Addresses: 0x08 (QUAD1)
0x09 (QUAD0)

Register update rate: $f_0/64$ (~240 Hz)

Scale factor: 80 LSB/°/sec equivalent

The QUADx registers contain a value corresponding to the amount of quadrature error present in the device at a given time. Quadrature can be likened to a measurement of the error of the motion of the resonator structure and can be caused by stresses and aging effects. The quadrature data is filtered to $f_0/200$ (~77.5 Hz) and can be read frequently to detect sudden shifts in the level of quadrature. The data is presented as a 16-bit, twos complement number.

MSB **LSB**

D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
QAD15	QAD14	QAD13	QAD12	QAD11	QAD10	QAD9	QAD8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
QAD7	QAD6	QAD5	QAD4	QAD3	QAD2	QAD1	QAD0

Fault (FAULTx) Registers

Addresses: 0x0A (FAULT1)
0x0B (FAULT0)

Register update rate: Not applicable

Scale factor: Not applicable

The FAULTx registers contain the state of the error flags in the device. The FAULT0 register is appended to the end of every device data transmission (see Table 10); however, this register can also be accessed independently through its memory location. The individual fault bits are updated asynchronously, requiring <5 µs to activate, as soon as the fault condition exists on chip. When toggled, each fault bit remains active until the fault register is read or a sensor data command is received. If the fault is still active after the bit is read, the fault bit is immediately reasserted.

MSB **LSB**

D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Unused				Fail	AMP	OV	UV
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PLL	Q	NVM	POR	PWR	CST	CHK	0

Part ID (PIDx) Registers

Addresses: 0x0C (PID1)
0x0D (PID0)

Register update rate: Not applicable

Scale factor: Not applicable

The (PIDx) registers contain a 16-bit number that identifies the version of the ADXRS453. Combined with the serial number, this information allows for a higher degree of device individualization and tracking. The initial product ID is R01 (0x5201), with subsequent versions of silicon incrementing this value to R02, R03, and so on.

MSB **LSB**

D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
PIDB15	PIDB14	PIDB13	PIDB12	PIDB11	PIDB10	PIDB9	PIDB8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PIDB7	PIDB6	PIDB5	PIDB4	PIDB3	PIDB2	PIDB1	PIDB0

Serial Number (SNx) Registers

Addresses: 0x0E (SN3)
0x0F (SN2)
0x10 (SN1)
0x11 (SN0)

Register update rate: Not applicable

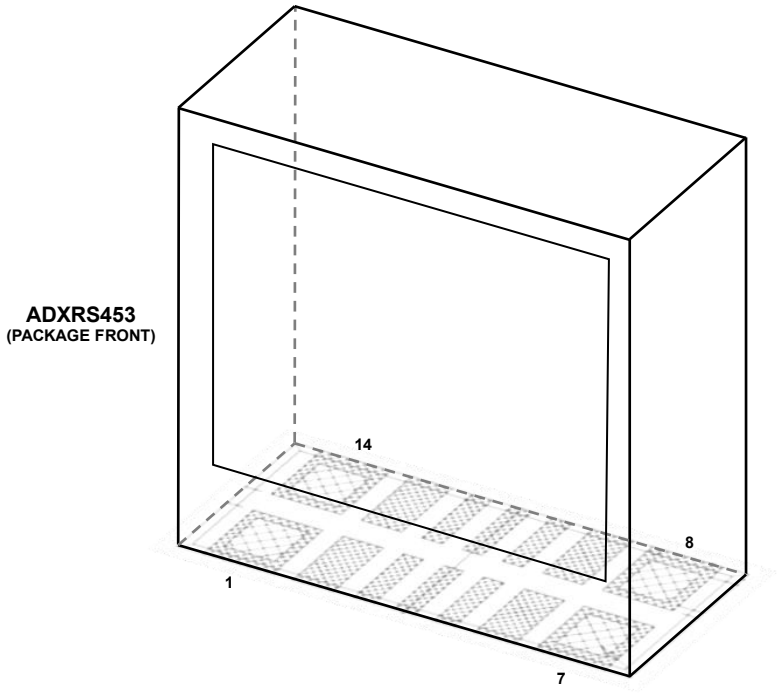
Scale factor: Not applicable

The SNx registers contain a 32-bit identification number that uniquely identifies the device. To read the entire serial number, two memory read requests must be initiated. The first read request to Address 0x0E returns the upper 16 bits of the serial number, and the following read request to Address 0x10 returns the lower 16 bits of the serial number.

MSB **LSB**

D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**
SNB31	SNB30	SNB29	SNB28	SNB27	SNB26	SNB25	SNB24
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
SNB23	SNB22	SNB21	SNB20	SNB19	SNB18	SNB17	SNB16
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
SNB15	SNB14	SNB13	SNB12	SNB11	SNB10	SNB9	SNB8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SNB7	SNB6	SNB5	SNB4	SNB3	SNB2	SNB1	SNB0

PACKAGE ORIENTATION AND LAYOUT INFORMATION



NOTES
1. THE PACKAGE HAS TERMINALS ON TWO FACES. HOWEVER, THE TERMINALS ON THE BACK ARE FOR INTERNAL EVALUATION ONLY AND SHOULD NOT BE USED IN THE END APPLICATION. THE TERMINALS ON THE BOTTOM OF THE PACKAGE INCORPORATE METALLIZATION BUMPS THAT ENSURE A MINIMUM SOLDER THICKNESS FOR IMPROVED SOLDER JOINT RELIABILITY. THESE BUMPS ARE NOT PRESENT ON THE BACK TERMINALS AND, THEREFORE, POOR SOLDER JOINT RELIABILITY CAN BE ENCOUNTERED IF THE BACK TERMINALS ARE USED IN THE END APPLICATION. FOR THE OUTLINE DIMENSIONS OF THIS PACKAGE, SEE FIGURE 38.

Figure 32. 14-Lead Ceramic LCC_V, Vertical Mount

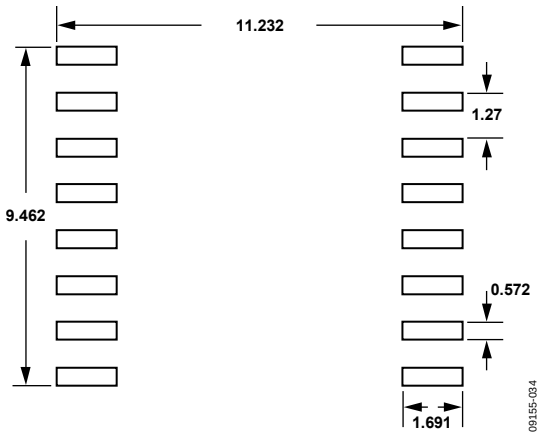


Figure 33. Sample SOIC_CAV Solder Pad Layout (Land Pattern), Dimensions Shown in Millimeters, Not to Scale

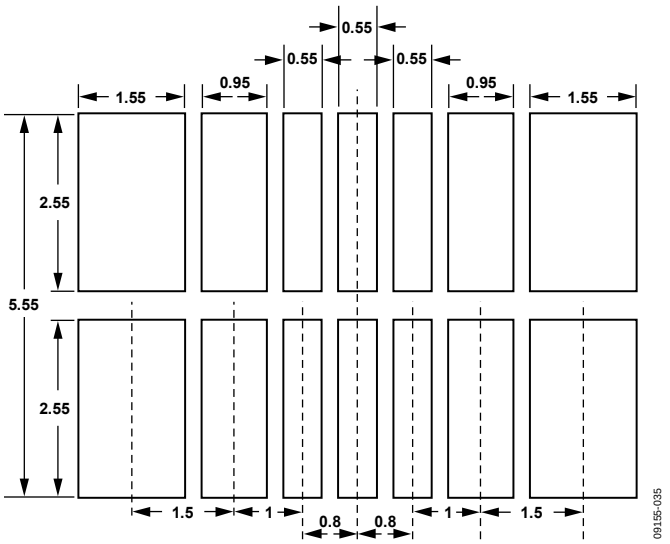


Figure 34. Sample LCC_V Solder Pad Layout (Land Pattern), Dimensions Shown in Millimeters, Not to Scale

SOLDER PROFILE

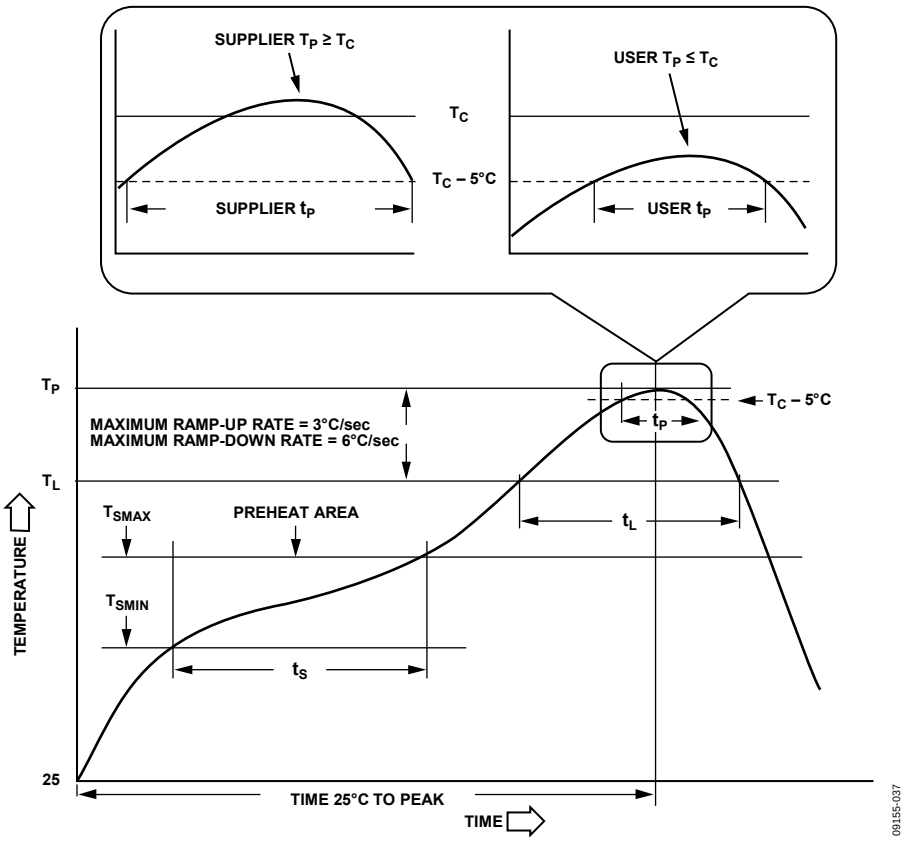


Figure 35. Recommended Soldering Profile

Table 18. Recommended Soldering Profile Limits

Profile Feature	Sn63/Pb37	Pb-Free
Average Ramp Rate (T_L to T_P)	3°C/sec max	3°C/sec max
Preheat		
Minimum Temperature (T_{SMIN})	100°C	150°C
Maximum Temperature (T_{SMAX})	150°C	200°C
Time (T_{SMIN} to T_{SMAX}), t_S	60 sec to 120 sec	60 sec to 120 sec
Ramp-Up Rate (T_{SMAX} to T_L)	3°C/sec max	3°C/sec max
Time Maintained Above Liquidous (t_L)	60 sec to 150 sec	60 sec to 150 sec
Liquidous Temperature (T_L)	183°C	217°C
Classification Temperature (T_C)[1]	220°C	250°C
Peak Temperature (T_P)	T_C + 0°C/−5°C	T_C + 0°C/−5°C
Time Within 5°C of Actual Peak Temperature (t_P)	10 sec to 30 sec	20 sec to 40 sec
Ramp-Down Rate (T_P to T_L)	6°C/sec max	6°C/sec max
Time 25°C to Peak Temperature	6 minutes max	8 minutes max

[1] Based on IPC/JEDEC J-STD-020D.01 for SnPb and Pb-free processes. Package volume < 350 mm^3, package thickness > 2.5 mm.

PACKAGE MARKING CODES

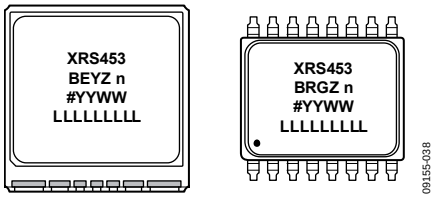


Figure 36. LCC_V and SOIC_CAV Package Marking Codes

Table 19. Package Code Designations

Marking	Meaning
XRS	Angular rate sensor
453	Series number
B	Temperature grade (−40°C to +105°C)
RG	Package designator (SOIC_CAV package)
EY	Package designator (LCC_V package)
Z	RoHS compliant
n	Revision number
#	Pb-free designation
YYWW	Assembly date code
LLLLLLLLL	Assembly lot code (up to nine characters)

OUTLINE DIMENSIONS

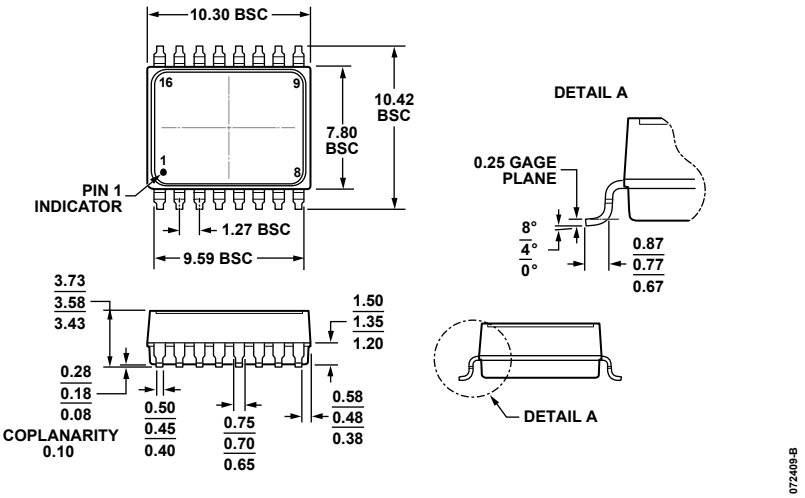


Figure 37. 16-Lead Small Outline, Plastic Cavity Package [SOIC_CAV]
(RG-16-1)
Dimensions shown in millimeters

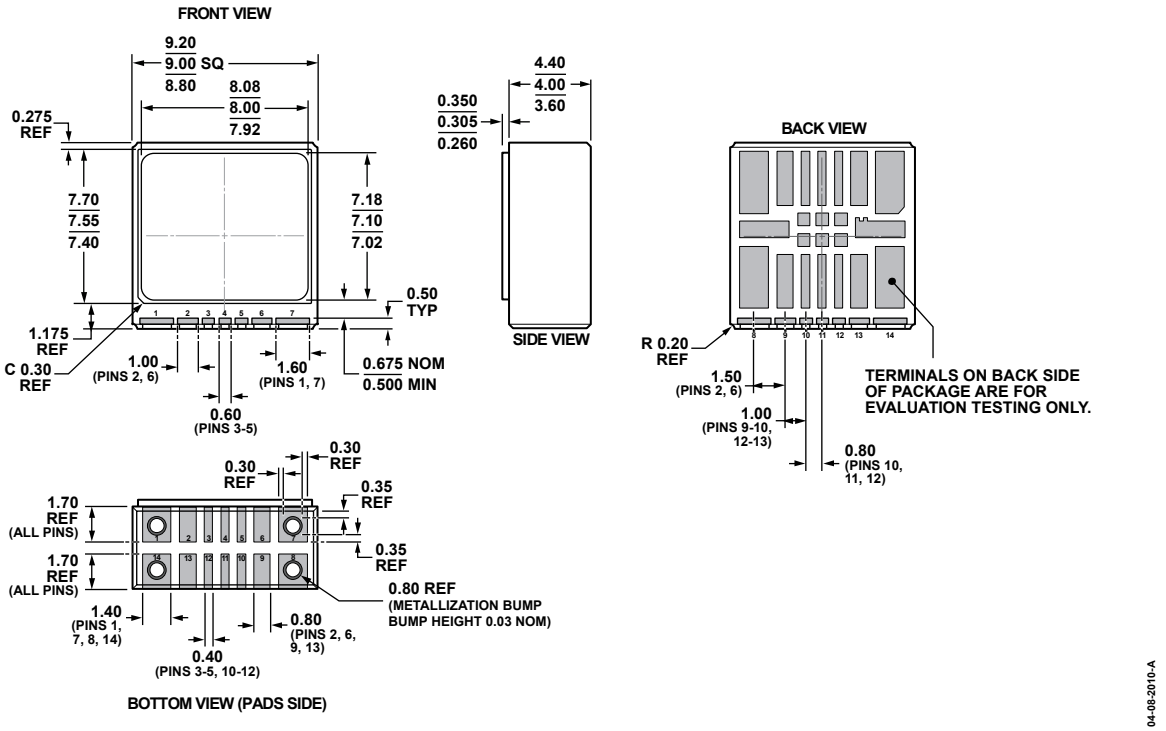


Figure 38. 14-Terminal Ceramic Leadless Chip Carrier, Vertical Form [LCC_V]
(EY-14-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADXRS453BEYZ	−40°C to +105°C	14-Terminal Ceramic Leadless Chip Carrier, Vertical Form [LCC_V]	EY-14-1
ADXRS453BEYZ-RL	−40°C to +105°C	14-Terminal Ceramic Leadless Chip Carrier, Vertical Form [LCC_V]	EY-14-1
ADXRS453BRGZ	−40°C to +105°C	16-Lead Small Outline, Plastic Cavity Package [SOIC_CAV]	RG-16-1
ADXRS453BRGZ-RL	−40°C to +105°C	16-Lead Small Outline, Plastic Cavity Package [SOIC_CAV]	RG-16-1
EVAL-ADXRS453Z		Evaluation Board, SOIC_CAV	
EVAL-ADXRS453Z-V		Evaluation Board, LCC_V	
EVAL-ADXRS453Z-M		Analog Devices Inertial Sensor Evaluation System (Includes ADXRS453 Satellite)	
EVAL-ADXRS453Z-S		ADXRS453 Satellite, Standalone, to be used with Inertial Sensor Evaluation System	

[1] Z = RoHS Compliant Part.

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