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REVISION HISTORY

3/10—Rev. 0 to Rev. A

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SPECIFICATIONS

Table 1.

DIGITAL INPUTS input Voltage, High (Vw) Input Voltage, High (Vw) Input Voltage, High (Vw) Output Voltage Differential Output Short-Circuit Current Transmitter Supply Current Transmitter Supply Voltage Vw Supply Voltag	Parameter	Test Conditions/Comments	Temp	Test Level ¹	Min	Тур	Max	Unit
Input Voltage, Low (Vk) Full Vit Full Vit U U U U U U U V <	DIGITAL INPUTS							
Input Voltage, Low (V4) Full VI Imput Voltage, Low (V4) Imput Voltage, Low (V4) Imput Voltage, Low (V4) VI Imput Voltage, Low (V4) VI VIII VIII VIIII VIIII VIIIII VIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII	Input Voltage, High (V⊮)		Full	VI	1.4		3.5	v
Input Capacitance 25°C V 3 F DIGITAL OUTPUTS Full Full Vul Vul<								v
DIGITAL OUTPUTS Output Voltage, High (Von) Output Voltage, Low (Vo.) Full VI Van_0.1 V THERMAL CHARACTERISTICS Full VI 0.4 V Thermal Resistance v 15.2 "C/W 0.4 Junction to Case V 15.2 "C/W Mabient Temperature Full V 25°C VI -10 +10 µA Input Clamp Voltage -16 mA 25°C V -0.8 V V 0.4 V Differential High Level Output Voltage -16 mA 25°C V -0.8 V V 0 0.4 V V 0.8 V V 0.4 V <						3		рF
Output Voltage, Liny (Von) Full VI Von -0.1 V Von -0.1 V Output Voltage, Low (Von) - Full VI -0.4 V THERMAL CHRANCTERNITICS -				-				- F
Output Voltage, Owt (Vo.)FullVI			Full	VI	V _{DD} – 0.1			v
THERMAL CHARACTERISTICS Thermal Resistance v 15.2 *C/W Gr. Junction to Case gr. Junction to Ambient Full V -25 +25 +85 *C DC SPECIFICATIONS Input Leakage Current, IL Input Clamp Voltage -16 mA 25°C V -0.8 V Differential High Level Output Voltage -16 mA 25°C V -0.8 V Differential Notput Short-Circuit Current +16 mA 25°C V +0.8 V POWER SUPPLY Vso (All) Supply Voltage V +10 µA POWER SUPPLY Vso (All) Supply Voltage With active video applied, 165 MHz, typical random pattern 25°C IV 240 280 mA Transmitter Supply Current 165 MHz, typical random pattern VI 432 504 mW TMDS Output CLK Duty Cycle 80 MHz derivative 25°C IV 13.5 165 MHz MDS Differential Output JUTE 165 MHz derivative 25°C IV 13.5 165 MHz CLK Frequency 165 MHz derivative			-				0.4	
Thermal Resistance Image: Participation of Ambient Image: Partipation of Ambient Image: Partipation of Ambien			-					
θ_x Junction to Case θ_y Junction to Ambient V 15.2 V								
θ _μ Junction to Ambient Ambient TemperaturerefuilV-57+28*CMDC SPECIFICATIONS Input Laskage Current, Ia Input Clamp Voltage-16 mA25°CVI-10+10μAInput Clamp Voltage-16 mA25°CV-0.8VV				v		15.2		°C/W
Ambient TemperatureFullV-25+25+25*25DC SPECIFICATIONS-16 mA25°CVI-10+10µAInput Camp Voltage-16 mA25°CV-0.8VVDifferential High Level Output Voltage-16 mA25°CV-0.8VVDifferential Output Short-Circuit CurrentFullVV-0.8VVPOWER SUPPLY-FullV1.01.81.89VVoo Guply Voltage Noise-FullV1.711.81.89VPower-Down CurrentWith active video applied, 165 MHz, typical random pattern25°CIV1.02.40280mAAC SPECIFICATIONS-FullV2.402.80mAMACLK Frequency165 MHz derivative25°CIV1.51.65MHzMohz Dut LCLK Duty Cycle80 MHz derivative25°CIV1.51.65MHzVors Case CLK Input Jitter165 MHz derivative25°CIV1.51.65MHzInput Data Betup Time-FullVI1.1.011.01Input Data Hold Time1.011.011.01Input Data Hold Time1.011.011.01Input Data Betup Time1.011.011.01Input Data Hold Time1.011.011.01Inp								
DC SPECIFICATIONS Input Leakage Current, I.a. Input Clamp Voltage 16 mA 25°C V 10 +10 µA Differential High Level Output Voltage 16 mA +15 mA 25°C V 0.8 V Differential Output Short-Circuit Current 16 mA +15 mA 25°C V -0.8 V POWER SUPPLY 16 mA +16 mA 25°C V -0.8 V Yoo (AII) Supply Voltage 16 mA -25°C V -0.8 V POWER SUPPLY Voo (AII) Supply Voltage V -0.8 V -0 Yoo Supply Voltage Noise Voo (AII) Supply Current With active video applied, 165 MHz, typical random pattern 25°C IV 240 280 mA AC SPECIFICATIONS CLK Frequency 165 MHz derivative 25°C IV 13.5 165 MHz Input Data Betup Time Input Data Setup Time 10 V 1 11 112 ns Input Data Hold Time Eligh Time 25°C IV 13.8			Full		-25		+85	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	-			-		. 20		-
$\begin{array}{ c c c c c c } \mbox{Input Clamp Voltage} & -16 mA & 25 °C & V & -0.8 & V \\ +16 mA & 25 °C & V & +0.8 & V \\ \mbox{Differential High Level Output Voltage} & V & AV_{CC} & V \\ \mbox{Differential Output Short-Circuit Current} & V & V & V \\ \mbox{Differential Output Short-Circuit Current} & V & V & V & V \\ \mbox{POWER SUPPLY} & V_{00} (All) Supply Voltage Noise & V & V & V & V \\ \mbox{Power-Down Current} & With active video applied, 165 MHz, typical random pattern \\ \mbox{Transmitter Supply Current} & With active video applied, 165 MHz, typical random pattern \\ \mbox{Transmitter Total Power} & V & V & V & V & V & V \\ \mbox{CLF Fequency} & 165 MHz, typical random pattern \\ \mbox{CLF Fequency} & 165 MHz derivative \\ \mbox{80 MHz derivative} & 25 °C & IV & 13.5 & V & MHz \\ \mbox{SPECIFICATIONS} & V & V & V & 13.5 & V & MHz \\ \mbox{TMDS Output CLK Duty Cycle} & 80 MHz derivative \\ \mbox{80 MHz derivative} & 25 °C & IV & 48 & V & 52 & \% \\ \mbox{Worst Case CLK Input Jitter} & I65 MHz derivative \\ \mbox{B0 MHz derivative} & 52 °C & IV & 48 & V & 52 & \% \\ \mbox{Worst Case CLK Input Jitter} & V & V & V & V & 13.5 & V & V \\ \mbox{Input Data Hold Time} & V & V & V & V & 10 & V & N \\ \mbox{TMDS Differential Swing} & V & V & V & V & 10 & V & N \\ \mbox{Vswc and Hswc Delay from DE Falling Edge } & V & V & V & V & V & 10 & 1 & V \\ \mbox{Vswc and Hswc Delay from DE Falling Edge } & V & V & V & V & V & 13.5 & V & 490 & ps \\ \mbox{High transition Time} & V & V & V & V & V & 13.5 & V & 490 & ps \\ \mbox{High to Low Transition Time} & V^{2} & AdS S/PDIF & VI & VI & 32 & V & V & 490 & ps \\ \mbox{High to Low Transition Time} & I^{2} & AdS S/PDIF & VI & $			25℃	VI	-10		+10	μА
Differential High Level Output Voltage Differential Output Short-Circuit Current+16 mA25°CV+0.8VVPOWER SUPPLY Voc (All) Supply Voltage Voc Supply Voltage Noise Power-Down CurrentFullIV1.711.81.89VYoo (All) Supply Voltage Noise Power-Down CurrentKith active video applied, 165 MHz, typical random pattern With active video applied, 165 MHz, typical random patternFullIV1.711.81.89VTransmitter Total PowerWith active video applied, 165 MHz, typical random pattern25°CIV240280mAAC SPECIFICATIONS CLK FrequencyI65 MHz derivative 80 MHz derivative25°CIV1.3.5165MHzTMDS Output CLK Duty Cycle Worst Case CLK Input Jitter Input Data Setup Time Input Data Setup Time Input Data Hold Time TMDS Differential Swing Vorwet and Hswc Delay ford DE Falling Edge Vorwet and Hswc Delay ford DE Falling Edge Lew to thigh Transition Time High to Low Transition TimeIIIIIIAUDIO AC TIMING Sample Rate IPS Setup TimeI*S and S/PDIFFullIV32II92KHzIS Setup Time IPS Setup TimeI*S and S/PDIFFullIV32II92KHz </td <td></td> <td>-16 mA</td> <td></td> <td></td> <td>10</td> <td>-0.8</td> <td></td> <td></td>		-16 mA			10	-0.8		
Differential High Level Output Voltage Differential Output Short-Circuit CurrentVVVAVccVVPOWER SUPPLY Voo Supply Voltage Noise Power-Down CurrentFullI/VI.71I.81.89VYoo (All) Supply Voltage Noise Power-Down CurrentWith active video applied, 165 MHz, typical random pattern 165 MHz, typical random patternFullVVI.71I.81.89VTransmitter Total PowerWith active video applied, 165 MHz, typical random pattern25°CIVIV240280mAAC SPECIFICATIONS CLK FrequencyI65 MHz derivative 80 MHz derivative25°CIVI.3.5I.65MHzTMDS Output CLK Duty Cycle Worst Case CLK Input JitterI65 MHz derivative 80 MHz derivative25°CIVI.3.5I.65MHzTMDS Differential Swing Vswc and Hswc Delay to DE Rising Edge Differential SwingI.64FullIVII	input clump voltage							-
Differential Output Short-Circuit CurrentImage: Circuit Current	Differential High Level Output Voltage		25 C					
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Woo Supply Voltage Noise Power-Down CurrentWith active video applied, 165 MHz, typical random pattern 165 MHz, typical random pattern Mith active video applied, 165 MHz, typical random patternFullVSoSoMV pTransmitter Supply CurrentWith active video applied, 165 MHz, typical random pattern 25° CIV240280mATransmitter Total PowerI65 MHz, typical random patternFullVI432504mWAC SPECIFICATIONS CLK FrequencyI65 MHz derivative 80 MHz derivative 25° CIV13.5I65MHzTMDS Output CLK Duty Cycle Worst Case CLK Input JitterI65 MHz derivative 80 MHz derivative 25° CIV13.552%Input Data Setup Time Input Data Setup TimeI64 Mith active video applied, 1000 Differential SwingIV1IIIIVVsinc and Hsinc Delay from DE Falling Edge Differential Output SwingIIIIV1IVIVIVIVDE Low TimeIIIIVIIV			Eull	N/	1 71	1 0	1 90	V
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$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		With active video applied	-			0	50	
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And the set of t	CLK Frequency	165 MHz derivative	25°C	IV	13.5		165	MHz
TMDS Output CLK Duty Cycle25°CIV48529%Worst Case CLK Input JitterFullIVI2nsInput Data Setup TimeFullIV1111Input Data Hold TimeFullIV1010001200MVVSWc and Hswc Delay from DE Falling EdgeVVI11111111VSWc and Hswc Delay to DE Rising EdgeVIVI1111111111DE High TimeFuel No25°CVII11					13.5			
Worst Case CLK Input JitterFullIV12nsInput Data Setup TimeInput Data Hold TimeFullIV11nsInput Data Hold TimeFullIV11nsTMDS Differential SwingVI80010001200mVVsrnc and Hsrnc Delay from DE Falling EdgeVI1UI2UI2Vsrnc and Hsrnc Delay to DE Rising EdgeVI1UI2UI2DE High Time25°CVI1UI2UI2DE Low Time25°CVI138U12Differential Output Swing25°CVI75490psLow to High Transition Time25°CVI75490psAUDIO AC TIMINGI2S and S/PDIFFullIV32192KHzI2S Setup TimeI2S and S/PDIFFullIV321U12I2S Setup TimeI2S°CIV11U12	TMDS Output CLK Duty Cycle		25°C	IV	48		52	%
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TMDS Differential Swing Image: style s			Full	IV				
Vsrnc and Hsrnc Delay from DE Falling EdgeIIIIIIIIVsrnc and Hsrnc Delay to DE Rising EdgeIIIIIIIIIIIDE High TimeISoftVIIIIIIIIIIIIIIDE Low TimeIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII	-				800	1000	1200	
Vsrnc and Hsrnc Delay to DE Rising EdgeVI1Ul2DE High Time25°CVI8191Ul2DE Low Time25°CVI138Ul2Differential Output SwingLow to High Transition Time25°CVII75490psHigh to Low Transition Time25°CVII75490psAUDIO AC TIMING12S and S/PDIFFullIV32192KHzI²S Setup Time25°CIV110I21110I2I²S Setup TimeI²S Setup Time1112112I²S Setup Time15ns	-					1		
DE High Time25°CVI8191Ul²DE Low Time25°CVI138Ul²Differential Output SwingLow to High Transition Time25°CVII75490psHigh to Low Transition Time25°CVII75490psAUDIO AC TIMINGSample RateI²S and S/PDIFFullIV32192kHzI²S Setup Time-25°CIV-1Ul²I²S Setup TimeI²S Setup Time15ns-						1		
DE Low Time25°CVI138Ul²Differential Output Swing <td< td=""><td></td><td></td><td>25°C</td><td></td><td></td><td></td><td>8191</td><td></td></td<>			25°C				8191	
Differential Output SwingImage: space of the	-					138		
Low to High Transition Time 25°C VII 75 490 ps High to Low Transition Time 25°C VII 75 490 ps AUDIO AC TIMING r								-
High to Low Transition Time 25°C VII 75 490 ps AUDIO AC TIMING - <t< td=""><td></td><td></td><td>25℃</td><td>VII</td><td>75</td><td></td><td>490</td><td>ps</td></t<>			25℃	VII	75		490	ps
AUDIO AC TIMINGI2S and S/PDIFFullIV32192kHzSample RateI2S and S/PDIFFullIV32192kHzI2S Cycle Time25°CIV1UI2I2S Setup Time25°CIV15ns	-							
Sample Rate I ² S and S/PDIF Full IV 32 192 kHz I ² S Cycle Time 25°C IV 10 11 Ul ² I ² S Setup Time I 25°C IV 15 ns					-			1
I ² S Cycle Time 25°C IV 1 UI ² I ² S Setup Time 25°C IV 15 ns		I ² S and S/PDIF	Full	IV	32		192	kHz
l ² S Setup Time 25°C IV 15 ns	•							
	-					15	•	
Audio Pipeline Delay 25°C IV 75 µs								

 1 See Explanation of Test Levels section. 2 UI = unit interval.

ABSOLUTE MAXIMUM RATINGS

Table 2.

1 4010 20	
Parameter	Rating
Digital Inputs	+5.5 V to -0.3 V
Digital Output Current	20 mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

EXPLANATION OF TEST LEVELS

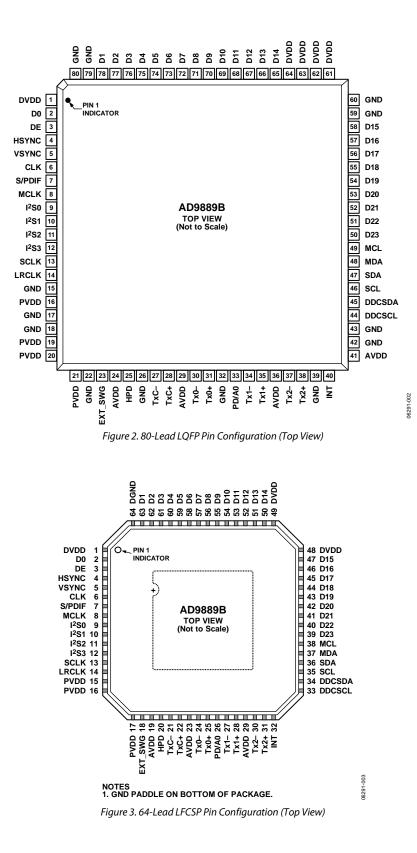
- I. 100% production tested.
- II. 100% production tested at 25°C and sample tested at specified temperatures.
- III. Sample tested only.
- IV. Parameter is guaranteed by design and characterization testing.
- V. Parameter is a typical value only.
- VI. 100% production tested at 25°C; guaranteed by design and characterization testing.
- VII. Limits defined by HDMI specification; guaranteed by design and characterization testing.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



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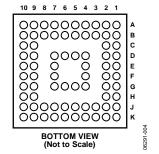


Figure 4. 76-Ball BGA Configuration (Top View)

Table 3. Pin Function Descriptions

Pin No.					
BGA	LFCSP	LQFP	Mnemonic	Type ¹	Description
D10, D9, C10, C9, A10, B10, A9, B9, A8, B8, A7, B7, A6, B6, A5, B5, A4, B4, A3, B3, A2, B2, A1, B1	39 to 47, 50 to 63, 2	50 to 58, 65 to 78, 2	D[23:0]	1	Video Data Input. Digital input in RGB or YCbCr format. Supports CMOS logic levels from 1.8 V to 3.3 V.
D1	6	6	CLK	1	Video Clock Input. Supports CMOS logic levels from 1.8 V to 3.3 V.
C2	3	3	DE	I	Data Enable Bit for Digital Video. Supports CMOS logic levels from 1.8 V to 3.3 V.
C1	4	4	HSYNC	I	Horizontal Sync Input. Supports CMOS logic levels from 1.8 V to 3.3 V.
D2	5	5	VSYNC	I	Vertical Sync Input. Supports CMOS logic levels from 1.8 V to 3.3 V.
J3	18	23	EXT_SWG	I	Sets Internal Reference Currents. Place 887 Ω resistor (1% tolerance) between this pin and ground.
К3	20	25	HPD	I	Hot Plug Detect Signal. This indicates to the interface whether the receiver is connected. Supports 1.8 V to 5.0 V CMOS logic levels.
E2	7	7	S/PDIF	I	S/PDIF (Sony/Philips Digital Interface) Audio Input. This is the audio input from a Sony/Philips digital interface. Supports CMOS logic levels from 1.8 V to 3.3 V.
E1	8	8	MCLK	1	Audio Reference Clock. $128 \times N \times f_s$ with N = 1, 2, 3, or 4. Set to $128 \times sampling$ frequency (f_s), $256 \times f_s$, $384 \times f_s$, or $512 \times f_s$. Supports 1.8 V to 3.3 V CMOS logic levels.
F2, F1, G2, G1	9 to 12	9 to 12	I ² S[3:0]	I	I ² S Audio Data Inputs. These represent the eight channels of audio (two per input) available through I ² S. Supports CMOS logic levels from 1.8 V to 3.3 V.
H2	13	13	SCLK	1	I ² S Audio Clock. Supports CMOS logic levels from 1.8 V to 3.3 V.
H1	14	14	LRCLK	I	Left/Right Channel Selection. Supports CMOS logic levels from 1.8 V to 3.3 V.
J7 ²	26 ²	33 ²	PD/A0	I	Power-Down Control and I ² C Address Selection. The I ² C address and the PD polarity are set by the PD/A0 pin state when the supplies are applied to the AD9889B. Supports 1.8 V to 3.3 V CMOS logic levels.
K1, K2	21, 22	27, 28	TxC-/TxC+	0	Differential Clock Output. Differential clock output at pixel clock rate; supports TMDS logic level.
K10, J10	30, 31	37, 38	Tx2-/Tx2+	0	Differential Output Channel 2. Differential output of the red data at 10× the pixel clock rate; supports TMDS logic level.

Data Sheet

	Pin No.				
BGA	LFCSP	LQFP	Mnemonic	Type ¹	Description
K7, K8	27, 28	34, 35	Tx1-/Tx1+	0	Differential Output Channel 1. Differential output of the green data at 10× the pixel clock rate; supports TMDS logic level.
K4, K5	24, 25	30, 31	Tx0-/Tx0+	0	Differential Output Channel 0. Differential output of the blue data at 10× the pixel clock rate; TMDS logic level.
H10	32	40	INT	0	Interrupt. Open drain. A 2 k Ω pull-up resistor to the microcontroller I/O supply is recommended.
J2, J5, J8, K9	19, 23, 29	24, 29, 36, 41	AVDD	Р	1.8 V Power Supply for TMDS Outputs.
D5, D6, D7, E7	1, 48, 49	1, 61, 62, 63, 64	DVDD	Р	1.8 V Power Supply for Digital and I/O Power Supply. These pins supply power to the digital logic and I/Os. They should be filtered and as quiet as possible.
G4, G5, J1	15, 16, 17,	16, 19, 20, 21	PVDD	Ρ	1.8 V PLL Power Supply. The most sensitive portion of the AD9889B is the clock generation circuitry. These pins provide power to the clock PLL. The designer should provide quiet, noise-free power to these pins.
D4, E4, F4, J4, G6, J6, K6, F7, G7, H9, J9	N/A	15, 17, 18, 22, 26, 32, 39, 42, 43, 59, 60, 79, 80	GND	Р	Ground. The ground return for all circuitry on-chip. For best practice, assemble the AD9889B on a single, solid ground plane with careful attention given to ground current paths.
N/A	64, paddle on bottom side	N/A	DGND	Ρ	Digital Ground. The ground return for all circuitry on-chip. For best practice, assemble the AD9889B on a single, solid ground plane with careful attention given to ground current paths.
F9	36	47	SDA	C ³	Serial Port Data I/O. This pin serves as the serial port data I/O slave for register access. Supports CMOS logic levels from 1.8 V to 3.3 V.
F10	35	46	SCL	C ³	Serial Port Data Clock. This pin serves as the serial port data clock slave for register access. Supports CMOS logic levels from 1.8 V to 3.3 V.
E10	37	48	MDA	C ³	Serial Port Data I/O Master to HDCP Key EEPROM. Supports CMOS logic levels from 1.8 V to 3.3 V.
E9	38	49	MCL	C ³	Serial Port Data Clock Master to HDCP Key EEPROM. Supports CMOS logic levels from 1.8 V to 3.3 V.
G9	34	45	DDCSDA	C ³	Serial Port Data I/O to Receiver. This pin serves as the master to the DDC bus. Supports a 5 V CMOS logic level.
G10	33	44	DDCSCL	C ³	Serial Port Data Clock to Receiver. This pin serves as the master clock for the DDC bus. Supports a 5 V CMOS logic level.

¹ I = input, O = output, P = power supply, C = control.
 ² Pin J7 (BGA), Pin 26 (LFCSP), and Pin 33 (LQFP) are dual function pins: I²C selection and power-down control. The I²C selection function occurs at power-up; the power-down control function occurs whenever the state of the pin is changed from its original state at power-up.
 ³ For a full description of the 2-wire serial interface and its functionality, obtain documentation by contacting NDA from ATV_VideoTx_Apps@analog.com.

APPLICATIONS INFORMATION

DESIGN RESOURCES

Analog Devices, Inc. evaluation kits, reference design schematics, and other support documentation are available under the nondisclosure agreement (NDA) from ATV_VideoTx_Apps@analog.com.

Other resources include:

EIA/CEA-861B, which describes audio and video infoframes as well as the E-EDID structure for HDMI. It is available from Consumer Electronics Association (CEA).

The *HDMI v. 1.3*, a defining document for HDMI Version 1.3, and the *HDMI Compliance Test Specification Version 1.3* are available from HDMI Licensing, LLC.

The *HDCP v. 1.2* is the defining document for HDCP Version 1.2 available from Digital Content Protection, LLC.

DOCUMENT CONVENTIONS

In this data sheet, data is represented using the conventions described in Table 4.

Table 4. Document Conventions

Data Type	Format
0xNN	Hexadecimal (Base-16) numbers are represented using the C language notation, preceded by 0x.
0bNN	Binary (Base-2) numbers are represented using the C language notation, preceded by 0b.
NN	Decimal (Base-10) numbers are represented using no additional prefixes or suffixes.
Bit	Bits are numbered in little endian format, that is, the least significant bit of a byte or word is referred to as Bit 0.

PCB LAYOUT RECOMMENDATIONS

The AD9889B is a high precision, high speed analog device. As such, to obtain the maximum performance from the part, it is important to have a well laid out board.

POWER SUPPLY BYPASSING

It is recommended to bypass each power supply pin with a 0.1 μ F capacitor. The exception is when two or more supply pins are adjacent to each other. For these groupings of powers/grounds, it is necessary to have only one bypass capacitor. The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power pin. Also, avoid placing the capacitor on the opposite side of the PC board from the AD9889B, as that interposes resistive vias in the path.

The bypass capacitors should be physically located between the power plane and the power pin. Current should flow from the power plane to the capacitor to the power pin. Do not make a power connection between the capacitor and the power pin. Placing a via underneath the capacitor pads, down to the power plane, is generally the best approach.

It is particularly important to maintain low noise and good stability of PVDD (the PLL supply). Abrupt changes in PVDD can result in similarly abrupt changes in sampling clock phase and frequency. This can be avoided by careful attention to regulation, filtering, and bypassing. It is best practice to provide separate regulated supplies for each of the analog circuitry groups (AVDD and PVDD).

It is also recommended to use a single ground plane for the entire board. Experience has repeatedly shown that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

DIGITAL INPUTS

Video and Audio Data Input Signals

The digital inputs on the AD9889B are designed to work with signals ranging from 1.8 V to 3.3 V logic levels. Therefore, no extra components need to be added when using 3.3 V logic. Any noise that gets onto the clock input (labeled CLK) trace adds jitter to the system. Therefore, minimize the video clock input (Pin 6: CLK) trace length and do not run any digital or other high frequency traces near it. Make sure to match the length of the input data signals to optimize data capture, especially for high frequency modes such as 1080p, UXGA, and double data rate input formats.

Other Input Signals

The HPD must be connected to the HDMI connector. A 10 k Ω pull-down resistor to ground is also recommended.

The PD/A0 input pin can be connected to GND or supply (through a resistor or a control signal). The device address and power-down polarity are set by the state of the PD/A0 pin when the AD9889B supplies are applied/enabled. For example, if the PD/A0 pin is low (when the supplies are turned on), then the device address is 0x72 and the power-down is active high. If the PD/A0 pin is high (when the supplies are turned on), the device address is 0x7A and the power-down is active low.

The SCL and SDA pins should be connected to the I²C master. A pull-up resistor of 2 k Ω to 1.8 V or 3.3 V is recommended.

EXTERNAL SWING RESISTOR

The external swing resistor must be connected directly to the EXT_SWG pin and ground. The external swing resistor must have a value of 887 Ω (±1% tolerance). Avoid running any high speed ac or noisy signals next to, or close to, the EXT_SWG pin.

OUTPUT SIGNALS

TMDS Output Signals

The AD9889B has three TMDS data channels (0, 1, and 2) that output signals up to 800 MHz as well as the TMDS output data clock. To minimize the channel-to-channel skew, make the trace length of these signals the same. Additionally, these traces need to have a 50 Ω characteristic impedance and need to be routed as 100 Ω differential pairs. Best practice recommends routing these lines on the top PCB layer to avoid the use of vias.

Other Output Signals (non TMDS)

DDCSCL and DDCSDA

The DDCSCL and DDCSDA outputs need to have a minimum amount of capacitance loading to ensure the best signal integrity. The DDCSCL and DDCSDA capacitance loading must be less than 50 pF to meet the HDMI compliance specification. The DDCSCL and DDCSDA must be connected to the HDMI connector and a pull-up resistor to 5 V is required. The pull-up resistor must have a value between 1.5 k Ω and 2 k Ω .

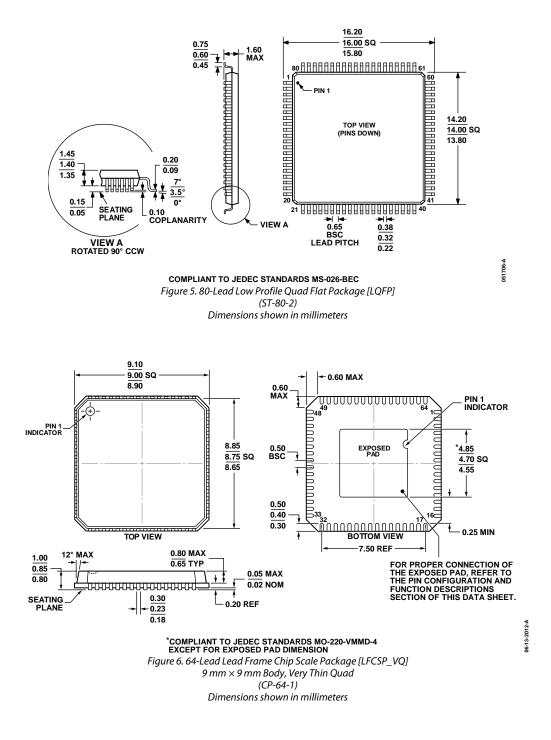
INT Pin

The INT pin is an output that should be connected to the microcontroller of the system. A pull-up resistor to 1.8 V or 3.3 V is required for proper operation—the recommended value is $2 \text{ k}\Omega$.

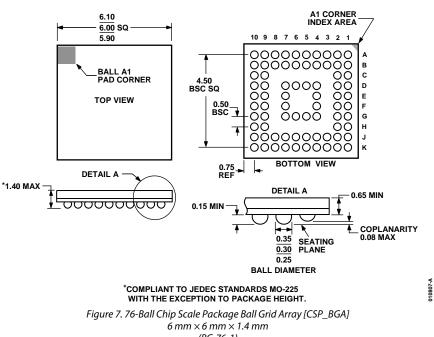
MCL and MDA

The MCL and MDA outputs should be connected to the EEPROM containing the HDCP key (if HDCP is implemented). Pull-up resistors of 2 k Ω are recommended.

OUTLINE DIMENSIONS



Data Sheet



(BC-76-1) Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
AD9889BBCPZ-80	–25°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-1
AD9889BBCPZ-165	–25°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-1
AD9889BBSTZ-80	–25°C to +85°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-2
AD9889BBSTZ-165	–25°C to +85°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-2
AD9889BBBCZ-80	–25°C to +85°C	76-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-76-1
AD9889BBBCZRL-80	–25°C to +85°C	76-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-76-1

¹ Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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