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9/07—Rev. A to Rev B

Change to Current Noise Density in Table 1 3

12/06—Rev. 0 to Rev. A

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Updated Outline Dimensions 13
Changes to Ordering Guide 14

10/99—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

5 V ≤ V_S ≤ 18 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.[1]

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1.0	2.5	mV
		−20°C ≤ T_A ≤ +85°C			3	mV
Input Bias Current	I_B			80	400	nA
		−20°C ≤ T_A ≤ +85°C			500	nA
Input Offset Current	I_{OS}			5	100	nA
		−20°C ≤ T_A ≤ +85°C			200	nA
Input Voltage Range			0		V_S	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to V_S	60	75		dB
Voltage Gain	A_{VO}	V_{OUT} = 0.5 V to V_S − 0.5 V, R_L = 10 kΩ	10	150		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{LOAD} = 10 mA	V_S − 0.15			V
Output Voltage Low	V_{OL}	I_{LOAD} = 10 mA		65	150	mV
Output Short-Circuit Current	I_{SC}		35	70		mA
		−20°C ≤ T_A ≤ +85°C	30			mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.25 V to ±9.25 V	80	110		dB
Supply Current/Amplifier	I_{SY}			0.8	1.1	mA
		−20°C ≤ T_A ≤ +85°C			1.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	C_L = 200 pF		7.5		V/µs
Gain Bandwidth Product	GBP			5.5		MHz
Phase Margin	Φo			65		Degrees
Settling Time	t_S	0.01%, 10 V step		3		µs
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		12		nV/√Hz
	e_n	f = 10 kHz		11		nV/√Hz
Current Noise Density	i_n	f = 10 kHz		1		pA/√Hz

[1] All typical values are for V_S = 18 V.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	20 V
Input Voltage	GND to V_S
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−20°C to +85°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
5-Lead SOT-23 (RJ)	230	140	°C/W
14-Lead TSSOP (RU)	180	35	°C/W
14-Lead SOIC (R)	120	56	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

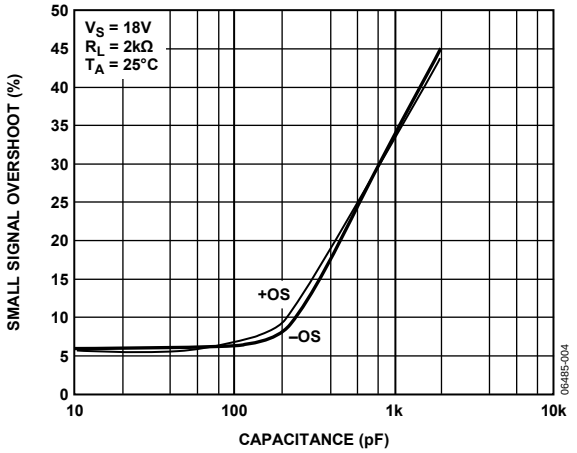

Figure 4. Small Signal Overshoot vs. Load Capacitance

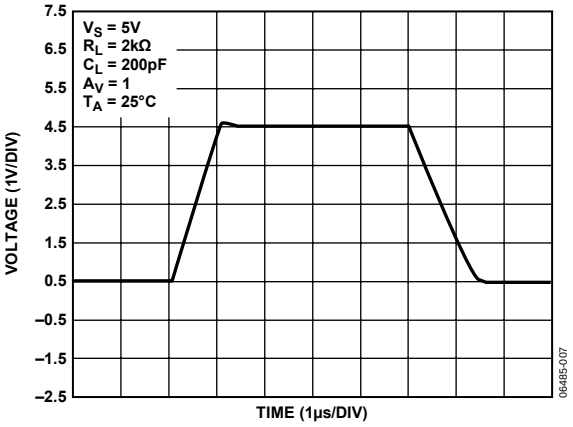

Figure 7. Large Signal Transient Response, V_S = 5 V

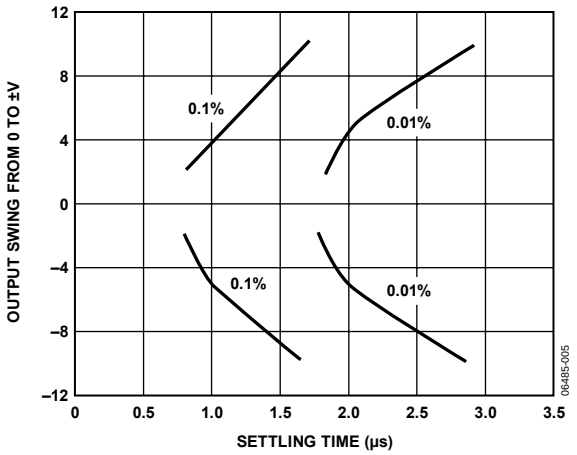

Figure 5. Output Swing vs. Settling Time

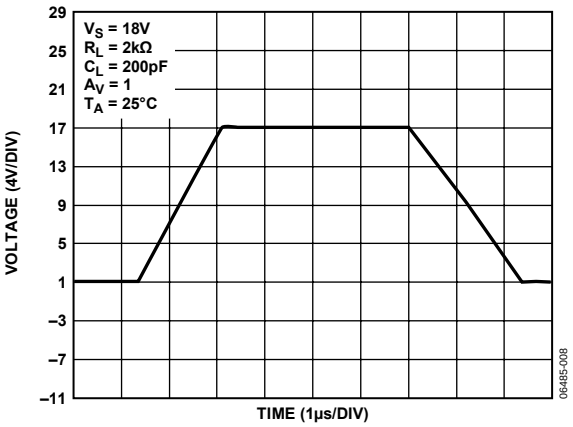

Figure 8. Large Signal Transient Response, V_S = 18 V

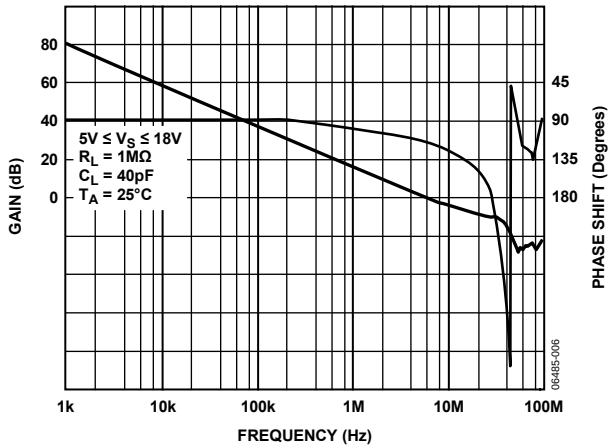

Figure 6. Open-Loop Gain and Phase Shift vs. Frequency

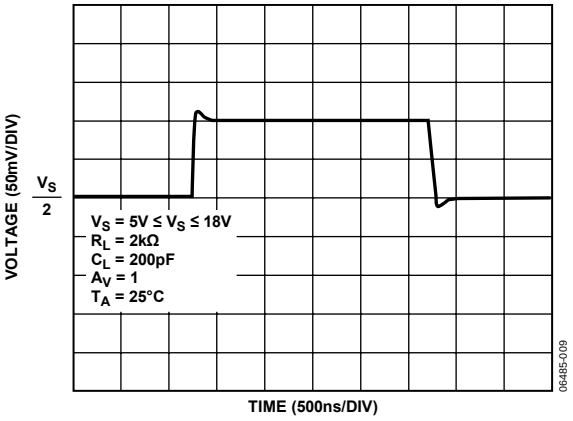

Figure 9. Small Signal Transient Response

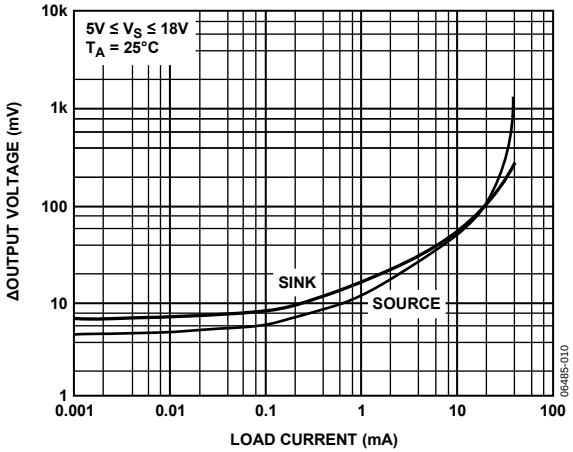

Figure 10. Output Voltage to Supply Rail vs. Load Current

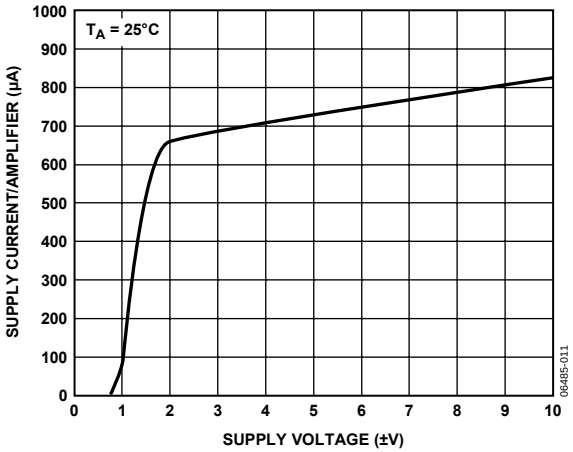

Figure 11. Supply Current vs. Supply Voltage

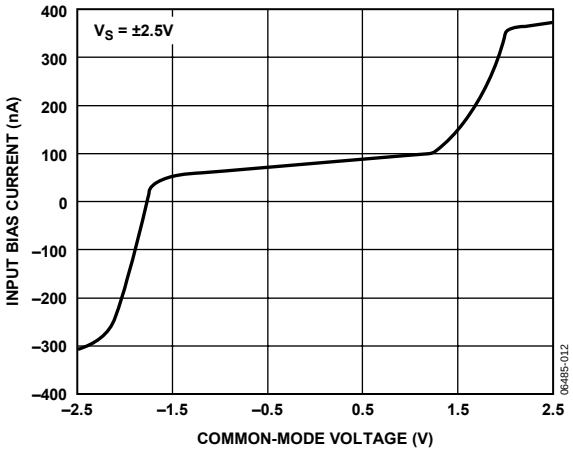

Figure 12. Input Bias Current vs. Common-Mode Voltage, V_S = ±2.5 V

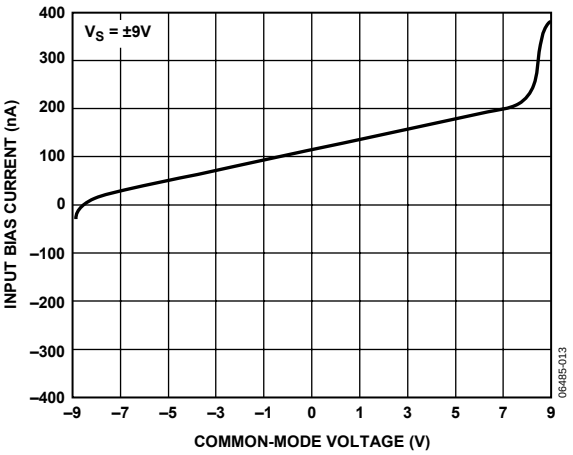

Figure 13. Input Bias Current vs. Common-Mode Voltage, V_S = ±9 V

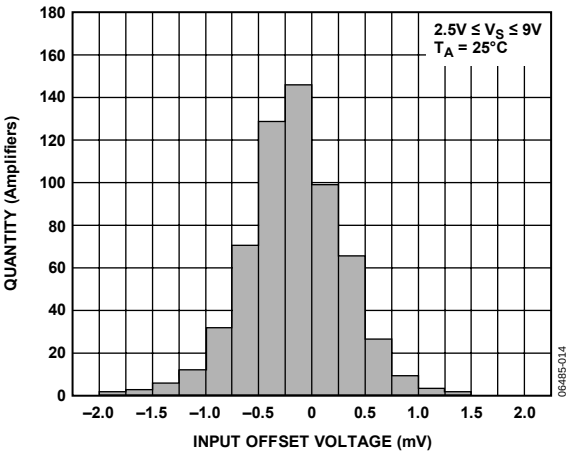

Figure 14. Input Offset Voltage Distribution

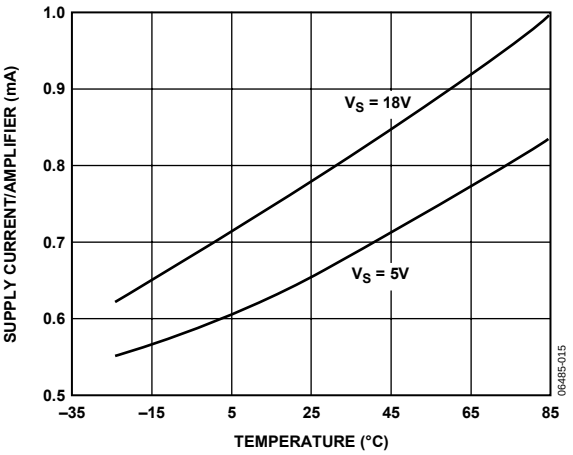

Figure 15. Supply Current vs. Temperature

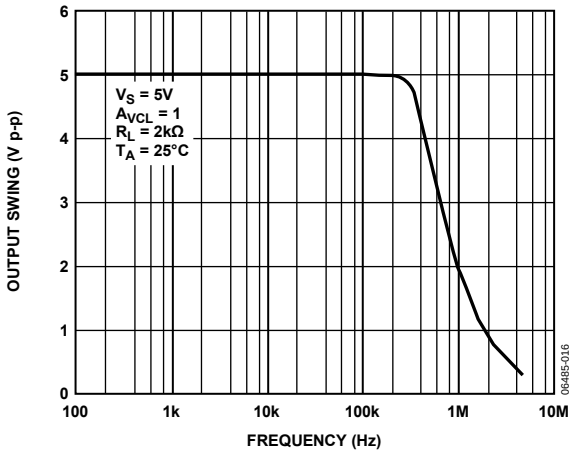

Figure 16. Maximum Output Swing vs. Frequency, V_S = 5 V

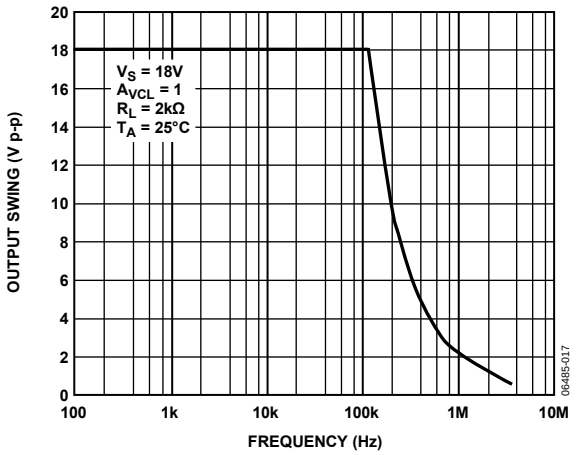

Figure 17. Maximum Output Swing vs. Frequency, V_S = 18 V

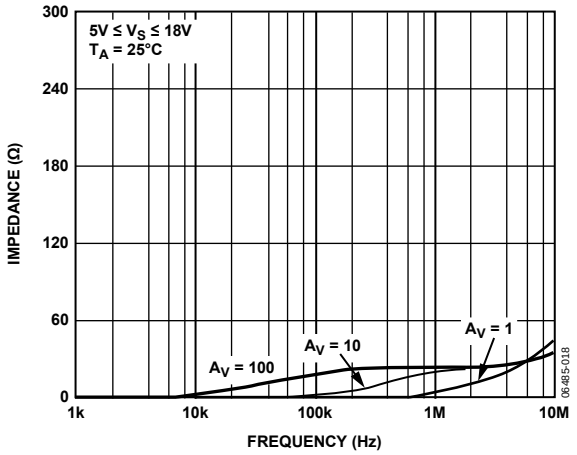

Figure 18. Closed-Loop Output Impedance vs. Frequency

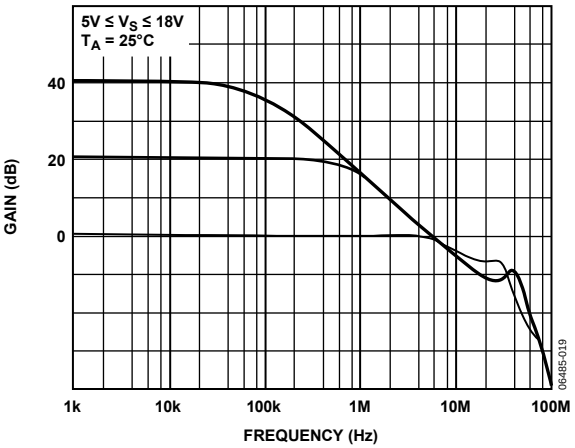

Figure 19. Closed-Loop Gain vs. Frequency

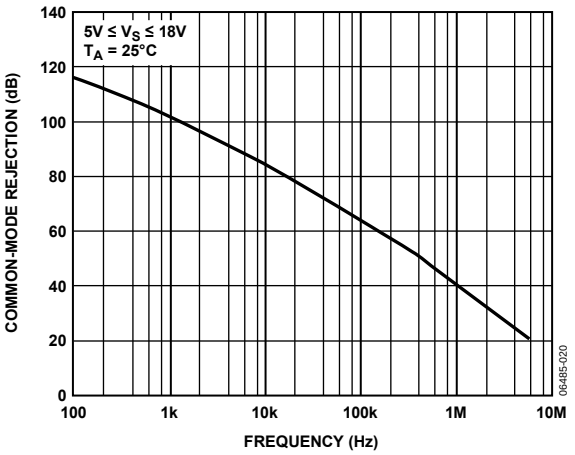

Figure 20. Common-Mode Rejection vs. Frequency

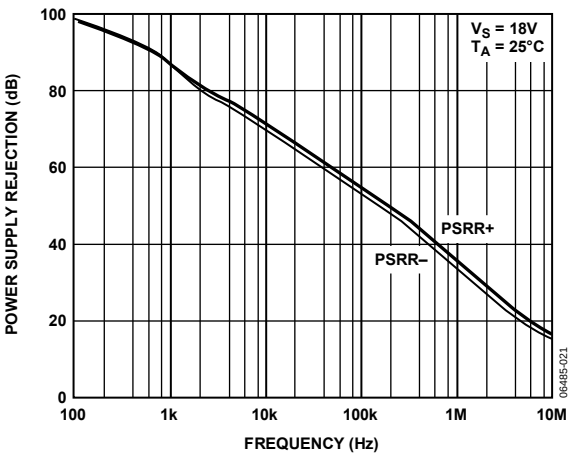

Figure 21. Power Supply Rejection vs. Frequency

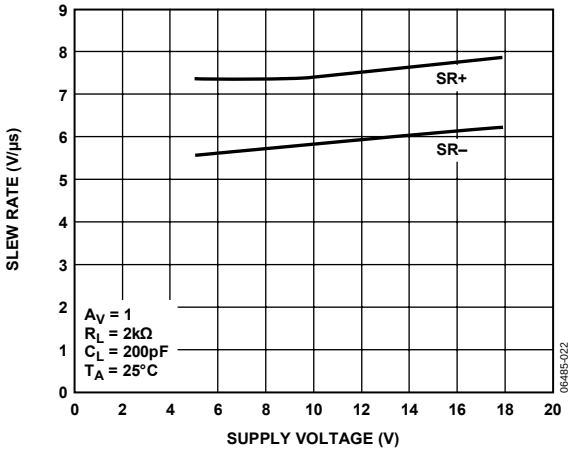

Figure 22. Slew Rate vs. Supply Voltage

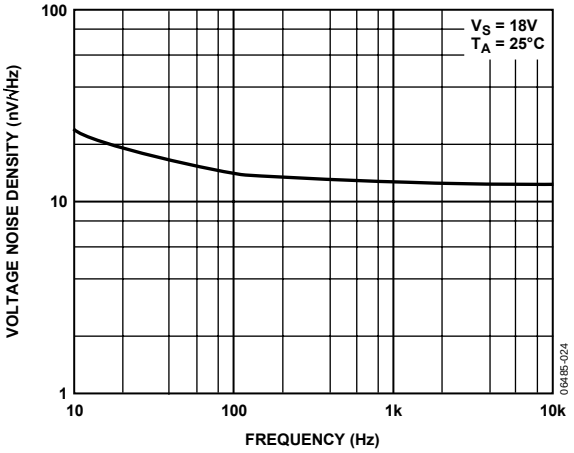

Figure 24. Voltage Noise Density vs. Frequency, V_S = 18 V

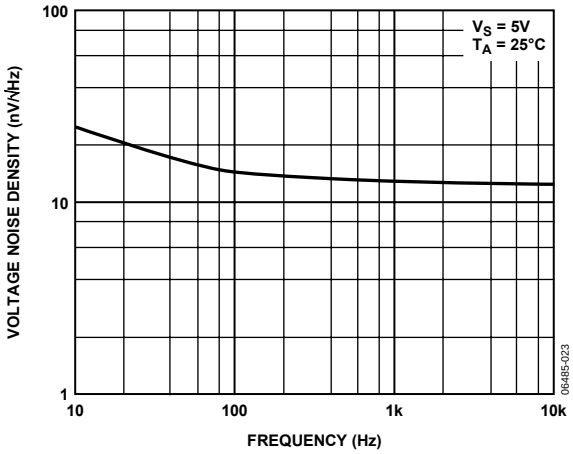

Figure 23. Voltage Noise Density vs. Frequency, V_S = 5 V

THEORY OF OPERATION

The AD8614/AD8644 are processed using Analog Devices high voltage, extra fast complementary bipolar (HV XFCB) process. This process includes trench-isolated transistors that lower parasitic capacitance.

Figure 26 shows a simplified schematic of the AD8614/AD8644. The input stage is rail-to-rail, consisting of two complementary differential pairs, one NPN pair and one PNP pair. The input stage is protected against avalanche breakdown by two back-to-back diodes. Each input has a 1.5 kΩ resistor that limits input current during overvoltage events and furnishes phase reversal protection if the inputs are exceeded. The two differential pairs are connected to a double-folded cascode. This is the stage in the amplifier with the most gain. The double-folded cascode differentially feeds the output stage circuitry. Two complementary common emitter transistors are used as the output stage. This allows the output to swing to within 125 mV from each rail with a 10 mA load. The gain of the output stage, and thus the open-loop gain of the op amp, depends on the load resistance.

The AD8614/AD8644 have no built-in short-circuit protection. The short-circuit limit is a function of high current roll-off of the output stage transistors and the voltage drop over the resistor shown on the schematic at the output stage. The voltage over this resistor is clamped to one diode during short-circuit voltage events.

OUTPUT SHORT-CIRCUIT PROTECTION

To achieve a wide bandwidth and high slew rate, the output of the AD8614/AD8644 is not short-circuit protected. Shorting the output directly to ground or to a supply rail can destroy the device. The typical maximum safe output current is 70 mA.

In applications where some output current protection is needed, but not at the expense of reduced output voltage headroom, a low value resistor in series with the output can be used. This is shown in Figure 25. The resistor is connected within the feedback loop of the amplifier so that if V_{OUT} is shorted to ground and V_{IN} swings up to 18 V, the output current does not exceed 70 mA.

For 18 V single-supply applications, resistors less than 261 Ω are not recommended.

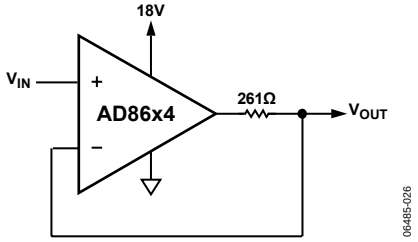

Figure 25. Output Short-Circuit Protection

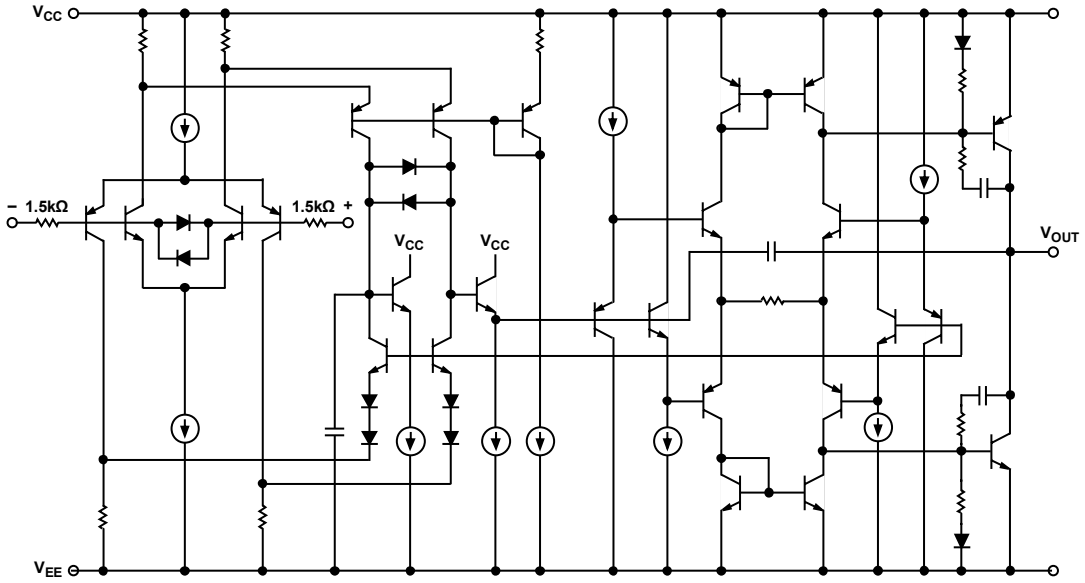

Figure 26. Simplified Schematic

INPUT OVERVOLTAGE PROTECTION

As with any semiconductor device, whenever the condition exists for the input to exceed either supply voltage, attention needs to be paid to the input overvoltage characteristic. As an overvoltage occurs, the amplifier can be damaged, depending on the voltage level and the magnitude of the fault current. When the input voltage exceeds either supply by more than 0.6 V, internal pin junctions energize, allowing current to flow from the input to the supplies. Observing Figure 26, the AD8614/AD8644 have 1.5 kΩ resistors in series with each input, which helps to limit the current. This input current is not inherently damaging to the device as long as it is limited to 5 mA or less. If the voltage is large enough to cause more than 5 mA of current to flow, an external series resistor should be added. The size of this resistor is calculated by dividing the maximum overvoltage by 5 mA and subtracting the internal 1.5 kΩ resistor. For example, if the input voltage could reach 100 V, the external resistor should be (100 V ÷ 5 mA) – 1.5 kΩ = 18.5 kΩ. This resistance should be placed in series with either or both inputs if they are subjected to the overvoltages.

OUTPUT PHASE REVERSAL

The AD8614/AD8644 are immune to phase reversal as long as the input voltage is limited to within the supply rails. Although the device's output does not change phase, large currents due to input overvoltage can result, damaging the device. In applications where the possibility of an input voltage exceeding the supply voltage exists, overvoltage protection should be used, as described in the previous section.

POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8614/AD8644 is limited by the associated rise in junction temperature. The maximum safe junction temperature is 150°C, and should not be exceeded or device performance could suffer. If this maximum is momentarily exceeded, proper circuit operation is restored as soon as the die temperature is reduced. Leaving the device in an overheated condition for an extended period can result in permanent damage to the device.

To calculate the internal junction temperature of the AD8614/AD8644, the following formula can be used:

$$T_J = P_{DISS} \times \theta_{JA} + T_A$$

where:

T_J is the AD8614/AD8644 junction temperature.
P_{DISS} is the AD8614/AD8644 power dissipation.
θ_{JA} is the AD8614/AD8644 junction-to-ambient package thermal resistance.
T_A is the ambient temperature of the circuit.

The power dissipated by the device can be calculated as:

$$P_{DISS} = I_{LOAD} \times (V_S - V_{OUT})$$

where:

I_{LOAD} is the AD8614/AD8644 output load current.
V_S is the AD8614/AD8644 supply voltage.
V_{OUT} is the AD8614/AD8644 output voltage.

Figure 27 provides a convenient way to determine if the device is being overheated. The maximum safe power dissipation can be found graphically, based on the package type and the ambient temperature around the package. By using the previous equation, it is a simple matter to see if P_{DISS} exceeds the device's power derating curve. To ensure proper operation, it is important to observe the recommended derating curves shown in Figure 27.

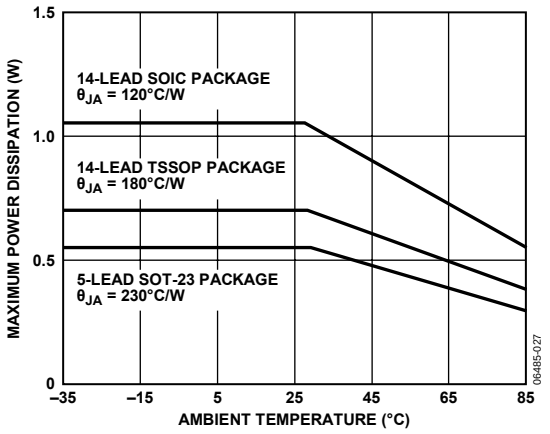

Figure 27. Maximum Power Dissipation vs. Temperature (5-Lead and 14-Lead Package Types)

UNUSED AMPLIFIERS

It is recommended that any unused amplifiers in the quad package be configured as a unity-gain follower with a 1 kΩ feedback resistor connected from the inverting input to the output, and the noninverting input tied to the ground plane.

CAPACITIVE LOAD DRIVE

The AD8614/AD8644 exhibit excellent capacitive load driving capabilities. Although the device is stable with large capacitive loads, there is a decrease in amplifier bandwidth as the capacitive load increases.

When driving heavy capacitive loads directly from the AD8614/AD8644 output, a snubber network can be used to improve the transient response. This network consists of a series R-C connected from the amplifier's output to ground, placing it in parallel with the capacitive load. The configuration is shown in Figure 28. Although this network does not increase the bandwidth of the amplifier, it does significantly reduce the amount of overshoot.

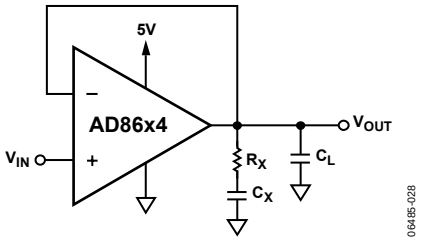

Figure 28. Snubber Network Compensation for Capacitive Loads

The optimum values for the snubber network should be determined empirically based on the size of the capacitive load. Table 4 shows a few sample snubber network values for a given load capacitance.

Table 4. Snubber Networks for Large Capacitive Loads

Load Capacitance (C_L)	Snubber Network (R_X, C_X)
0.47 nF	300 Ω, 0.1 µF
4.7 nF	30 Ω, 1 µF
47 nF	5 Ω, 10 µF

DIRECT ACCESS ARRANGEMENT

Figure 29 shows a schematic for a 5 V single-supply transmit/receive telephone line interface for 600 Ω transmission systems. It allows full duplex transmission of signals on a transformer-coupled 600 Ω line. Amplifier A1 provides gain that can be adjusted to meet the modem's output drive requirements. Both A1 and A2 are configured to apply the largest possible differential signal to the transformer. The largest signal available on a single 5 V supply is approximately 4.0 V p-p into a 600 Ω transmission system. Amplifier A3 is configured as a difference amplifier to extract the receive information from the transmission line for amplification by A4. A3 also prevents the transmit signal from interfering with the receive signal. The gain of A4 can be adjusted in the same manner as A1 to meet the modem input signal requirements. Standard resistor values permit the use of single in-line package (SIP) format resistor arrays. Couple this with the AD8644 14-lead SOIC or TSSOP package and this circuit can offer a compact solution.

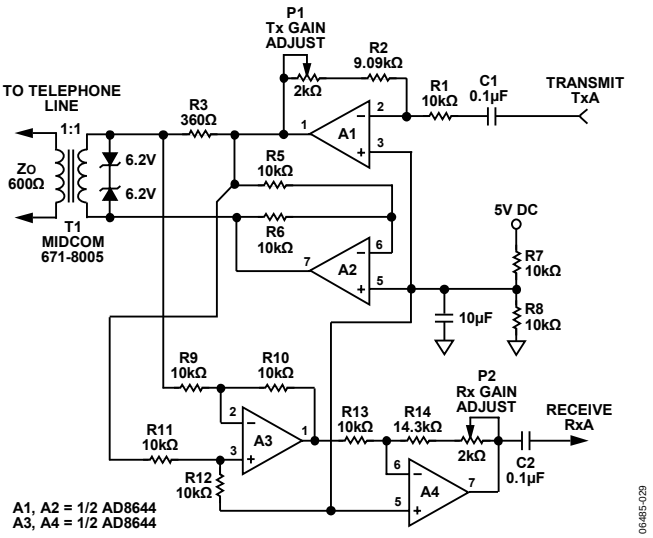

Figure 29. A Single-Supply Direct Access Arrangement for Modems

A ONE-CHIP HEADPHONE/MICROPHONE PREAMPLIFIER SOLUTION

Because of its high output current performance, the AD8644 makes an excellent amplifier for driving an audio output jack in a computer application. Figure 30 shows how the AD8644 can be interfaced with an ac codec to drive headphones or speakers.

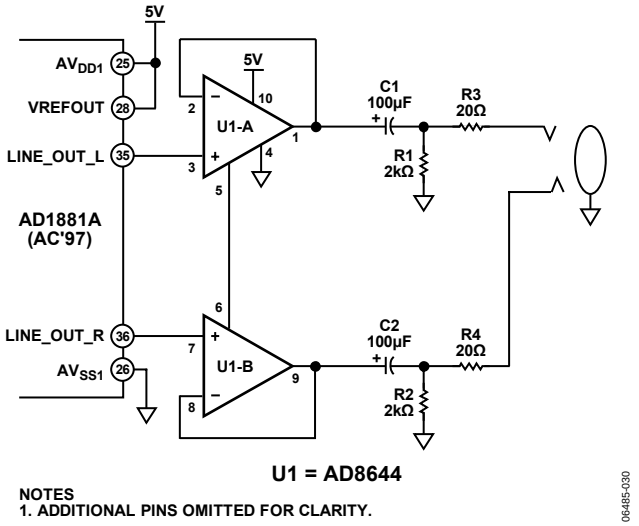

Figure 30. A PC-99-Compliant Headphone/Line Out Amplifier

If gain is required from the output amplifier, four additional resistors should be added as shown in Figure 31.

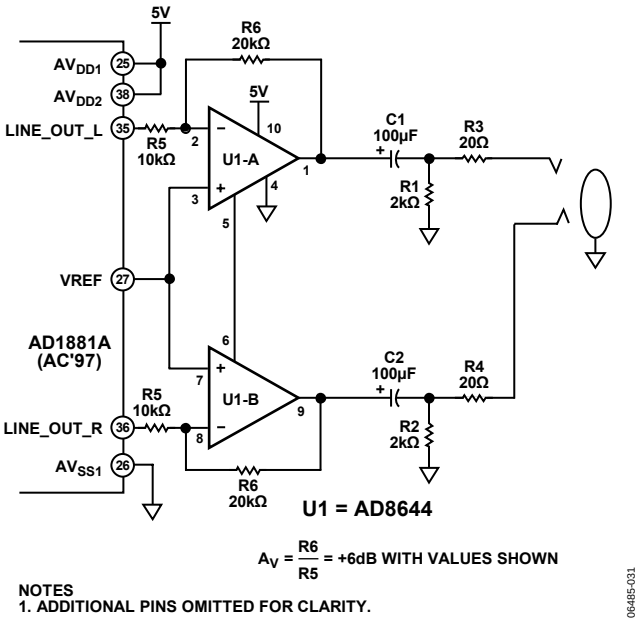

Figure 31. A PC-99-Compliant Headphone/Speaker Amplifier with Gain

The gain of the AD8644 can be set as

$$A_V = \frac{R6}{R5}$$

Input coupling capacitors are not required for either circuit as the reference voltage is supplied from the AD1881A.

The resistors R4 and R5 help protect the AD8644 output in case the output jack or headphone wires are accidentally shorted to ground. The output coupling capacitors C1 and C2 block dc current from the headphones and create a high-pass filter with a corner frequency of

$$f_{-3\,dB} = \frac{1}{2\pi C1(R4 + R_L)}$$

where R_L is the resistance of the headphones.

The remaining two amplifiers can be used as low voltage microphone preamplifiers. A single AD8614 can be used as a standalone microphone preamplifier. Figure 32 shows this implementation.

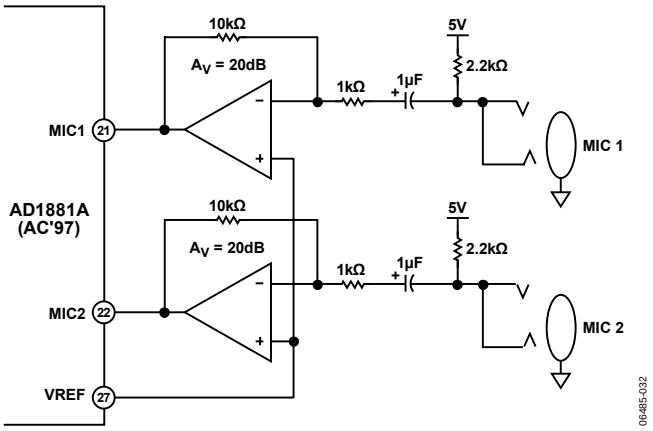

Figure 32. Microphone Preamplifier

OUTLINE DIMENSIONS

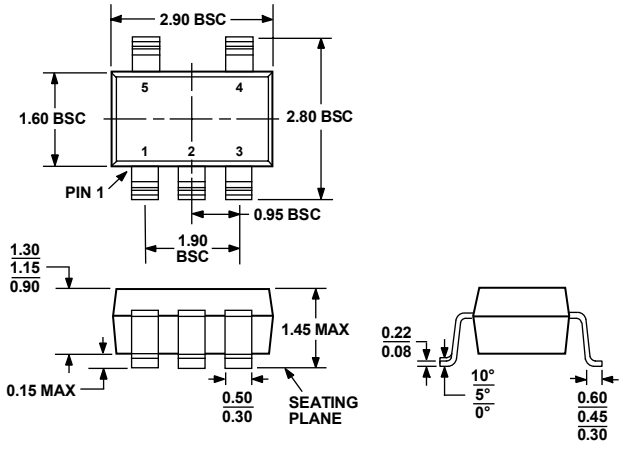

Figure 33. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters

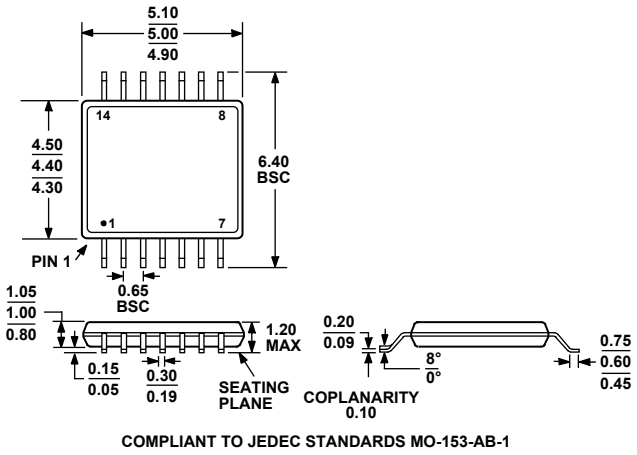

Figure 34. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

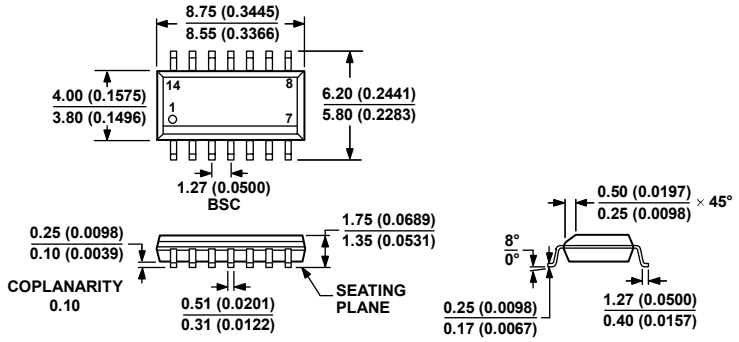

Figure 35. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8614ART-R2	−20°C to +85°C	5-Lead SOT-23	RJ-5	A6A
AD8614ART-REEL	−20°C to +85°C	5-Lead SOT-23	RJ-5	A6A
AD8614ART-REEL7	−20°C to +85°C	5-Lead SOT-23	RJ-5	A6A
AD8614ARTZ-REEL[1]	−20°C to +85°C	5-Lead SOT-23	RJ-5	A0Z
AD8614ARTZ-REEL7[1]	−20°C to +85°C	5-Lead SOT-23	RJ-5	A0Z
AD8644AR	−20°C to +85°C	14-Lead SOIC_N	R-14	
AD8644AR-REEL	−20°C to +85°C	14-Lead SOIC_N	R-14	
AD8644AR-REEL7	−20°C to +85°C	14-Lead SOIC_N	R-14	
AD8644ARZ[1]	−20°C to +85°C	14-Lead SOIC_N	R-14	
AD8644ARZ-REEL[1]	−20°C to +85°C	14-Lead SOIC_N	R-14	
AD8644ARZ-REEL7[1]	−20°C to +85°C	14-Lead SOIC_N	R-14	
AD8644ARU	−20°C to +85°C	14-Lead TSSOP	RU-14	
AD8644ARU-REEL	−20°C to +85°C	14-Lead TSSOP	RU-14	
AD8644ARUZ[1]	−20°C to +85°C	14-Lead TSSOP	RU-14	
AD8644ARUZ-REEL[1]	−20°C to +85°C	14-Lead TSSOP	RU-14	

[1] Z = RoHS Compliant Part.

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