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REVISION HISTORY

8/15—Revision 0: Initial Version

SPECIFICATIONS

V_{SY} = ±15 V, V_{CM} = 0 V, V_O = 0 V, T_A = 25°C, unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			10	120	µV
		−55°C ≤ T_A ≤ +125°C			300	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−55°C ≤ T_A ≤ +125°C		0.8	2.5	µV/°C
Input Bias Current	I_B			25	200	nA
		−55°C ≤ T_A ≤ +125°C			350	nA
Input Offset Current	I_{OS}			50	200	nA
		−55°C ≤ T_A ≤ +125°C			350	nA
Input Voltage Range	IVR		−12.5		+12.5	V
Common-Mode Rejection Ratio	CMRR	−12.5 V ≤ V_{CM} ≤ +12.5 V	120	135		dB
		−55°C ≤ T_A ≤ +125°C	115			dB
Large Signal Voltage Gain	A_{VO}	R_L ≥ 600 Ω, V_O = −11 V to +11 V	110	116		dB
		−55°C ≤ T_A ≤ +125°C	106			dB
Input Capacitance						
Differential Capacitance	C_{DIFF}			12.1		pF
Common-Mode Capacitance	C_{CM}			5.1		pF
OUTPUT CHARACTERISTICS						
Output Voltage						
High	V_{OH}	R_L = 600 Ω	13.1	13.4		V
		−55°C ≤ T_A ≤ +125°C	12.8			V
		R_L = 2 kΩ	13.5	13.7		V
		−55°C ≤ T_A ≤ +125°C	13.2			V
Low	V_{OL}	R_L = 600 Ω		−13.2	−12.9	V
		−55°C ≤ T_A ≤ +125°C			−12.8	V
		R_L = 2 kΩ		−13.5	−13.4	V
		−55°C ≤ T_A ≤ +125°C			−13.3	V
Output Short-Circuit Current	I_{SC}			±52		mA
Closed-Loop Output Impedance	Z_{OUT}	At 1 MHz, A_{VO} = 1		5		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±18 V to ±4.5 V	120	140		dB
		−55°C ≤ T_A ≤ +125°C	118			dB
Supply Current per Amplifier	I_{SY}			5.0	5.7	mA
		−55°C ≤ T_A ≤ +125°C			6.75	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	A_{VO} = −1, R_L = 2 kΩ		16		V/µs
		A_{VO} = 1, R_L = 2 kΩ		15		V/µs
Settling Time	t_S	To 0.01%, step = 10 V		2		µs
Gain Bandwidth Product	GBP			10		MHz
Phase Margin	Φ_M			65		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	0.1 Hz to 10 Hz		76		nV p-p
Voltage Noise Density	e_n	f = 1 kHz		1.07	1.15	nV/√Hz
		f = 10 Hz			1.5	nV/√Hz
Correlated Current Noise		f = 1 kHz		1.9		pA/√Hz
		f = 10 Hz		4.3		pA/√Hz
Uncorrelated Current Noise		f = 1 kHz		2.3		pA/√Hz
		f = 10 Hz		5.3		pA/√Hz
Total Harmonic Distortion + Noise	THD + N	G = 1, R_L ≥ 1 kΩ, f = 1 kHz, V_{RMS} = 3 V		−120		dB
Channel Separation	CS	f = 10 kHz		−120		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	$-V \le V_{IN} \le +V$
Differential Input Voltage[1]	±1 V
Output Short-Circuit to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering 60 sec)	300°C
Junction Temperature	150°C

[1] If the differential input voltage exceeds 1 V, limit the current to 5 mA.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified with the device soldered on a circuit board with its exposed paddle soldered to a pad (if applicable) on a 4-layer JEDEC standard PCB with zero air flow.

Table 3.

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC (R-8)	120	36	°C/W

POWER SEQUENCING

Apply the op amp supplies simultaneously. The op amp supplies must be stable before any input signals are applied. In any case, the input current must be limited to 5 mA.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

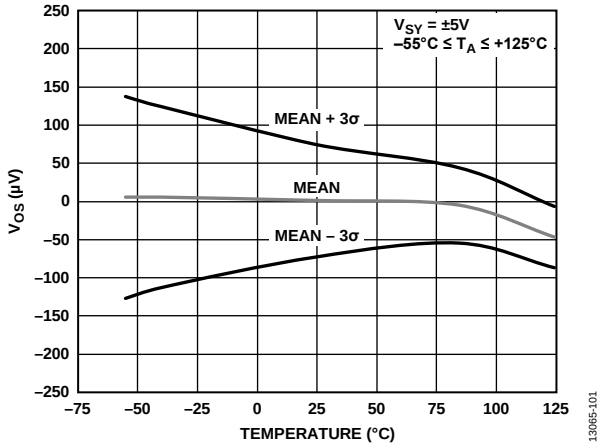

Figure 2. Input Offset Voltage (V_{OS}) Distribution, V_{SY} = ±5 V

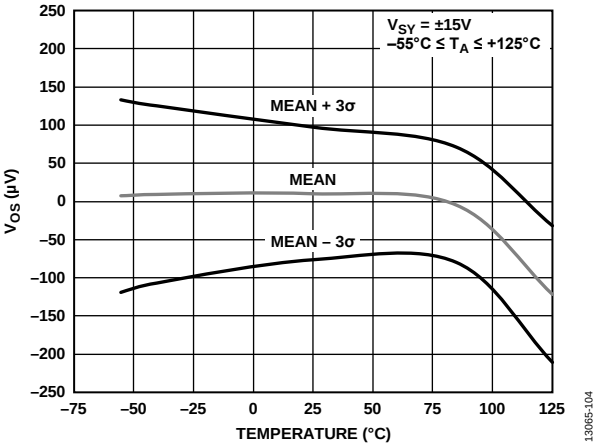

Figure 5. Input Offset Voltage (V_{OS}) Distribution, V_{SY} = ±15 V

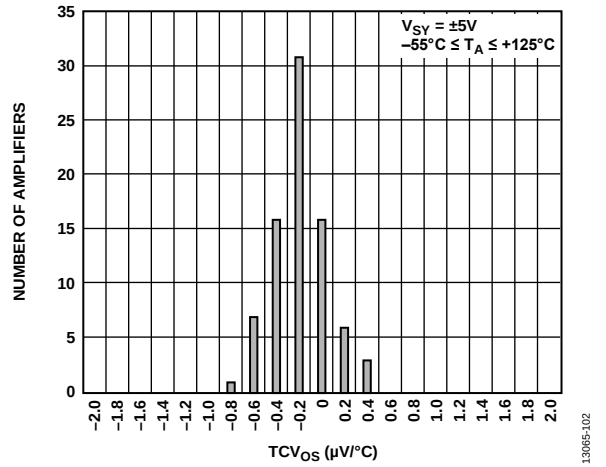

Figure 3. Input Offset Voltage Drift (TCV_{OS}) Distribution, V_{SY} = ±5 V

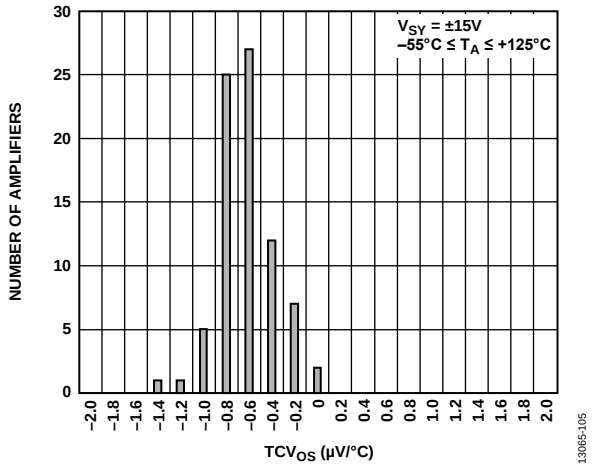

Figure 6. Input Offset Voltage Drift (TCV_{OS}) Distribution, V_{SY} = ±15 V

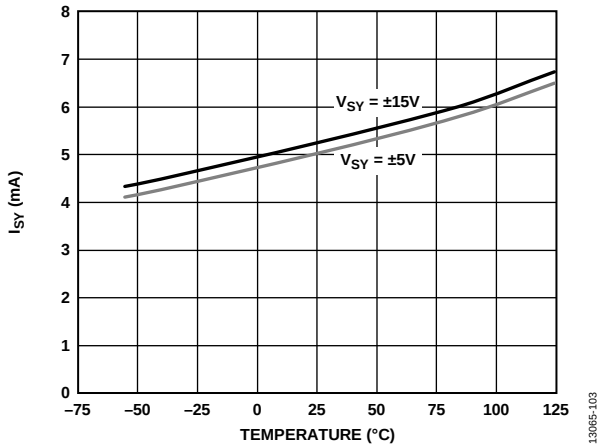

Figure 4. Supply Current (I_{SY}) vs. Temperature

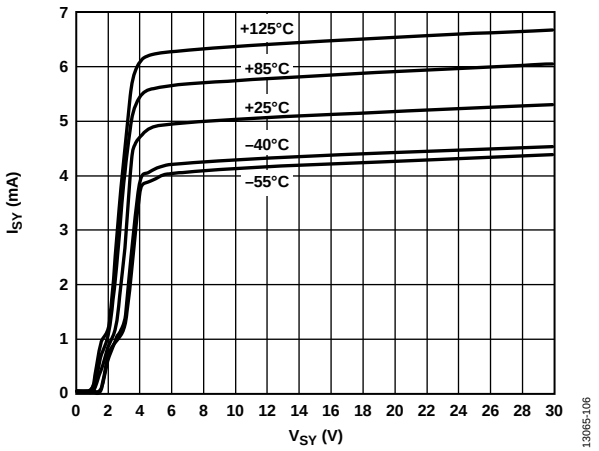

Figure 7. Supply Current (I_{SY}) vs. Supply Voltage (V_{SY})

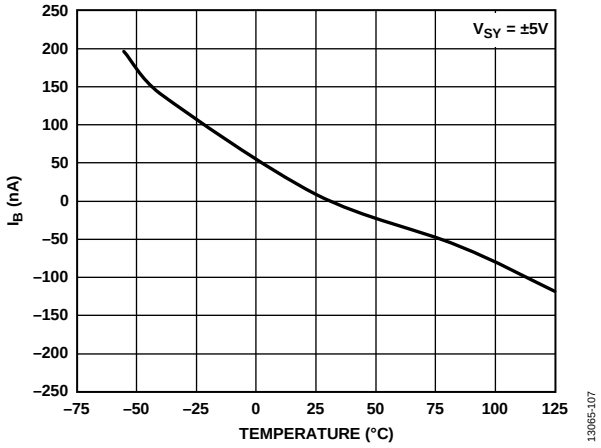

Figure 8. Input Bias Current (I_B) vs. Temperature, V_{SY} = ±5 V

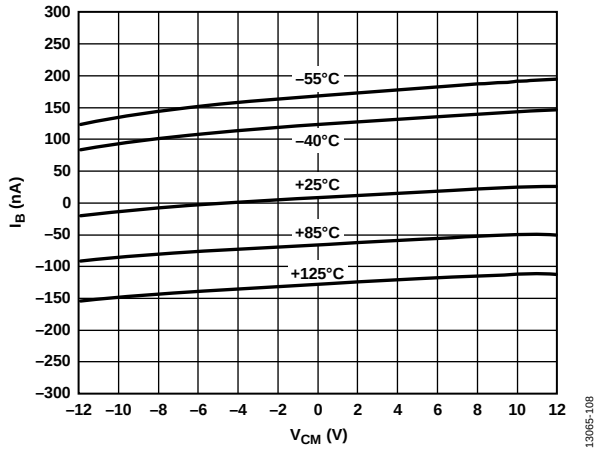

Figure 9. Input Bias Current (I_B) vs. Common-Mode Voltage (V_{CM})

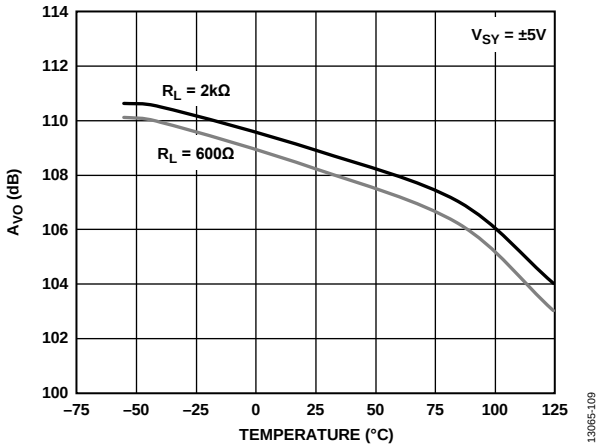

Figure 10. Large Signal Voltage Gain (A_{VO}) vs. Temperature, V_{SY} = ±5 V

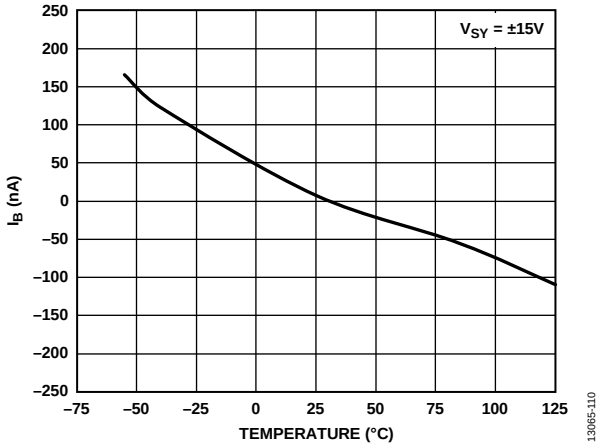

Figure 11. Input Bias Current (I_B) vs. Temperature, V_{SY} = ±15 V

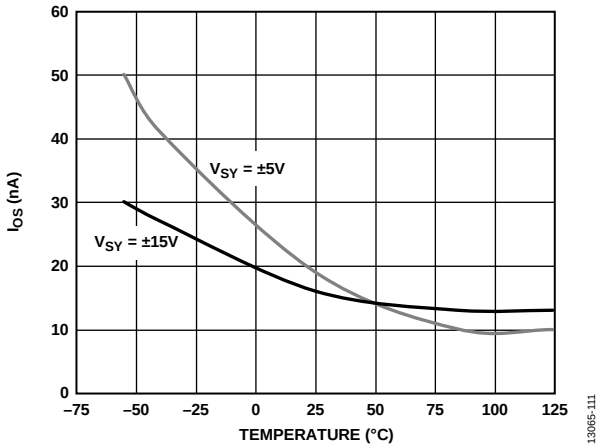

Figure 12. Input Offset Current (I_{OS}) vs. Temperature

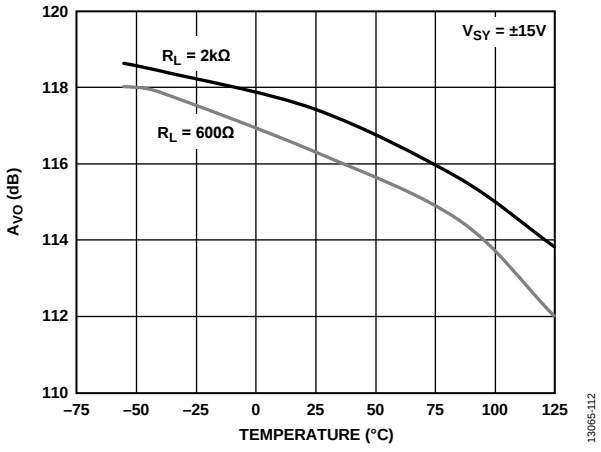

Figure 13. Large Signal Voltage Gain (A_{VO}) vs. Temperature

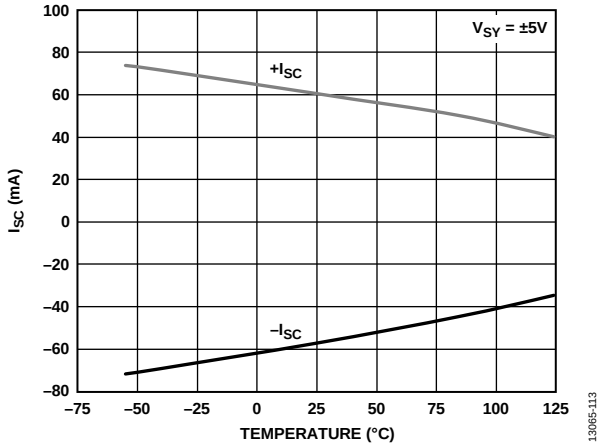

Figure 14. Output Short-Circuit Current (I_{SC}) vs. Temperature, V_{SY} = ±5 V

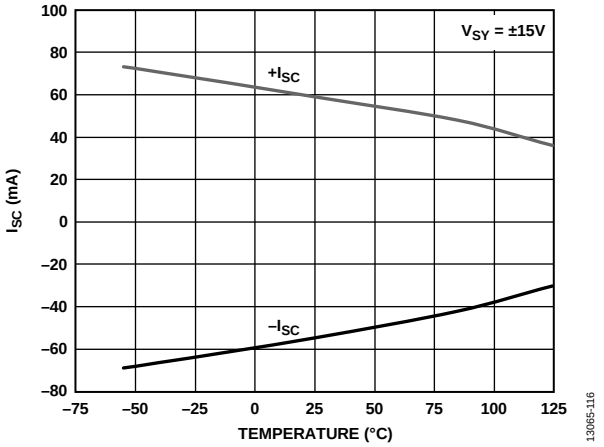

Figure 17. Output Short-Circuit Current (I_{SC}) vs. Temperature, V_{SY} = ±15 V

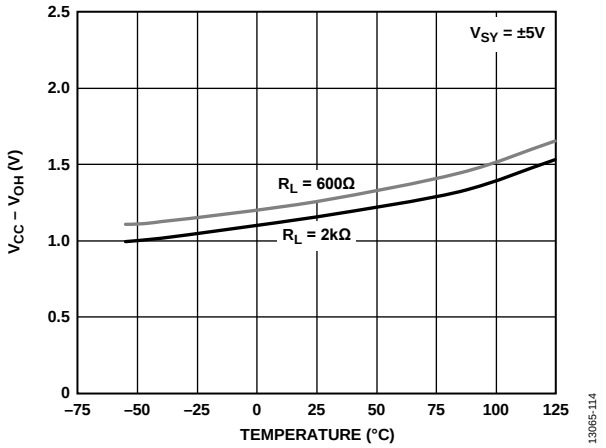

Figure 15. Output Saturation Voltage ($V_{CC} – V_{OH}$) vs. Temperature, V_{SY} = ±5 V

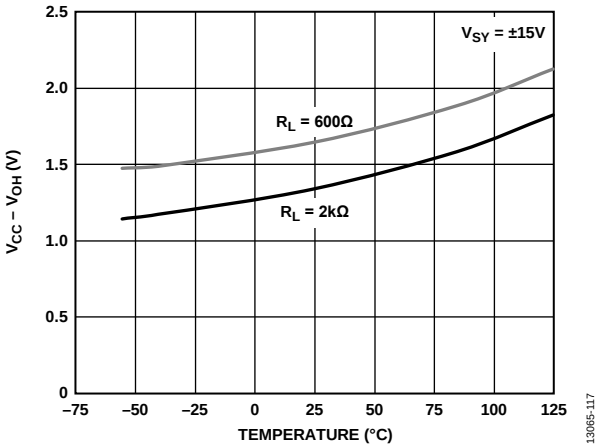

Figure 18. Output Saturation Voltage ($V_{CC} – V_{OH}$) vs. Temperature, V_{SY} = ±15 V

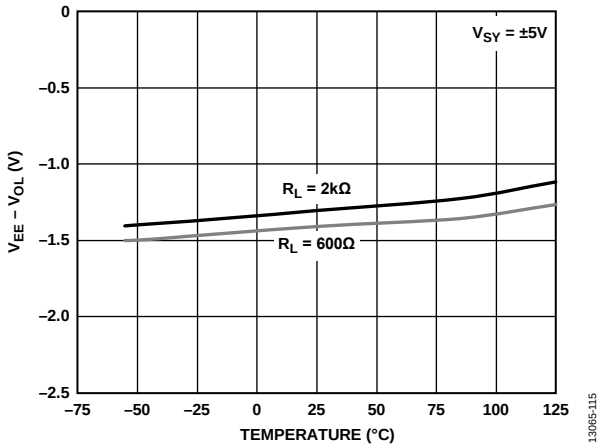

Figure 16. Output Saturation Voltage ($V_{EE} – V_{OL}$) vs. Temperature, V_{SY} = ±5 V

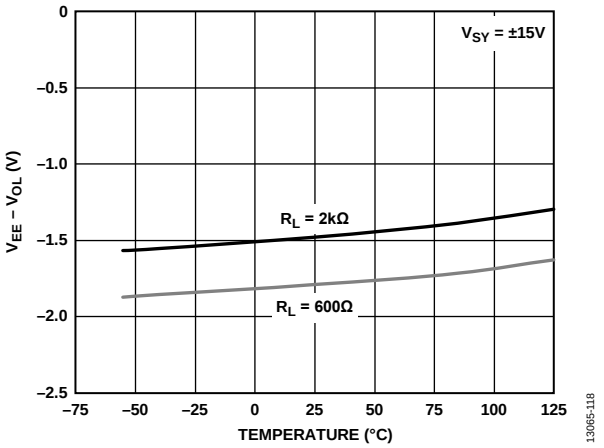

Figure 19. Output Saturation Voltage ($V_{EE} – V_{OL}$) vs. Temperature, V_{SY} = ±15 V

OUTLINE DIMENSIONS

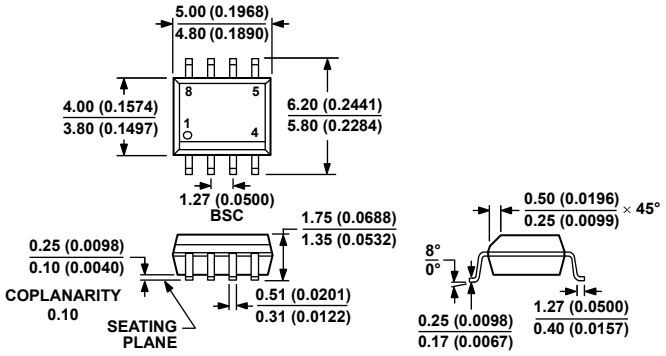

Figure 20. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8599TRZ-EP	−55°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD8599TRZ-EP-R7	−55°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8

[1] Z = RoHS Complaint Part.