AD678–SPECIFICATIONS

AC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = –12 V ± 5%, V_{DD} = +5 V ± 10%, f_{SAMPLE} = 200 kSPS, f_{IN} = 10.06 kHz unless otherwise noted)[1]

Parameter	AD678J/A/S Min	AD678J/A/S Typ	AD678J/A/S Max	AD678K/B/T Min	AD678K/B/T Typ	AD678K/B/T Max	Units
SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO[2]							
–0.5 dB Input (Referred to –0 dB Input)	70	71		71	73		dB
–20 dB Input (Referred to –20 dB Input)		51			53		dB
–60 dB Input (Referred to –60 dB Input)		11			13		dB
TOTAL HARMONIC DISTORTION (THD)[3]		–88	–80		–88	–80	dB
		0.004	0.010		0.004	0.010	%
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		–87	–80		–87	–80	dB
FULL POWER BANDWIDTH		1			1		MHz
FULL LINEAR BANDWIDTH	500			500			kHz
INTERMODULATION DISTORTION (IMD)[4]							
2nd Order Products		–85	–80		–85	–80	dB
3rd Order Products		–90	–80		–90	–80	dB

NOTES
[1]f_{IN} amplitude = –0.5 dB (9.44 V p-p) bipolar mode full scale unless otherwise indicated. All measurements referred to a –0 dB (9.997 V p-p) input signal unless otherwise indicated.
[2]See Figures 13 and 14 for higher frequencies and other input amplitudes.
[3]See Figure 12.
[4]f_A = 9.08 kHz, f_B = 9.58 kHz, with f_{SAMPLE} = 200 kSPS. See Definition of Specifications section and Figure 16.
Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (All device types T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = –12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter		Test Conditions	Min	Max	Units
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		2.0	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	0.8	V
I_{IH}	High Level Input Current	V_{IN} = V_{DD}	–10	+10	µA
I_{IL}	Low Level Input Current	V_{IN} = 0 V	–10	+10	µA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	4.0		V
		I_{OH} = 0.5 mA	2.4		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		0.4	V
I_{OZ}	High Z Leakage Current	V_{IN} = 0 or V_{DD}	–10	+10	µA
C_{OZ}	High Z Output Capacitance			10	pF

Specifications subject to change without notice.

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = –12 V ± 5%, V_{DD} = +5 V ± 10% unless otherwise noted)

Parameter	AD678J/A/S Min	AD678J/A/S Typ	AD678J/A/S Max	AD678K/B/T Min	AD678K/B/T Typ	AD678K/B/T Max	Units
TEMPERATURE RANGE							
J, K Grades	0		+70	0		+70	°C
A, B Grades	–40		+85	–40		+85	°C
S, T Grades	–55		+125	–55		+125	°C
ACCURACY							
Resolution	12			12			Bits
Integral Nonlinearity (INL)		±1			±0.7	±1	LSB
Differential Nonlinearity (DNL)	12			12			Bits
Unipolar Zero Error (@ +25°C)[1]		±4			±2	±3	LSB
Bipolar Zero Error (@ +25°C)[1]		±4			±3	±5	LSB
Gain Error (@ +25°C)[1, 2]		±4			±3	±6	LSB
Temperature Drift							
Unipolar/Bipolar Zero							
J, K Grades		±2			±2	±4	LSB
A, B Grades		±4			±3	±4	LSB
S, T Grades		±5			±4	±5	LSB
Gain[3]							
J, K Grades		±4			±4	±6	LSB
A, B Grades		±7			±5	±9	LSB
S, T Grades		±10			±8	±10	LSB
Gain[4]							
J, K Grades		±2			±2	±4	LSB
A, B Grades		±4			±3	±4	LSB
S, T Grades		±6			±5	±6	LSB
ANALOG INPUT							
Input Ranges							
Unipolar Range	0		+10	0		+10	V
Bipolar Range	–5		+5	–5		+5	V
Input Resistance		10			10		MΩ
Input Capacitance		10			10		pF
Input Settling Time			1			1	µs
Aperture Delay		10			10		ns
Aperture Jitter		150			150		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage[5]	4.98		5.02	4.98		5.02	V
External Load							
Unipolar Mode			+1.5			+1.5	mA
Bipolar Mode			+0.5			+0.5	mA
POWER SUPPLIES							
Power Supply Rejection							
V_{CC} = +12 V ± 5%		±2				±2	LSB
V_{EE} = –12 V ± 5%		±2				±2	LSB
V_{DD} = +5 V ± 10%		±2				±2	LSB
Operating Current							
I_{CC}		18	20		18	20	mA
I_{EE}		25	34		25	34	mA
I_{DD}		8	12		8	12	mA
Power Consumption		560	745		560	745	mW

NOTES
[1]Adjustable to zero.
[2]Includes internal voltage reference error.
[3]Includes internal voltage reference drift.
[4]Excludes internal voltage reference drift.
[5]With maximum external load applied.

Specifications subject to change without notice.

TIMING SPECIFICATIONS (All grades, T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = –12 V ± 5%, V_{DD} = +5 V ± 10% unless otherwise noted)

Parameter	Symbol	Min	Max	Units
$\overline{SC}$ Delay	t_{SC}	50		ns
Conversion Time	t_C	3.0	4.4	µs
Conversion Rate[1]	t_{CR}		5	µs
Convert Pulsewidth	t_{CP}	97		ns
Aperture Delay	t_{AD}	5	20	ns
Status Delay	t_{SD}	0	400	ns
Access Time[2, 3]	t_{BA}	10	100	ns
		10	57[4]	ns
Float Delay[5]	t_{FD}	10	80	ns
Output Delay	t_{OD}		0	ns
Format Setup	t_{FS}	47		ns
$\overline{OE}$ Delay	t_{OE}	0		ns
Read Pulsewidth	t_{RP}	97		ns
Conversion Delay	t_{CD}	150		ns
$\overline{EOCEN}$ Delay	t_{EO}	0		ns

NOTES
[1]Includes acquisition time.
[2]Measured from the falling edge of $\overline{OE}/\overline{EOCEN}$ (0.8 V) to the time at which the data lines/EOC cross 2.0 V or 0.8 V. See Figure 3.
[3]C_{OUT} = 100 pF.
[4]C_{OUT} = 50 pF.
[5]Measured from the rising edge of $\overline{OE}/\overline{EOCEN}$ (2.0 V) to the time at which the output voltage changes by 0.5 V. See Figure 3; C_{OUT} = 10 pF.
Specifications subject to change without notice.

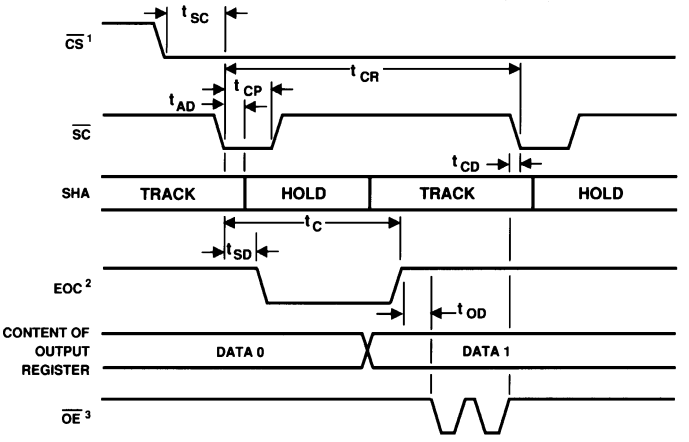


Figure 1. Conversion Timing

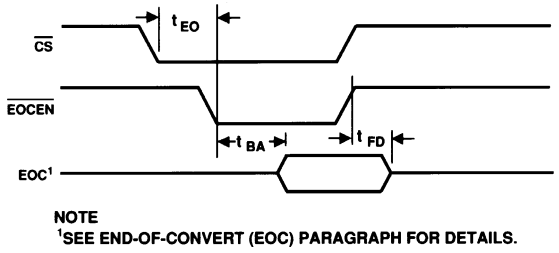


Figure 2. EOC Timing

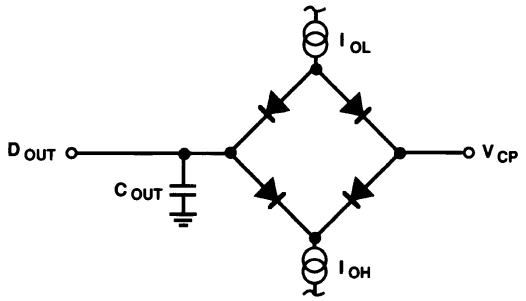
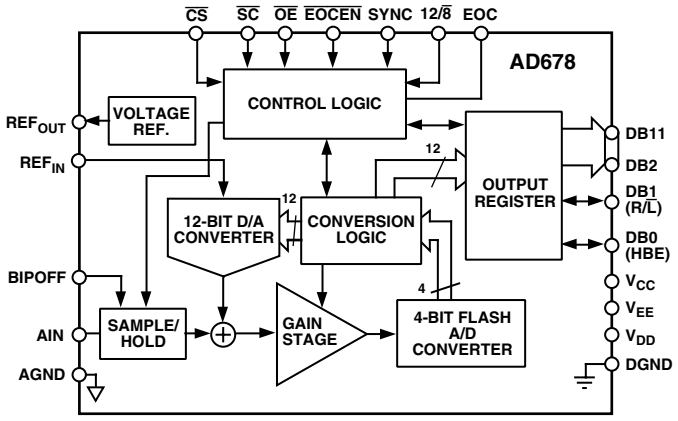


Figure 3. Load Circuit for Bus Timing Specifications

ABSOLUTE MAXIMUM RATINGS*

Specification	With Respect To	Min	Max	Units
V_{CC}	AGND	–0.3	+18	V
V_{EE}	AGND	–18	+0.3	V
V_{CC}	V_{EE}	–0.3	+26.4	V
V_{DD}	DGND	0	+7	V
AGND	DGND	–1	+1	V
AIN, REF_{IN}	AGND	V_{EE}	V_{CC}	V
Digital Inputs	DGND	–0.5	+7	V
Digital Outputs	DGND	–0.5	V_{DD} + 0.3	V
Max Junction Temperature			175	°C
Operating Temperature				
J and K Grades		0	+70	°C
A and B Grades		–40	+85	°C
S and T Grades		–55	+125	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec max)			+300	°C

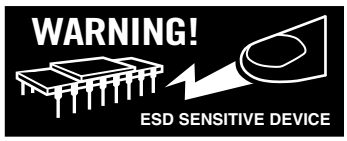
*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



Functional Block Diagram

ESD SENSITIVITY

The AD678 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD678 has been classified as a Category 1 device.



Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual.*

ORDERING GUIDE

Model[1]	Package	Temperature Range	Tested and Specified	Package Option[2]
AD678JN	28-Lead Plastic DIP	0°C to +70°C	AC	N-28
AD678KN	28-Lead Plastic DIP	0°C to +70°C	AC + DC	N-28
AD678JD	28-Lead Ceramic DIP	0°C to +70°C	AC	D-28
AD678KD	28-Lead Ceramic DIP	0°C to +70°C	AC + DC	D-28
AD678AD	28-Lead Ceramic DIP	–40°C to +85°C	AC	D-28
AD678BD	28-Lead Ceramic DIP	–40°C to +85°C	AC + DC	D-28
AD678AJ	44-Lead Ceramic JLCC	–40°C to +85°C	AC	J-44
AD678BJ	44-Lead Ceramic JLCC	–40°C to +85°C	AC + DC	J-44
AD678SD	28-Lead Ceramic DIP	–55°C to +125°C	AC	D-28
AD678TD	28-Lead Ceramic DIP	–55°C to +125°C	AC + DC	D-28

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to Analog Devices Military Products Databook or /883 data sheet.
[2]N = Plastic DIP; D = Ceramic DIP; J = J-Leaded Ceramic Chip Carrier.

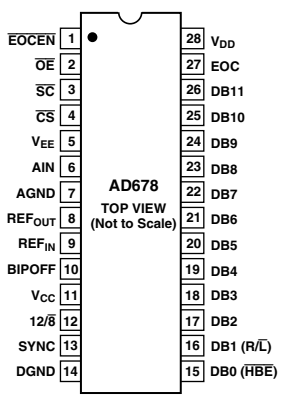
PIN DESCRIPTION

Symbol	28-Lead DIP Pin No.	44-Lead JLCC Pin No.	Type	Name and Function
AGND	7	11	P	Analog Ground. This is the ground return for AIN only.
AIN	6	10	AI	Analog Signal Input.
BIPOFF	10	15	AI	Bipolar Offset. Connect to AGND for +10 V input unipolar mode and straight binary output coding. Connect to REF_{OUT} through 50 Ω resistor for ±5 V input bipolar mode and twos complement binary output coding. See Figures 7 and 8.
$\overline{CS}$	4	6	DI	Chip Select. Active LOW.
DGND	14	23	P	Digital Ground
DB11–DB4	26–19	40, 39, 37, 36, 35, 34, 33, 31	DO	Data Bits 11 through 4. In 12-bit format (see 12/$\overline{8}$ pin), these pins provide the upper 8 bits of data. In 8-bit format, these pins provide all 12 bits in two bytes (see R/$\overline{L}$ pin). Active HIGH.
DB3, DB2	18, 17	30, 27	DO	Data Bits 3 and 2. In 12-bit format, these pins provide Data Bit 3 and Data Bit 2. Active HIGH. In 8-bit format they are undefined and should be tied to V_{DD}.
DB1 (R/$\overline{L}$)	16	26	DO	In 12-bit format, Data Bit 1. Active HIGH.
DB0 ($\overline{HBE}$)	15	25	DO	In 12-bit format, Data Bit 0. Active HIGH.
EOC	27	42	DO	End-of-Convert. EOC goes LOW when a conversion starts and goes HIGH when the conversion is finished. In asynchronous mode, EOC is an open drain output and requires an external 3 kΩ pull-up resistor. See $\overline{EOCEN}$ and SYNC pins for information on EOC gating.
$\overline{EOCEN}$	1	1	DI	End-Of-Convert Enable. Enables EOC pin. Active LOW.
$\overline{HBE}$ (DB0)	15	25	DI	In 8-bit format, High Byte Enable. If LOW, output contains high byte. If HIGH, output contains low byte.
$\overline{OE}$	2	3	DI	Output Enable. The falling edge of $\overline{OE}$ enables DB11–DB0 in 12-bit format and DB11–DB4 in 8-bit format. Gated with $\overline{CS}$. Active LOW.
REF_{IN}	9	14	AI	Reference Input. +5 V input gives 10 V full-scale range.
REF_{OUT}	8	12	AO	+5 V Reference Output. Tied to REF_{IN} through 50 Ω resistor for normal operation.
R/$\overline{L}$ (DB1)	16	26	DI	In 8-bit format, Right/Left justified. Sets alignment of 12-bit result within 16-bit field. Tied to V_{DD} for right-justified output and tied to DGND for left-justified output.
$\overline{SC}$	3	5	DI	Start Convert. Active LOW. See SYNC pin for gating.
SYNC	13	21	DI	SYNC Control. If tied to V_{DD} (synchronous mode), $\overline{SC}$, EOC and $\overline{EOCEN}$ are gated by $\overline{CS}$. If tied to DGND (asynchronous mode), $\overline{SC}$ and $\overline{EOCEN}$ are independent of $\overline{CS}$, and EOC is an open drain output. EOC requires an external 3 kΩ pull-up resistor in asynchronous mode.
V_{CC}	11	17	P	+12 V Analog Power.
V_{EE}	5	8	P	–12 V Analog Power.
V_{DD}	28	43	P	+5 V Digital Power.
12/$\overline{8}$	12	19	DI	Twelve/eight-bit format. If tied HIGH, sets output format to 12-bit parallel. If tied LOW, sets output format to 8-bit multiplexed.
No Connect		2, 4, 7, 9, 13, 16, 18, 20, 22, 24, 28, 29, 32, 38, 41, 44		These pins are unused and should be connected to DGND or V_{DD}.

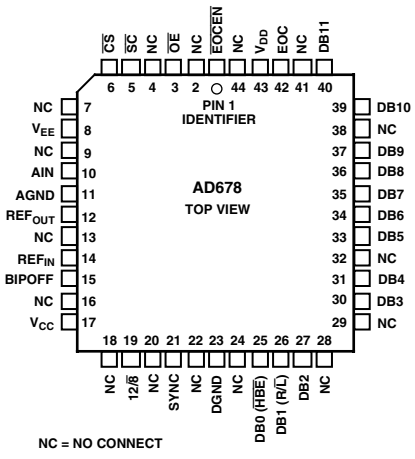
Type: AI = Analog Input; AO = Analog Output; DI = Digital Input (TTL and 5 V CMOS compatible); DO = Digital Output (TTL and 5 V CMOS compatible). All DO pins are three-state drivers; P = Power.

PIN CONFIGURATIONS

DIP PACKAGE



JLCC PACKAGE



NYQUIST FREQUENCY
An implication of the Nyquist sampling theorem, the "Nyquist Frequency" of a converter is that input frequency which is one-half the sampling frequency of the converter.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

TOTAL HARMONIC DISTORTION (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of a full-scale input signal and is expressed as a percentage or in decibels. For input signals or harmonics that are above the Nyquist frequency, the aliased component is used.

PEAK SPURIOUS OR PEAK HARMONIC COMPONENT
The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in decibels relative to the rms value of a full-scale input signal.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3.... Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa – fb) and the third order terms are (2 fa + fb), (2 fa – fb), (fa + 2 fb) and (fa – 2 fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input sides to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude and the peak value of their sum is –0.5 dB from full scale (9.44 V p-p). The IMD products are normalized to a 0 dB input signal.

BANDWIDTH
The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

The full-linear bandwidth is the input frequency at which the slew rate limit of the sample-hold-amplifier (SHA) is reached. At this point, the amplitude of the reconstructed fundamental has degraded by less than 0.1 dB. Beyond this frequency, distortion of the sampled input signal increases significantly.

The AD678 has been designed to optimize input bandwidth, allowing the AD678 to undersample input signals with frequencies significantly above the converter's Nyquist frequency.

APERTURE DELAY
Aperture delay is a measure of the SHA's performance and is measured from the falling edge of Start Convert ($\overline{SC}$) to when the input signal is held for conversion. In synchronous mode, Chip Select ($\overline{CS}$) should be LOW before $\overline{SC}$ to minimize aperture delay.

APERTURE JITTER
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

INPUT SETTLING TIME
Settling time is a function of the SHA's ability to track fast slewing signals. This is specified as the maximum time required in track mode after a full-scale step input to guarantee rated conversion accuracy.

DIFFERENTIAL NONLINEARITY (DNL)
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes (NMC) are guaranteed.

UNIPOLAR ZERO ERROR
In unipolar mode, the first transition should occur at a level 1/2 LSB above analog ground. Unipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

BIPOLAR ZERO ERROR
In the bipolar mode, the major carry transition (1111 1111 1111 to 0000 0000 0000) should occur at an analog value 1/2 LSB below analog ground. Bipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

GAIN ERROR
The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale (9.9963 volts for a 0–10 V range, 4.9963 volts for a ±5 V range). The gain error is the deviation of the actual difference between the first and last code transition from the ideal difference between the first and last code transition. This error can be adjusted as shown in the Input Connections and Calibration section.

INTEGRAL NONLINEARITY (INL)
The ideal transfer function for a linear ADC is a straight line drawn between "zero" and "full scale." The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition. Integral nonlinearity is the worst-case deviation of a code from the straight line. The deviation of each code is measured from the middle of that code.

POWER SUPPLY REJECTION
Variations in power supply will affect the full-scale transition, but not the converter's linearity. Power Supply Rejection is the maximum change in the full-scale transition point due to a change in power-supply voltage from the nominal value.

TEMPERATURE DRIFT
This is the maximum change in the parameter from the initial value (@ +25°C) to the value at T_{MIN} or T_{MAX}.

AD678–Dynamic Performance

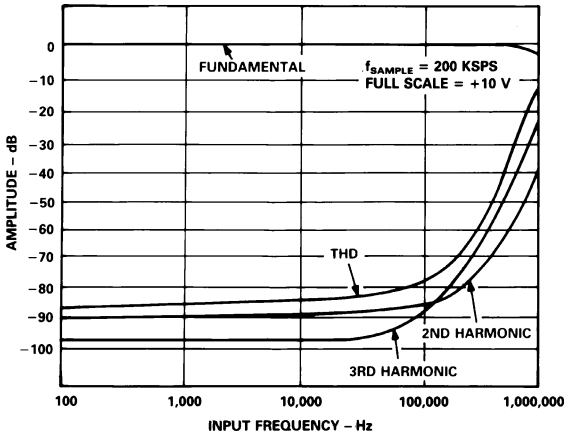


Figure 4. Harmonic Distortion vs. Input Frequency

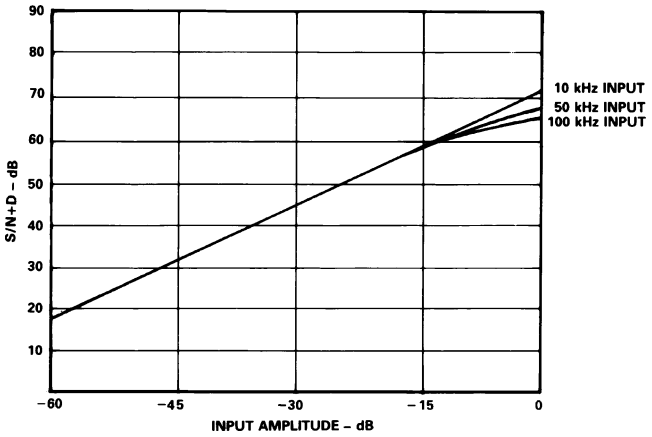


Figure 5. S/N+D vs. Input Amplitude (f_{SAMPLE} 200 kSPS)

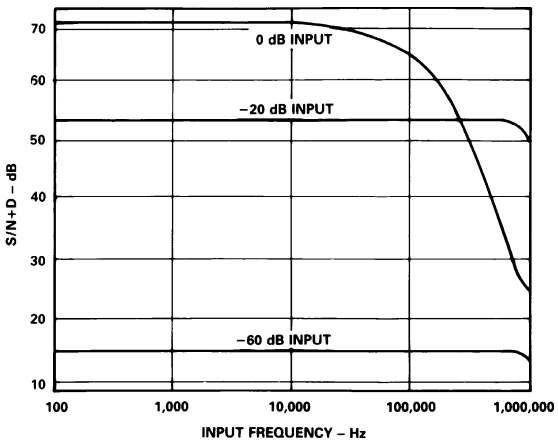


Figure 6. S/N+D vs. Input Frequency and Amplitude

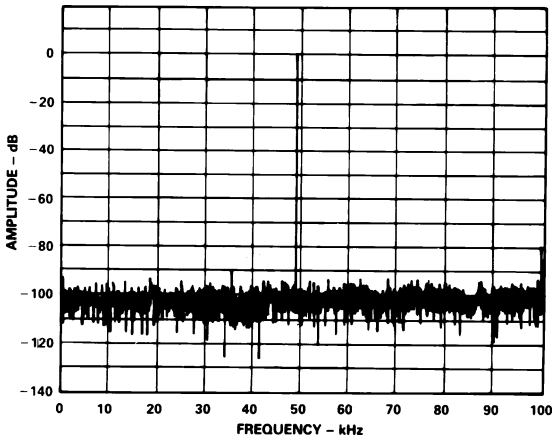


Figure 7. Nonaveraged 2048 Point FFT at 200 kSPS, f_{IN} = 49.902 kHz

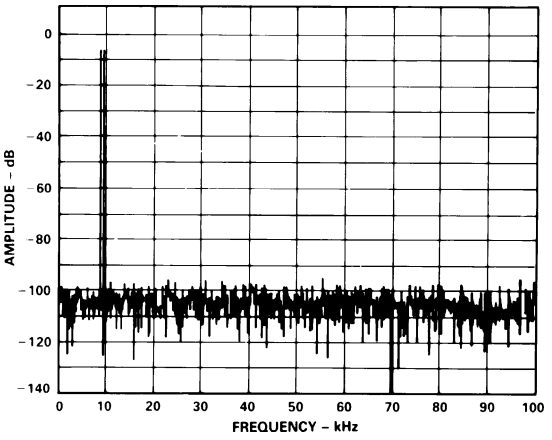


Figure 8. IMD Plot for f_{IN} = 9.08 kHz (fa), 9.58 kHz (fb)

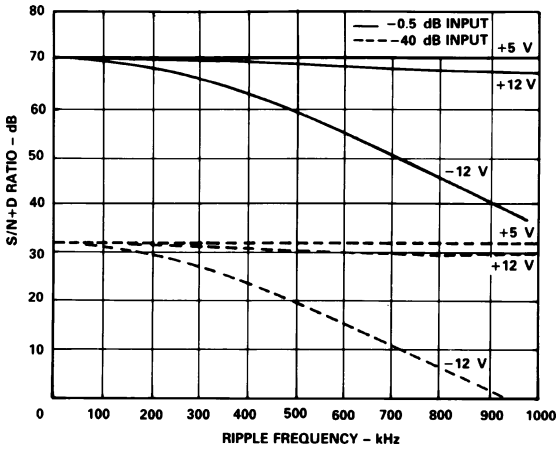


Figure 9. Power Supply Rejection (f_{IN} = 10 kHz, f_{SAMPLE} = 200 kSPS, V_{RIPPLE} = 0.1 V p-p)

CONVERSION CONTROL

In synchronous mode (SYNC = HIGH), both Chip Select ($\overline{CS}$) and Start Convert ($\overline{SC}$) must be brought LOW to start a conversion. $\overline{CS}$ should be LOW t_{SC} before $\overline{SC}$ is brought LOW. In asynchronous mode (SYNC = LOW), a conversion is started by bringing $\overline{SC}$ low, regardless of the state of $\overline{CS}$.

Before a conversion is started, End-of-Convert (EOC) is HIGH, and the sample-hold is in track mode. After a conversion is started, the sample-hold goes into hold mode and EOC goes LOW, signifying that a conversion is in progress. During the conversion, the sample-hold will go back into track mode and start acquiring the next sample. EOC goes HIGH when the conversion is finished.

In track mode, the sample-hold will settle to ±0.01% (12 bits) in 1 µs maximum. The acquisition time does not affect the throughput rate as the AD678 goes back into track mode more than 1 µs before the next conversion. In multichannel systems, the input channel can be switched as soon as EOC goes LOW if the maximum throughput rate is needed.

12-Bit Mode Coding Format (1 LSB = 2.44 mV)

Unipolar Coding (Straight Binary)		Bipolar Coding (Twos Complement)	
V_{IN}*	Output Code	V_{IN}*	Output Code
0 V	000 . . . 0	–5.000 V	100 . . . 0
5.000 V	100 . . . 0	–0.002 V	111 . . . 1
9.9976 V	111 . . . 1	0.000 V	000 . . . 0
		+2.500 V	010 . . . 0
		+4.9976 V	011 . . . 1

*Code center.

OUTPUT ENABLE TRUTH TABLES

12-BIT MODE (12/$\overline{8}$ = HIGH)

INPUTS ($\overline{CS}$ U $\overline{OE}$)	OUTPUT DB11–DB0
1	High Z
0	Enable 12-Bit Output

8-BIT MODE (12/$\overline{8}$ = LOW)

	INPUTS R/$\overline{L}$	$\overline{HBE}$	($\overline{CS}$ U $\overline{OE}$)	OUTPUTS DB11 . . . DB4							
	X	X	1	High Z							
	1	0	0	0	0	0	0	a	b	c	d
Unipolar	1	1	0	e	f	g	h	i	j	k	l
Mode	0	0	0	a	b	c	d	e	f	g	h
	0	1	0	i	j	k	l	0	0	0	0
	1	0	0	a	a	a	a	a	b	c	d
Bipolar	1	1	0	e	f	g	h	i	j	k	l
Mode	0	0	0	a	b	c	d	e	f	g	h
	0	1	0	i	j	k	l	0	0	0	0

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
U = Logical OR.
a = MSB.
1 = LSB.

END-OF-CONVERT

In asynchronous mode, End-of-Convert (EOC) is an open drain output (requiring a minimum 3 kΩ pull-up resistor) enabled by End-of-Convert ENable ($\overline{EOCEN}$). In synchronous mode, EOC is a three-state output which is enabled by $\overline{EOCEN}$ and $\overline{CS}$. See the Conversion Status Truth Table for details. Access (t_{BA}) and float (t_{FD}) timing specifications do not apply in asynchronous mode where they are a function of the time constant formed by the 10 pF output capacitance and the pull-up resistor.

START CONVERSION TRUTH TABLE

	INPUTS SYNC	$\overline{CS}$	$\overline{SC}$	STATUS
	1	1	X	No Conversion
Synchronous	1	0		Start Conversion
Mode	1		0	Start Conversion (Not Recommended)
	1	0	0	Continuous Conversion (Not Recommended)
	0	X	1	No Conversion
Asynchronous	0	X		Start Conversion
Mode	0	X	0	Continuous Conversion (Not Recommended)

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
= HIGH to LOW transition. Must stay low for t = t_{CP}.

CONVERSION STATUS TRUTH TABLE

	INPUTS SYNC	$\overline{CS}$	$\overline{EOCEN}$	OUTPUT EOC	STATUS
	1	0	0	0	Converting
	1	0	0	1	Not Converting
Synchronous	1	1	X	High Z	Either
Mode	1	X	1	High Z	Either
	0	X	0	0	Converting
Asynchronous	0	X	0	High Z	Not Converting
Mode*	0	X	1	High Z	Either

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
*EOC requires a pull-up resistor in asynchronous mode.

OUTPUT ENABLE OPERATION

The data bits (DB11–DB0) are three-state outputs enabled by Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$). $\overline{CS}$ should be LOW t_{OE} before $\overline{OE}$ is brought LOW. Bits DB1 (R/$\overline{L}$) and DB0 ($\overline{HBE}$) are bidirectional. In 12-bit mode they are data output bits. In 8-bit mode they are inputs which define the format of the output register.

In unipolar mode (BIPOFF tied to AGND), the output coding is straight binary. In bipolar mode (BIPOFF tied to REF_{OUT}), output coding is twos complement binary.

When EOC goes HIGH, the conversion is completed and the output data may be read. Bringing $\overline{OE}$ LOW t_{OE} after $\overline{CS}$ is brought LOW makes the output register contents available on the data bits. A period of time t_{CD} is required after $\overline{OE}$ is brought HIGH before the next $\overline{SC}$ instruction may be issued.

Figure 10 illustrates the 8-bit read mode (12/$\overline{8}$ = LOW), where only DB11–DB4 are used as output lines onto an 8-bit bus. The output is read in two steps, with the high byte read first, followed by the low byte. High Byte Enable ($\overline{HBE}$) controls the output sequence. The 12-bit result can be right or left justified depending on the state of R/$\overline{L}$.

In 12-bit read mode (12/$\overline{8}$ = HIGH), a single READ operation accesses all 12 output bits on DB11-DB0 for interface to a 16-bit bus. Figure 11 provides the output timing relationships. Note that t_{CR} must be observed, in that $\overline{SC}$ pulses should not be issued at intervals closer than 5 µs. If $\overline{SC}$ is asserted sooner than 5 µs, conversion accuracy may deteriorate. For this reason, $\overline{SC}$ should not be held LOW in an attempt to operate in a continuously converting mode.

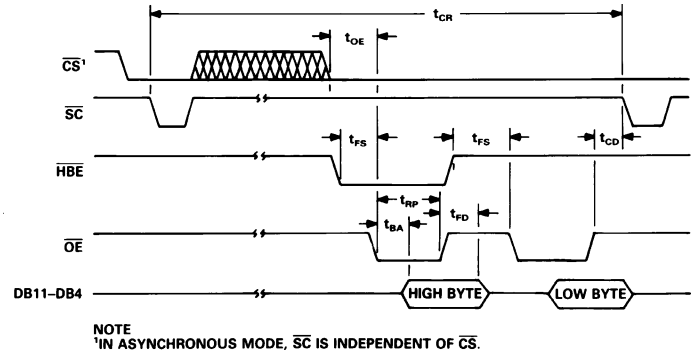


Figure 10. Output Timing, 8-Bit Read Mode

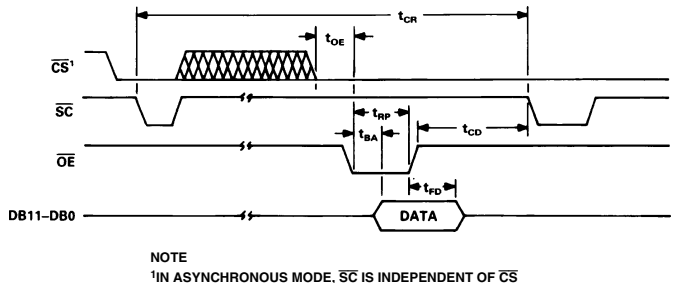


Figure 11. Output Timing, 12-Bit Read Mode

POWER-UP

The AD678 typically requires 10 µs after power-up to reset internal logic.

APPLICATION INFORMATION

INPUT CONNECTIONS AND CALIBRATION

The high (10 MΩ) input impedance of the AD678 eases the task of interfacing to high source impedances or multiplexer channel-to-channel mismatches of up to 1000 Ω. The 10 V p-p full-scale input range accepts the majority of signal voltages without the need for voltage divider networks which could deteriorate the accuracy of the ADC.

The AD678 is factory trimmed to minimize linearity, offset and gain errors. In unipolar mode, the only external component that is required is a 50 Ω ± 1% resistor. Two resistors are required in bipolar mode. If offset and gain are not critical (as in some ac applications), even these components can be eliminated.

In some applications, offset and gain errors need to be trimmed out completely. The following sections describe the correct procedure for these various situations.

UNIPOLAR RANGE INPUTS

Offset and gain errors can be trimmed out by using the configuration shown in Figure 12. This circuit allows approximately ±25 mV of offset trim range (±10 LSB) and ±0.5% of gain trim (±20 LSB).

The first transition (from 0000 0000 0000 to 0000 0000 0001) should nominally occur for an input level of +1/2 LSB (1.22 mV above ground for a 10 V range). To trim unipolar zero to this nominal value, apply a 1.22 mV signal to AIN and adjust R1 until the first transition is located.

The gain trim is done by adjusting R2. If the nominal value is required, apply a signal 1 1/2 LSB below full scale (9.9963 V for a 10 V range) and adjust R2 until the last transition is located (1111 1111 1110 to 1111 1111 1111).

If offset adjustment is not required, BIPOFF should be connected directly to AGND. If gain adjustment is not required, R2 should be replaced with a fixed 50 Ω ± 1% metal film resistor. If REF_{OUT} is connected directly to REF_{IN}, the additional gain error will be approximately 1%.

BIPOLAR RANGE INPUTS

The connections for the bipolar mode are shown in Figure 13. In this mode, data output coding will be in twos complement binary. This circuit will allow approximately ±25 mV of offset trim range (±10 LSB) and ±0.5% of gain trim range (20 LSB).

Either or both of the trim pots can be replaced with 50 Ω ± 1% fixed resistors if the AD678 accuracy limits are sufficient for the application. If the pins are shorted together, the additional offset and gain errors will be approximately 1%.

To trim bipolar zero to its nominal value, apply a signal 1/2 LSB below midrange (–1.22 mV for a ±5 V range) and adjust R1 until the major carry transition is located (1111 1111 1111 to 0000 0000 0000). To trim the gain, apply a signal 1 1/2 LSB below full scale (+4.9963 V for a ±5 V range) and adjust R2 to give the last positive transition (0111 1111 1110 to 0111 1111 1111). These trims are interactive so several iterations may be necessary for convergence.

A single-pass calibration can be done by substituting a bipolar offset trim (error at minus full scale) for the bipolar zero trim (error at midscale), using the same circuit. First, apply a signal 1/2 LSB above minus full scale (–4.9988 V for a ±5 V range) and adjust R1 until the minus full-scale transition is located (1000 0000 0000 to 1000 0000 0001). Then perform the gain error trim as outlined above.

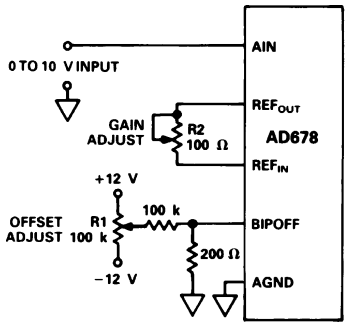


Figure 12. Unipolar Input Connections with Gain and Offset Trims

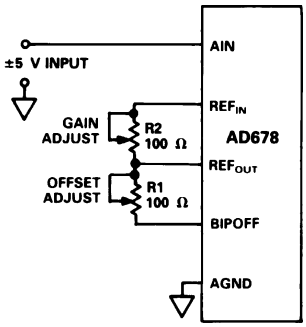


Figure 13. Bipolar Input Connections with Gain and Offset Trims

BOARD LAYOUT

Designing with high-resolution data converters requires careful attention to layout. Trace impedance is a significant issue. At the 12-bit level, a 5 mA current through a 0.5 Ω trace will develop a voltage drop of 2.5 mV, which is 1 LSB for a 10 V full-scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high- accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter out ac noise.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

The AD678 incorporates several features to help the user's layout. Analog pins (V_{EE}) AIN, AGND, REF_{OUT}, REF_{IN}, BIPOFF, V_{CC}) are adjacent to help isolate analog from digital signals. In addition, the 10 MΩ input impedance of AIN minimizes input trace impedance errors. Finally, ground currents have been minimized by careful circuit design. Current through AGND is 200 µA, with no code-dependent variation. The current through DGND is dominated by the return current for DB11–DB0 and EOC.

SUPPLY DECOUPLING

The AD678 power supplies should be well filtered, well regulated, and free from high-frequency noise. Switching power supplies are not recommended. These supplies generate spikes which can induce noise in the analog system.

Decoupling capacitors should be located as close as possible to all power supply pins. A 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic provides adequate decoupling. The power supply pins should be decoupled directly to AGND.

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD678, associated analog input circuitry and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD678 will isolate large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

GROUNDING

If a single AD678 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD678. If multiple AD678s are used or the AD678 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at each chip. This prevents large ground loops which inductively couple noise and allow digital currents to flow through the analog system.

INTERFACING THE AD678 TO MICROPROCESSORS

The I/O capabilities of the AD678 allow direct interfacing to general purpose and DSP microprocessor buses. The asynchronous conversion control feature allows complete flexibility and control with minimal external hardware.

The following examples illustrate typical AD678 interface configurations.

AD678 TO TMS320C25

In Figure 14 the AD678 is mapped into the TMS320C25 I/O space. AD678 conversions are initiated by issuing an OUT instruction to Port 8. EOC status and the conversion result are read in with an IN instruction to Port 8. A single wait state is inserted by generating the processor READY input from $\overline{IS}$, Port 8 and $\overline{MSC}$. This configuration supports processor clock speeds of 20 MHz and is capable of supporting processor clock speeds of 40 MHz if a NOP instruction follows each AD678 read instruction.

AD678 TO 80186

Figure 15 shows the AD678 interfaced to the 80186 microprocessor. This interface allows the 80186's built-in DMA controller to transfer the AD678 output into a RAM based FIFO buffer of any length, with no microprocessor intervention.

In this application the AD678 is configured in the asynchronous mode, which allows conversions to be initiated by an external trigger source independent of the microprocessor clock. After each conversion, the AD678 EOC signal generates a DMA request to Channel 1 (DRQ1). The subsequent DMA READ operation resets the interrupt latch. The system designer must assign a sufficient priority to the DMA channel to ensure that the DMA request will be serviced before the completion of the next conversion. This configuration can be used with 6 MHz and 8 MHz 80186 processors.

AD678 TO ANALOG DEVICES ADSP-2101

Figure 16 demonstrates the AD678 interfaced to an ADSP-2101. With a clock frequency of 12.5 MHz, and instruction execution in one 80 ns cycle, the digital signal processor supports the AD678 interface with one wait state.

The converter is configured to run asynchronously using a sampling clock. The EOC output of the AD678 gets asserted at the end of each conversion and causes an interrupt. Upon interrupt, the ADSP-2101 immediately asserts its FO pin LOW. In the following cycle, the processor starts a data memory read by providing an address on the DMA bus. The decoded address generates $\overline{OE}$ for the converter, and the high byte of the conversion result is read over the data bus. The read operation is extended with one wait state and thus started and completed within two processor cycles (160 ns). Next, the ADSP-2101 asserts its FO pin HIGH. This allows the processor to start reading the lower byte of data. This read operation executes in a similar manner to the first and is completed during the next 160 ns.

AD678 TO ANALOG DEVICES ADSP-2100A

Figure 17 demonstrates the AD678 interfaced to an ADSP-2100A. With a clock frequency of 12.5 MHz, and instruction execution in one 80 ns cycle, the digital signal processor will support the AD678 data memory interface with three hardware wait states.

The converter is configured to run asynchronously using a sampling clock. The EOC output of the AD678 gets asserted at the end of each conversion and causes an interrupt. Upon interrupt, the ADSP-2100A immediately executes a data memory write instruction which asserts $\overline{HBE}$. In the following cycle, the processor starts a data memory read (high byte read) by providing an address on the DMA bus. The decoded address generates $\overline{OE}$ for the converter. $\overline{OE}$, together with logic and latch, is used to force the ADSP-2100A into a one cycle wait state by generating DMACK. The read operation is thus started and completed within two processor cycles (160 ns). $\overline{HBE}$ is released during "high byte read." This allows the processor to read the lower byte of data as soon as "high byte read" is complete. The low byte read operation executes in a similar manner to the first and is completed during the next 160 ns.

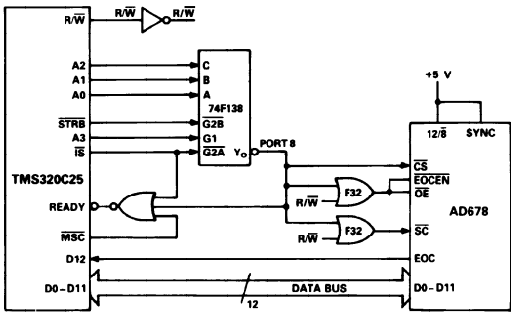


Figure 14. AD678 to TMS320C25 Interface

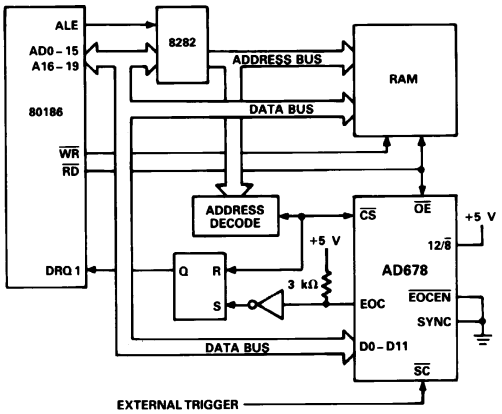


Figure 15. AD678 to 80186 DMA Interface

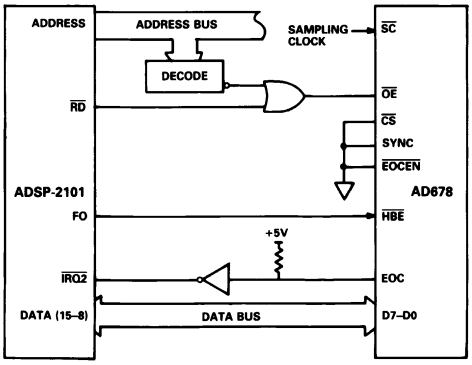


Figure 16. AD678 to ADSP-2101 Interface

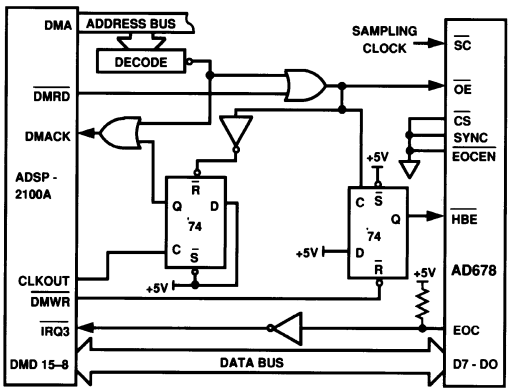
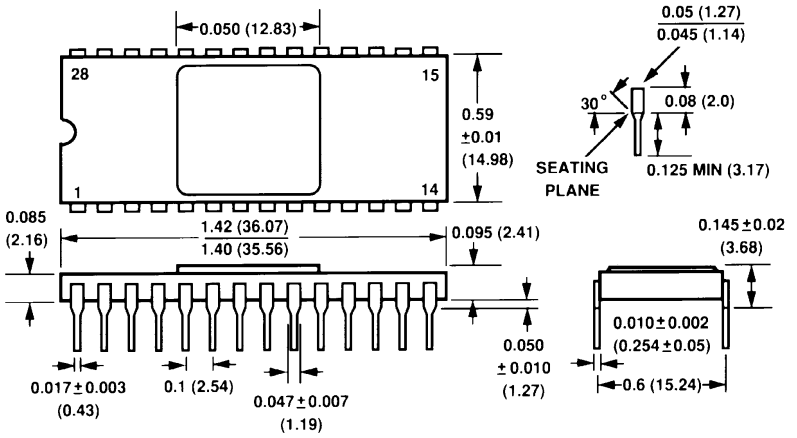


Figure 17. AD678 to ADSP-2100A Interface

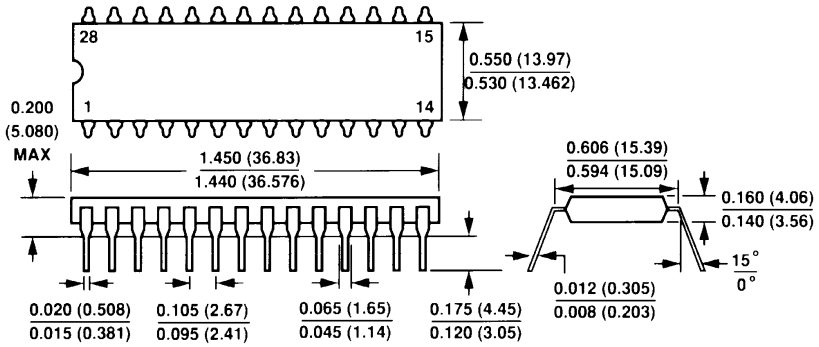
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Ceramic DIP Package (D-28)



28-Lead Plastic DIP Package (N-28A)

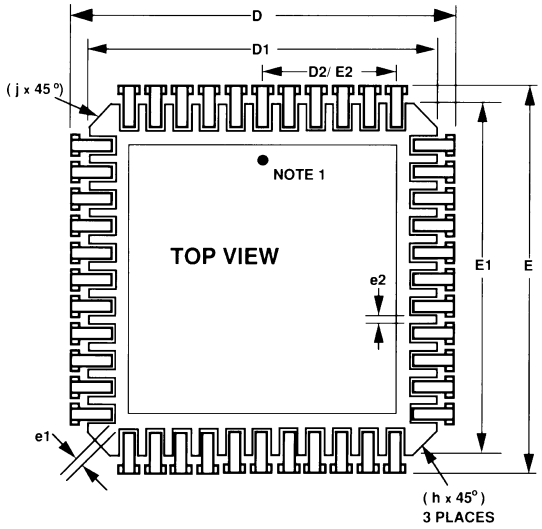


LEADS ARE SOLDER DIPPED OR TIN-PLATED ALLOY 42 OR COPPER.

OUTLINE DIMENSIONS

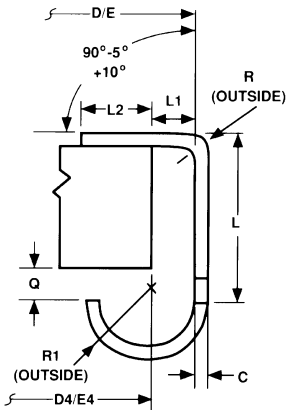
Dimensions shown in inches and (mm).

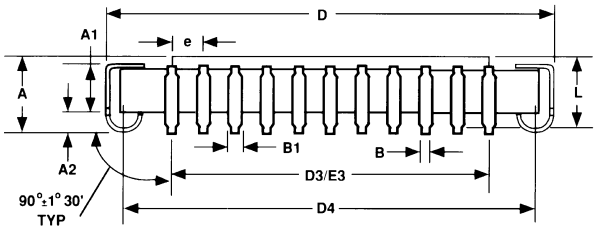
44-Terminal Lead Ceramic (J-44)



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.100	0.135	2.54	3.43	2
A1	0.054	0.078	1.37	1.98	
A2	0.025	–	0.64	–	
B	0.013	0.023	0.33	0.58	3
B1	0.020	0.032	0.51	0.81	3
C	0.006	0.013	0.15	0.33	3
D / E	0.680	0.700	17.27	17.78	
D1 / E1	0.628	0.662	15.95	16.82	
D2 / E2	0.250 BSC		6.35 BSC		
D3 / E3	0.500 BSC		12.70 BSC		
D4 / E4	0.610	0.650	15.49	16.51	
e	0.050 BSC		1.27 BSC		
e1/ e2	0.012	–	0.30	–	
L	0.030	–	0.76	–	
L1	0.005	–	0.12	–	
L2	0.025	–	0.76	–	
Q	0.003	–	0.08	–	
R	0.015	–	0.38	–	
R1	0.025	0.040	0.76	1.02	
h	0.040 REF		1.02 REF		
j	0.020 REF		0.52 REF		

NOTES
1. Pin 1 indicator is on the bottom of the package.
2. Dimension A controls the overall package thickness.
3. All Leads - increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.





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