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6/08—Rev. A to Rev. B

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Added Major Code Transition Glitch Impulse Section 12
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4/07—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = +5 V ± 5%, AV_{SS} = 0 V or −5 V ± 5%, V_{REFP} = +2.5 V, V_{REFN} = 0 V or −2.5 V, R_{LOAD} = 2 kΩ. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 1.

Parameter	Value	Unit	Test Conditions/Comments
ACCURACY			
Resolution	12	Bits	
Relative Accuracy (INL)	±1	LSB max	Y grade, AV_{SS} = −5 V, outputs unloaded
	±1	LSB max	Y grade, AV_{SS} = 0 V[2]
Differential Nonlinearity (DNL)	±1	LSB max	Guaranteed monotonic
Linearity Matching	±1	LSB typ	
Zero-Scale Error	±6	LSB max	AV_{SS} = −5 V
Full-Scale Error	±6	LSB max	AV_{SS} = −5 V
Zero-Scale Error	±12	LSB max	AV_{SS} = 0 V[2]
Full-Scale Error	±12	LSB max	AV_{SS} = 0 V[2]
Zero-Scale Temperature Coefficient[3]	±10	ppm FSR/°C typ	AV_{SS} = −5 V
Full-Scale Temperature Coefficient[3]	±10	ppm FSR/°C typ	AV_{SS} = −5 V
REFERENCE INPUT			
V_{REFP}			
Reference Input Range[4]	V_{REFN} + 2.5	V min	
	AV_{DD} − 2.5	V max	
Input Current	±0.75	mA max	Typically 0.25 mA
V_{REFN}			
Reference Input Range[4]	AV_{SS}	V min	
	0 V	V min	AV_{SS} = 0 V
	V_{REFP} − 2.5	V max	
Input Current	−1.0	mA max	Typically −0.6 mA, AV_{SS} = −5 V
Large Signal Bandwidth[3]	160	kHz typ	−3 dB, V_{REFP} = 0 V to 10 V p-p
OUTPUT CHARACTERISTICS[3]			
Output Current	±1.25	mA max	AV_{SS} = −5 V
DIGITAL INPUTS			
Input High Voltage, V_{IH}	2.4	V min	
Input Low Voltage, V_{IL}	0.8	V max	
Input Current[3]	10	µA max	
Input Capacitance[3]	5	pF typ	
POWER SUPPLY CHARACTERISTICS			
Power Supply Sensitivity[3]	0.002	%/% max	Typically 0.0004%/%
AI_{DD}	1.5	mA/channel max	Outputs unloaded, typically 0.75 mA, V_{IL} = DGND, V_{IH} = 5 V
AI_{SS}	1.5	mA/channel max	Outputs unloaded, typically 0.75 mA, V_{IL} = DGND, V_{IH} = 5 V
Power Dissipation	30	mW max	Outputs unloaded, typically 15 mW, AV_{SS} = 0 V

[1] All supplies can be varied ±5% and operation is guaranteed. Device is tested with AV_{DD} = 4.75 V.
[2] For single-supply operation (V_{REFN} = 0 V, AV_{SS} = 0 V), due to internal offset errors, INL and DNL are measured beginning at Code 0x005.
[3] Guaranteed by design and characterization, not production tested.
[4] Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.

AV_{DD} = +15 V ± 5%, AV_{SS} = −15 V ± 5%, V_{REFP} = +10 V, V_{REFN} = −10 V, R_{LOAD} = 2 kΩ. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 2.

Parameter	Value	Unit	Test Conditions/Comments
ACCURACY			
Resolution	12	Bits	
Relative Accuracy (INL)	±0.5	LSB max	Y grade
Differential Nonlinearity (DNL)	±1	LSB max	Guaranteed monotonic
Linearity Matching	±1	LSB max	
Zero-Scale Error	±3	LSB max	
Full-Scale Error	±3	LSB max	
Zero-Scale Temperature Coefficient[2]	±4	ppm FSR/°C typ	
Full-Scale Temperature Coefficient[2]	±4	ppm FSR/°C typ	
REFERENCE INPUT			
V_{REFP}			
Reference Input Range[3]	V_{REFN} + 2.5	V min	
	AV_{DD} − 2.5	V max	
Input Current	±2	mA max	Code 0x000, Code 0x555, typically 1 mA
V_{REFN}			
Reference Input Range[3]	−10 V	V min	
	V_{REFP} − 2.5	V max	
Input Current[2]	−3.5	mA min	Code 0x000, Code 0x555, typically −2 mA
Large Signal Bandwidth[2]	450	kHz typ	−3 dB, V_{REFP} = 0 V to 2.5 V p-p
OUTPUT CHARACTERISTICS[2]			
Output Current	±5	mA max	
DIGITAL INPUTS			
Input High Voltage, V_{IH}	2.4	V min	
Input Low Voltage, V_{IL}	0.8	V max	
Input Current[2]	10	µA max	
Input Capacitance[2]	5	pF typ	
POWER SUPPLY CHARACTERISTICS			
Power Supply Sensitivity[2]	0.002	%/% max	Typically 0.0004%/%
AI_{DD}	2	mA/channel max	Outputs unloaded, typically 1.25 mA, V_{IL} = DGND, V_{IH} = 5 V
AI_{SS}	2	mA/channel max	Outputs unloaded, typically 1.25 mA, V_{IL} = DGND, V_{IH} = 5 V
Power Dissipation	240	mW max	

[1] All supplies can be varied ±5% and operation is guaranteed.
[2] Guaranteed by design and characterization, not production tested.
[3] Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.

AC PERFORMANCE CHARACTERISTICS

AV_{DD} = +5 V ± 5% or +15 V ± 5%, AV_{SS} = −5 V ± 5% or 0 V or −15 V ± 5%, GND = 0 V, V_{REFP} = +2.5 V or +10 V, V_{REFN} = −2.5 V or 0 V or −10 V, R_{LOAD} = 2 kΩ. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 3.

Parameter	A Grade	B Grade	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Output Voltage Settling Time (t_S)	13	13	µs typ	To 0.01%, ±10 V voltage swing
	9	9	µs typ	To 0.01%, ±2.5 V voltage swing, AV_{DD} = 5 V
Slew Rate	2.3	2.3	V/µs typ	10% to 90%, ±10 V voltage swing
	2	2	V/µs typ	10% to 90%, ±2.5 V voltage swing
Analog Crosstalk	100	100	dB typ	
Digital Feedthrough	0.25	0.25	nV-sec typ	
Large Signal Bandwidth	90	90	kHz typ	3 dB, V_{REFP} = 5 V + 10 V p-p, V_{REFN} = −10 V
Major Code Transition Glitch Impulse	30	30	nV-sec typ	Code transition = 0x7FF to 0x800 and vice versa

[1] Guaranteed by design and characterization, not production tested.

TIMING CHARACTERISTICS

AV_{DD} = +15 V or +5 V, AV_{SS} = −15 V or −5 V or 0 V, GND = 0 V; V_{REFP} = +10 V or +2.5 V; V_{REFN} = −10 V or −2.5 V or 0 V, R_{LOAD} = 2 kΩ, C_L = 200 pF. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1, 2]

Table 4.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_{DS}	5	ns	Data setup time
t_{DH}	5	ns	Data hold time
t_{CH}	13	ns	Clock pulse width high
t_{CL}	13	ns	Clock pulse width low
t_{CSS}	13	ns	Select time
t_{CSH}	13	ns	Deselect delay
t_{LD1}	20	ns	Load disable time
t_{LD2}	20	ns	Load delay
t_{LDW}	20	ns	Load pulse width
t_{CLRW}	20	ns	Clear pulse width

[1] Guaranteed by design and characterization, not production tested.
[2] All input control signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

Timing Diagrams

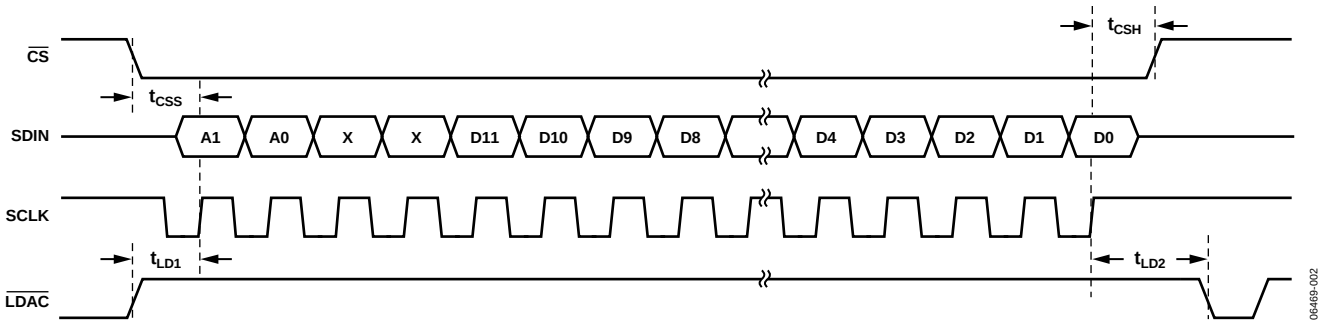


Figure 2. Data Load Sequence

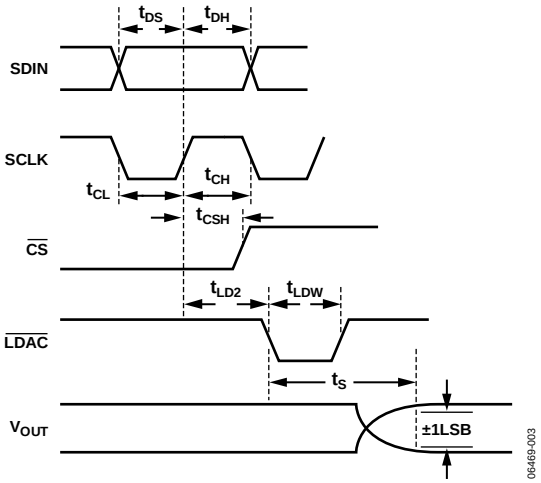


Figure 3. Data Load Timing

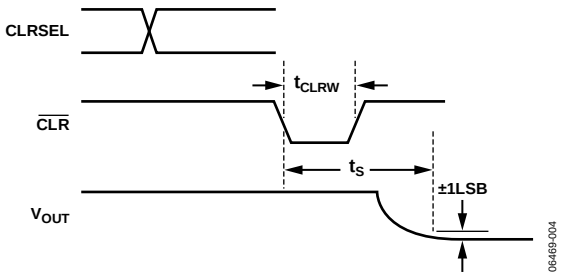


Figure 4. Clear Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents up to 100 mA do not cause SCR latch-up.

Table 5.

Parameter	Rating
AV_{SS} to GND	+0.3 V to −17 V
AV_{DD} to GND	−0.3 V to +17 V
AV_{SS} to AV_{DD}	−0.3 V to +34 V
AV_{SS} to V_{REFN}	−0.3 V to +AV_{SS} − 2 V
Current into Any Pin	±15 mA
Digital Input Voltage to GND	−0.3 V to +7 V
Digital Output Voltage to GND	−0.3 V to +7 V
Operating Temperature Range	
Industrial	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	145°C
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6.

Package Type	θ_{JA}	θ_{JC}	Unit
16-Lead SSOP	151	28	°C/W
16-Lead SOIC	124.9	42.9	°C/W
20-Lead SSOP	126	46	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

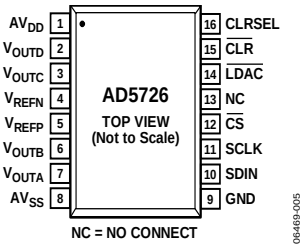


Figure 5. 16-Lead SSOP and 16-Lead SOIC Pin Configuration

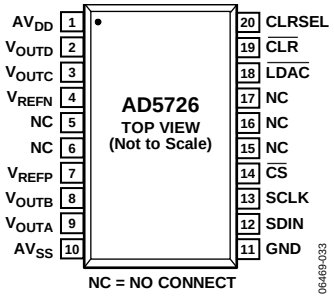


Figure 6. 20-Lead SSOP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.			
16-Lead SSOP/SOIC	**20-Lead SSOP**	**Mnemonic**	**Description**
1	1	AV_{DD}	Positive Analog Supply Pin. Voltage range is from 5 V to 15 V.
2	2	V_{OUTD}	Buffered Analog Output Voltage of DAC D.
3	3	V_{OUTC}	Buffered Analog Output Voltage of DAC C.
4	4	V_{REFN}	Negative DAC Reference Input. The voltage applied to this pin defines the zero-scale output. Allowable range is AV_{SS} to $V_{REFP} - 2.5$ V.
5	7	V_{REFP}	Positive DAC Reference Input. The voltage applied to this pin defines the full-scale output voltage. Allowable range is $AV_{DD} - 2.5$ V to $V_{REFN} + 2.5$ V.
6	8	V_{OUTB}	Buffered Analog Output Voltage of DAC B.
7	9	V_{OUTA}	Buffered Analog Output Voltage of DAC A.
8	10	AV_{SS}	Negative Analog Supply Pin. Voltage range is from 0 V to −15 V.
9	11	GND	Ground Reference Pin.
10	12	SDIN	Serial Data Input. Data must be valid on the rising edge of SCLK. This input is ignored when $\overline{CS}$ is high.
11	13	SCLK	Serial Clock Input. Data is clocked into the input register on the rising edge of SCLK.
12	14	$\overline{CS}$	Active Low Chip Select Pin. This pin must be active for data to be clocked in. This pin is logically OR'ed with the SCLK input and disables the serial data input when high.
13	5, 6, 15, 16, 17	NC	No Internal Connection.
14	18	$\overline{LDAC}$	Active Low, Asynchronous Load DAC Input. The data currently contained in the serial input register is transferred out to the DAC data registers on the falling edge of $\overline{LDAC}$, independent of $\overline{CS}$. Input data must remain stable while $\overline{LDAC}$ is low.
15	19	$\overline{CLR}$	Active Low Input. Sets input register and DAC registers to zero-scale (0x000) or midscale (0x800), depending on the state of CLRSEL. The data in the serial input register is unaffected by this control.
16	20	CLRSEL	Determines the action of $\overline{CLR}$. If high, a clear command sets the internal DAC registers to midscale (0x800). If low, the registers are set to zero (0x000).

TYPICAL PERFORMANCE CHARACTERISTICS

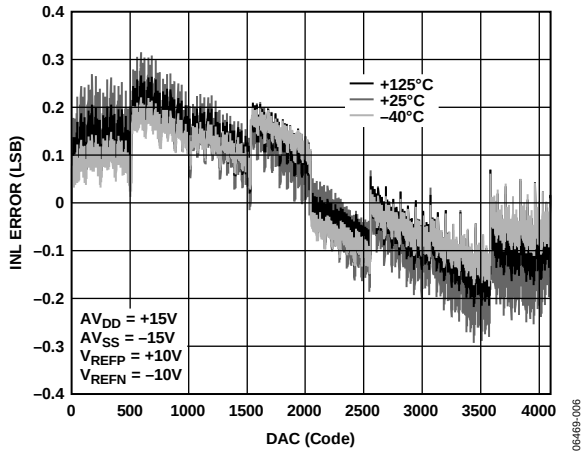


Figure 7. INL Error vs. DAC Code

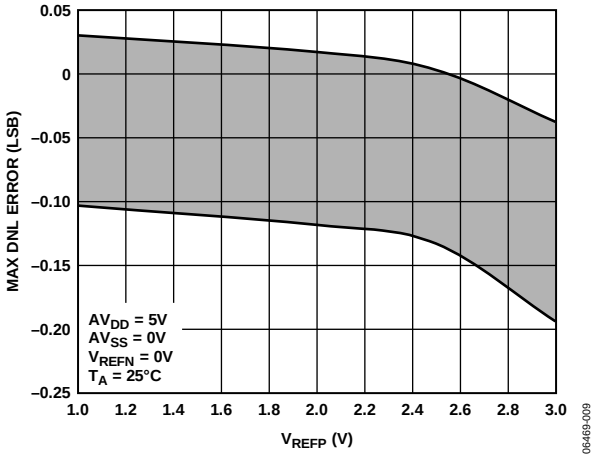


Figure 10. Maximum DNL Error vs. V_{REFP}

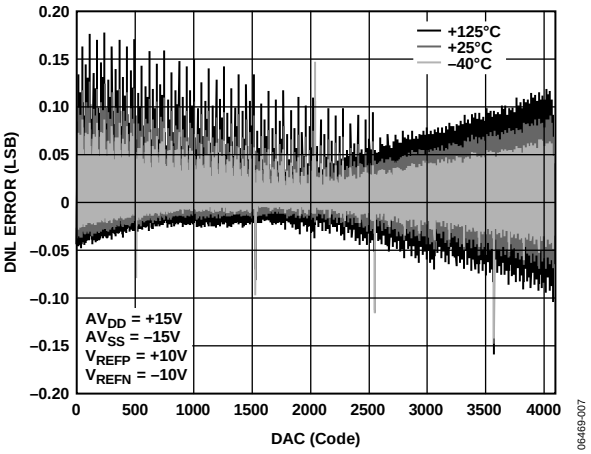


Figure 8. DNL Error vs. DAC Code

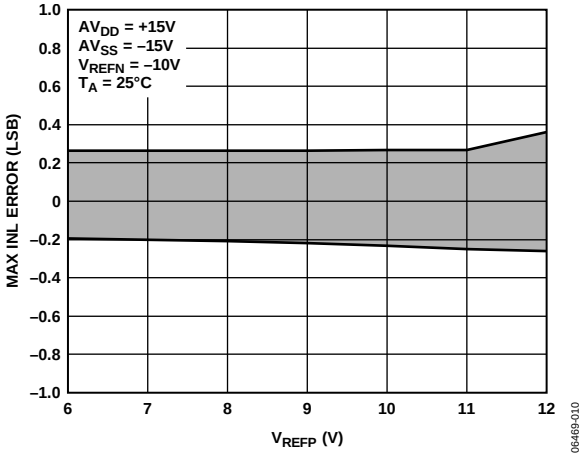


Figure 11. Maximum INL Error vs. V_{REFP}

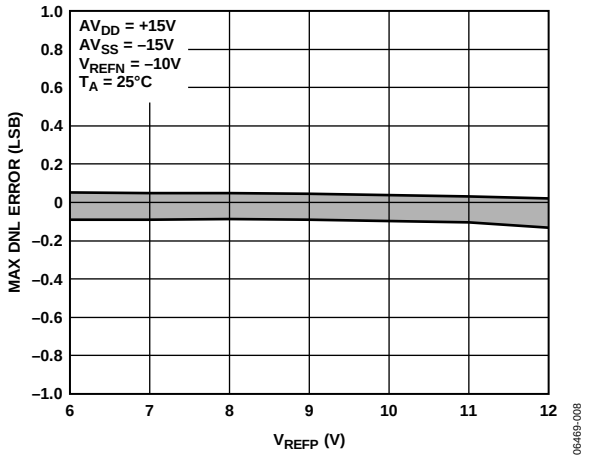


Figure 9. Maximum DNL Error vs. V_{REFP}

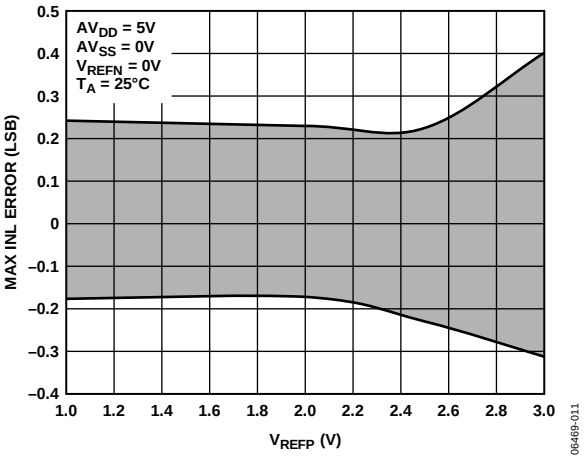


Figure 12. Maximum INL Error vs. V_{REFP}

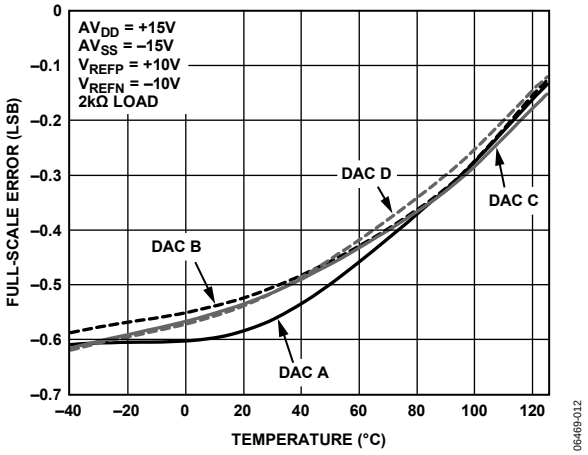


Figure 13. Full-Scale Error vs. Temperature

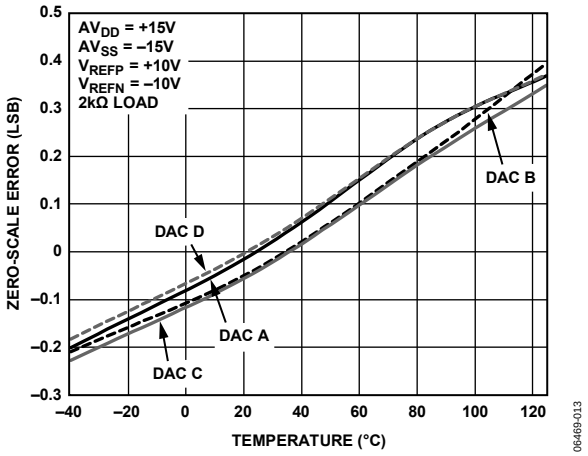


Figure 14. Zero-Scale Error vs. Temperature

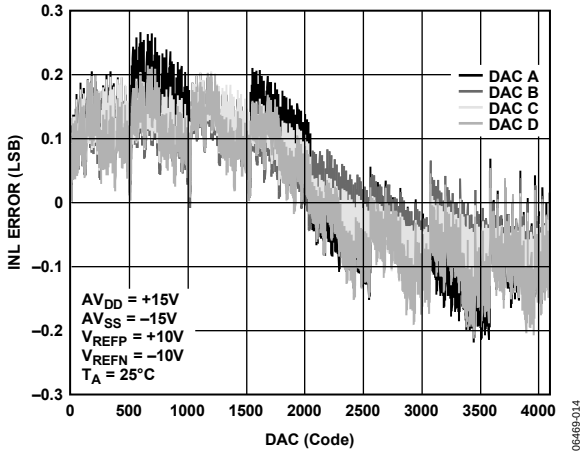


Figure 15. Channel-to-Channel Matching

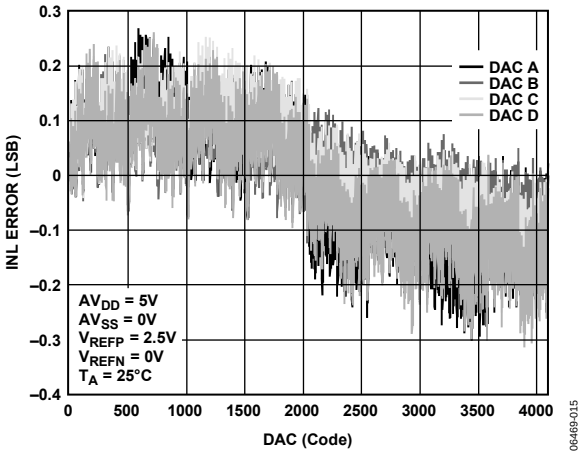


Figure 16. Channel-to-Channel Matching

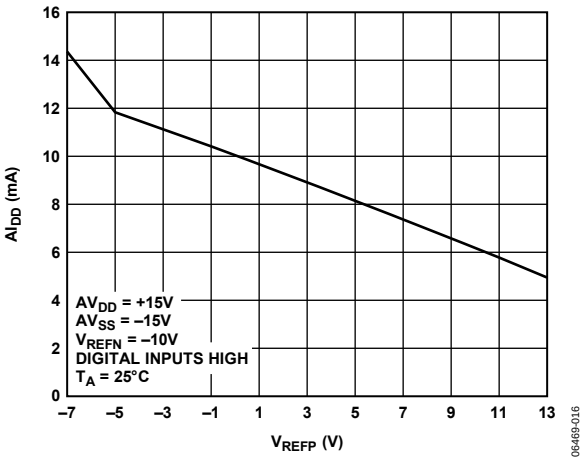


Figure 17. AI_{DD} vs. V_{REFP}, All DACs Loaded with Full-Scale Code

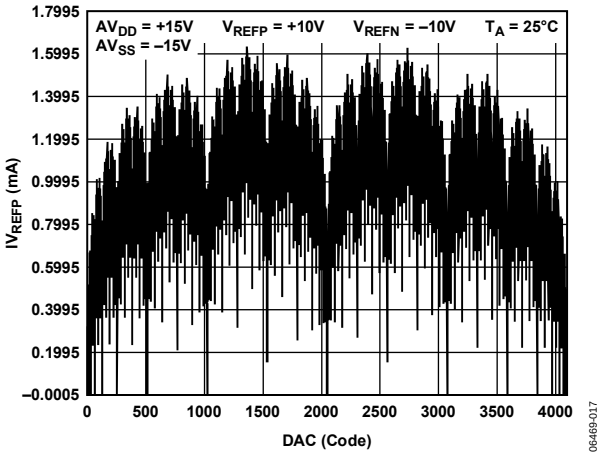


Figure 18. IV_{REFP} vs. DAC Code

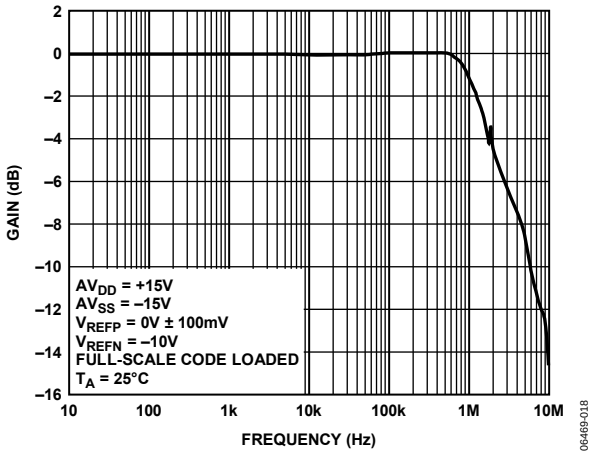


Figure 19. Small Signal Response

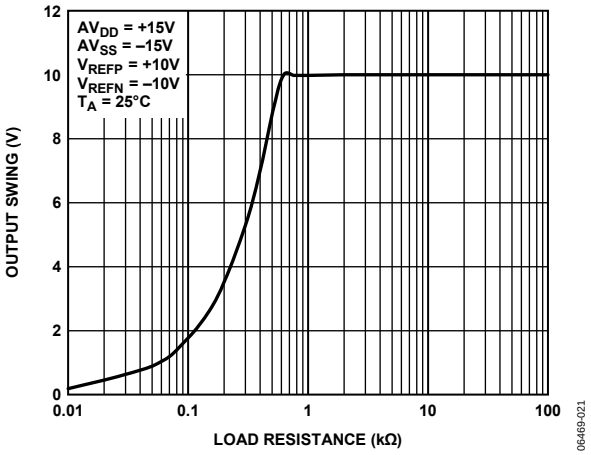


Figure 22. Output Swing vs. Load Resistance

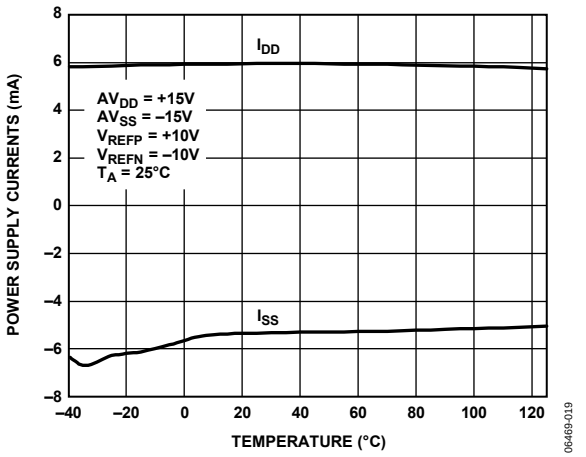


Figure 20. Power Supply Currents vs. Temperature

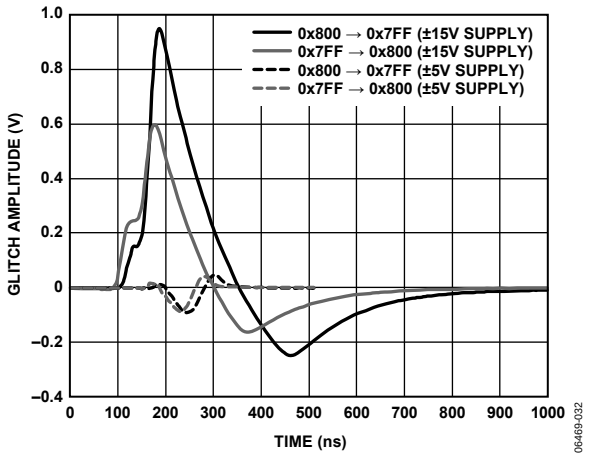


Figure 23. Major Code Transition Glitch

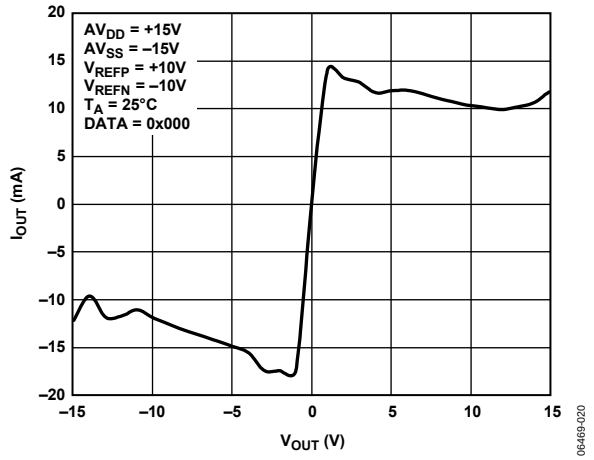


Figure 21. Output Current vs. Output Voltage

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot is shown in Figure 7.

Differential Nonlinearity (DNL)
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot is shown in Figure 8.

Monotonicity
A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5726 is monotonic over its full operating temperature range.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code is loaded to the DAC register. Ideally, the output should be V_{REFP} − 1 LSB. Full-scale error is expressed in LSBs. A plot of full-scale error vs. temperature is shown in Figure 13.

Zero-Scale Error
Zero-scale error is the error in the DAC output voltage when 0x0000 (straight binary coding) is loaded to the DAC register. Ideally, the output voltage should be V_{REFN}. A plot of zero-scale error vs. temperature is shown in Figure 14.

Zero-Scale Error Temperature Coefficient
Zero-scale error temperature coefficient is a measure of the change in zero-scale error with a change in temperature. Zero-scale error temperature coefficient is expressed in ppm FSR/°C.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

Slew Rate
The slew rate of a device is a limitation in the rate of change of the output voltage. The output slewing speed of a voltage-output DAC converter is usually limited by the slew rate of the amplifier used at its output. Slew rate is measured from 10% to 90% of the output signal and is given in V/µs.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus.

Power Supply Sensitivity
Power supply sensitivity indicates how the output of the DAC is affected by changes in the power supply voltage.

Analog Crosstalk
Analog crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC. It is expressed in decibels.

Major Code Transition Glitch Impulse
Major code transition glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state, but the output voltage remains constant. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major code transition (0x7FF to 0x800 and 0x800 to 0x7FF). See Figure 23.

THEORY OF OPERATION

The AD5726 is a quad, 12-bit, serial input, unipolar/bipolar voltage output DAC. It operates from single-supply voltages of +5 V to +15 V or dual-supply voltages of ±5 V to ±15 V. The four outputs are buffered and capable of driving a 2 kΩ load. Data is written to the AD5726 in a 16-bit word format via a 3-wire serial interface.

DAC ARCHITECTURE

Each of the four DACs is a voltage switched, high impedance (50 kΩ), R-2R ladder configuration. Each 2R resistor is driven by a pair of switches that connect the resistor to either V_{REFP} or V_{REFN}.

OUTPUT AMPLIFIERS

The AD5726 features buffered analog voltage outputs capable of sourcing and sinking up to 5 mA when operating from ±15 V supplies, eliminating the need for external buffer amplifiers in most applications while maintaining specified accuracy over the rated operating conditions. The output amplifiers are short-circuit protected. The designer should verify that the output load meets the capabilities of the device, in terms of both output current and load capacitance. The AD5726 is stable with capacitive loads up to 2 nF typically. However, any capacitance load increases the settling time and should be minimized if speed is a concern.

The output stage includes a P-channel MOSFET to pull the output voltage down to the negative supply. This is very important in single-supply systems where V_{REFN} usually has the same potential as the negative supply. With no load, the zero-scale output voltage in these applications is less than 500 μV typically, or less than 1 LSB when V_{REFP} = 2.5 V. However, when sinking current, this voltage increases because of the finite impedance of the output stage. The effective value of the pull-down resistor in the output stage is typically 320 Ω. With a 100 kΩ resistor connected to 5 V, the resulting zero-scale output voltage is 16 mV. Thus, the best single-supply operation is obtained with the output load connected to ground, so the output stage does not have to sink current.

Like all amplifiers, the AD5726 output buffers generate voltage noise, 5 nV/√Hz typically. This is easily reduced by adding a simple RC low-pass filter on each output.

REFERENCE INPUTS

The two reference inputs of the AD5726 allow a great deal of flexibility in circuit design. The user must take care, however, to observe the minimum voltage input levels on V_{REFP} and V_{REFN} to maintain the accuracy shown in the data sheet. These input voltages can be set anywhere across a wide range within the supplies, but must be a minimum of 2.5 V apart in any case (see Figure 24). A wide output voltage range can be obtained with ±5 V references that can be provided by the AD588 as shown in Figure 26. Many applications utilize the DACs to synthesize symmetric bipolar waveforms, which require an accurate, low drift bipolar reference. The AD588 provides both voltages and needs no external components. Additionally, the part is trimmed in production for 12-bit accuracy over the full temperature range without user calibration.

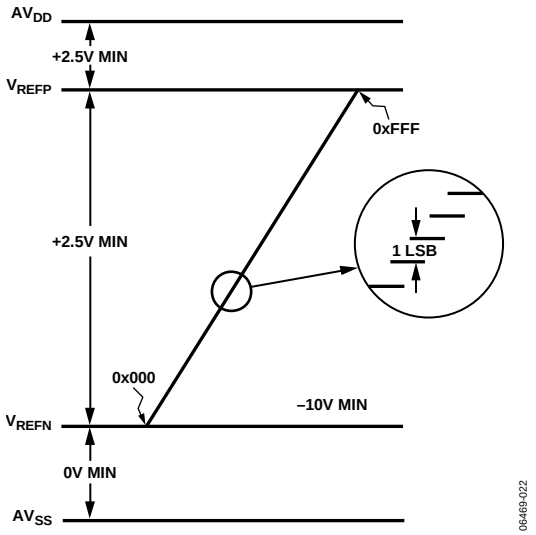


Figure 24. Output Voltage Range Programming

When driving the reference input, it is important to note that V_{REFP} both sinks and sources current, and that the input currents of both are code dependent. Many voltage reference products have limited current sinking capabilities and must be buffered with an amplifier to drive V_{REFP} to maintain overall system accuracy. The input, V_{REFN}, however, has no such requirement.

For a single 5 V supply, V_{REFP} is limited to 2.5 V at the most, and must always be at least 2.5 V less than the positive supply to ensure linearity of the device. For these applications, the AD780 is an excellent low drift 2.5 V reference. It works well with the AD5726 in a single 5 V system, as shown in Figure 28.

It is recommended that the reference inputs be bypassed with 0.2 μF capacitors when operating with ±10 V references. This limits the reference bandwidth.

V_{REFP} Input Requirements

The AD5726 uses a DAC switch driver circuit that compensates for different supplies, reference voltages, and digital code inputs. This ensures that all DAC ladder switches are always biased equally, ensuring excellent linearity under all conditions. Thus, as indicated in the specifications, the V_{REFP} input of the AD5726 requires both sourcing and sinking current capability from the reference voltage source. Many positive voltage references are intended as current sources only and offer little sinking capability. The user should consider references such as the AD584, AD586, AD587, AD588, AD780, and REF43 for such an application.

SERIAL INTERFACE

The AD5726 is controlled over a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with SPI, QSPI™, MICROWIRE™, and DSP standards.

Input Shift Register

The input shift register is 16 bits wide. Data is loaded into the device MSB first as a 16-bit word under the control of a serial clock input, SCLK. The input register consists of two address bits, two don't care bits, and 12 data bits as shown in Table 10. The timing diagram for this operation is shown in Figure 2.

When $\overline{CS}$ is low, the data presented to the input, SDIN, is shifted MSB first into the internal shift register on the rising edge of SCLK. Once all 16 bits of the serial data-word have been input, the load control $\overline{LDAC}$ is strobed, and the word is latched onto the internal data bus. The two address bits are decoded and used to route the 12-bit data-word to the appropriate DAC data register.

Operation of $\overline{CS}$ and SCLK

The $\overline{CS}$ and SCLK pins are internally fed to the same logical OR gate and, therefore, require careful attention during a load cycle to avoid clocking in false data bits. As shown in the timing diagram in Figure 2, SCLK must be halted high, or $\overline{CS}$ must be brought high, during the last high portion of SCLK following the rising edge that clocked in the last data bit. Otherwise, an additional rising edge is generated by $\overline{CS}$ rising while SCLK is low, causing $\overline{CS}$ to act as the clock and allowing a false data bit into the input shift register. The same must also be considered for the beginning of the data load sequence.

Coding

The AD5726 uses binary coding. The output voltage can be calculated from the following equation:

$$V_{OUT} = V_{REFN} + \frac{(V_{REFP} - V_{REFN}) \times D}{4096}$$

where D is the digital code in decimal.

Load DAC ($\overline{LDAC}$)

When asserted, the $\overline{LDAC}$ pin is an asynchronous, active low, digital input that transfers the contents of the input register to the internal data bus, updating the addressed DAC output. New data must not be programmed to the AD5726 while the $\overline{LDAC}$ pin is low.

$\overline{CLR}$ and CLRSEL

The $\overline{CLR}$ control allows the user to perform an asynchronous clear function. Asserting $\overline{CLR}$ loads all four DAC registers, forcing the DAC outputs to either zero scale (0x000) or midscale (0x800), depending on the state of CLRSEL as shown in Table 8. The $\overline{CLR}$ function is asynchronous and independent of $\overline{CS}$. When $\overline{CLR}$ returns high, the DAC outputs remain at the clear value until $\overline{LDAC}$ is strobed, reloading the individual DAC registers with either the data held in the input register prior to the clear or with new data loaded through the serial interface.

Table 8. $\overline{CLR}$/CLRSEL Truth Table

$\overline{CLR}$	CLRSEL	DAC Registers
0	0	Zero scale (0x000)
0	1	Midscale (0x800)
1	0	No change
1	1	No change

Table 9. DAC Address Word Decode Table

A1	A0	DAC Addressed
0	0	DAC A
0	1	DAC B
1	0	DAC C
1	1	DAC D

Table 10. Input Register Format

DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8	DB9	DB10	DB11	DB12	DB13	DB14	DB15
A1	A0	X	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

APPLICATIONS INFORMATION

POWER-UP SEQUENCE

To prevent CMOS latch-up conditions, powering AV_{DD}, AV_{SS}, and GND prior to any reference voltages is recommended. The ideal power-up sequence is GND, AV_{SS}, AV_{DD}, V_{REFP}, V_{REFN}, and the digital inputs. Noncompliance with the power-up sequence over an extended period can elevate the reference currents and eventually damage the device. On the other hand, if the noncompliant power-up sequence condition is as short as a few milliseconds, the device can resume normal operation without damage once AV_{DD}/AV_{SS} are powered up.

REFERENCE CONFIGURATION

Output voltage ranges can be configured as either unipolar or bipolar, and within these choices, a wide variety of options exists. The unipolar configuration can be either a positive (as shown in Figure 25) or a negative voltage output. The bipolar configuration can be either symmetrical (as shown in Figure 26) or nonsymmetrical.

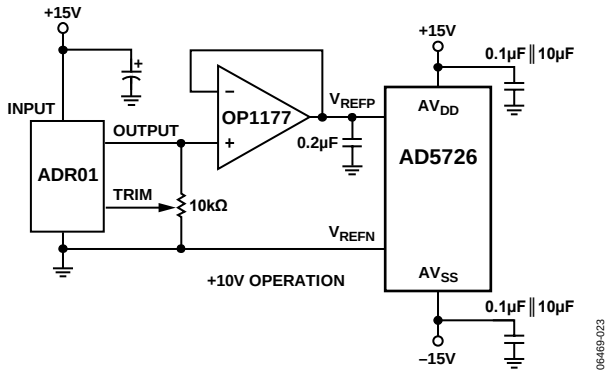


Figure 25. Unipolar +10 V Operation

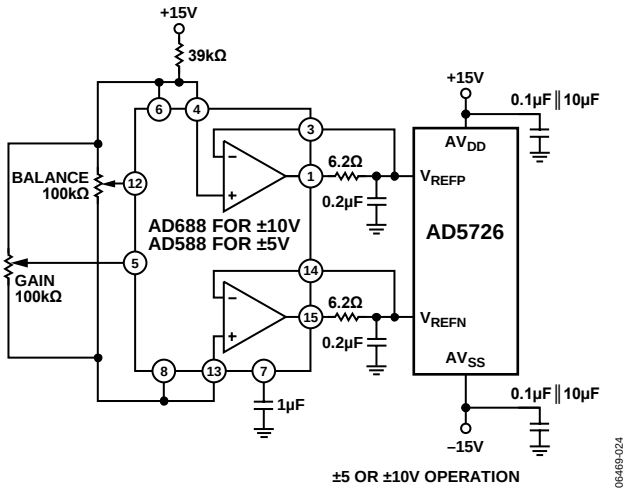


Figure 26. Symmetrical Bipolar Operation

Figure 26 (symmetrical bipolar operation) shows the AD5726 configured for ±10 V operation. See the AD688 data sheet for a full explanation of the reference operation.

Adjustments may not be necessary for many applications because the AD688 is a very high accuracy reference. However, if additional adjustments are required, adjust the AD5726 full-scale first. Begin by loading the digital full-scale code (0xFFF). Then, modify the gain adjust potentiometer to attain a DAC output voltage of 9.9976 V. Next, alter the balance adjust to set the midscale output voltage to 0.000 V.

The 0.2 µF bypass capacitors shown at their reference inputs in Figure 26 should be used whenever ±10 V references are used. Applications with single references or references to ±5 V may not require the 0.2 µF bypassing. The 6.2 Ω resistor in series with the output of the reference amplifier keeps the amplifier from oscillating with the capacitive load. This has been found to be large enough to stabilize this circuit. Larger resistor values are acceptable if the drop across the resistor does not exceed a V_{BE}. Assuming a minimum V_{BE} of 0.6 V and a maximum current of 2.75 mA, the resistor should be under 200 Ω for the loading of a single AD5726.

Using two separate references is not recommended. Having two references may cause different drifts with time and temperature, whereas with a single reference, most drifts track.

Unipolar positive full-scale operation can usually be set by a reference with the correct output voltage. This is preferable to using a reference and dividing down to the required value. For a +10 V full-scale output, the circuit can be configured as shown in Figure 25. In this configuration, the full-scale value is first set by adjusting the 10 kΩ resistor for a full-scale output of 9.9976 V.

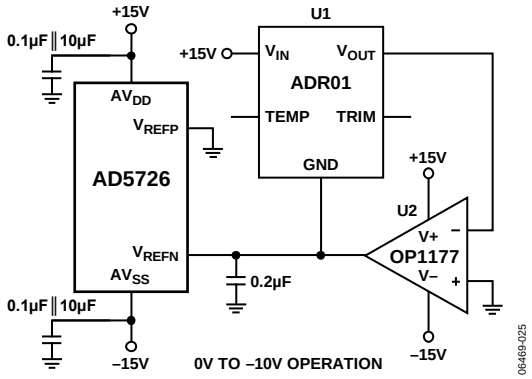


Figure 27. Unipolar –10 V Operation

Figure 27 shows the AD5726 configured for –10 V to 0 V operation. An ADR01 and OP1177 are configured to produce a –10 V output that is connected directly to V_{REFP} for the reference voltage.

Single 5 V Supply Operation

For operation with a 5 V supply, the reference voltage should be set between 1.0 V and 2.5 V for optimum linearity. Figure 28 shows an AD780 used to supply a 2.5 V reference voltage. The headroom of the reference and DAC are both sufficient to support a +5 V supply with ±5 V tolerance.

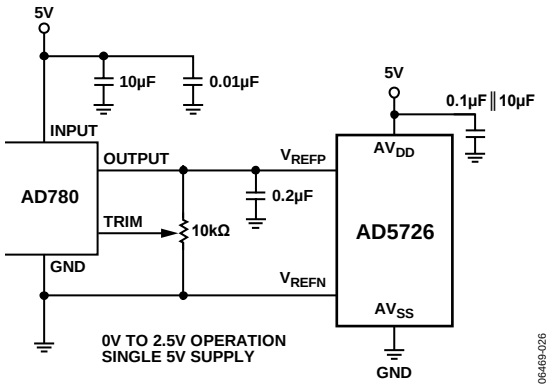


Figure 28. 5 V Single-Supply Operation

POWER SUPPLY BYPASSING AND GROUNDING

In any circuit where accuracy is important, careful consideration to the power supply and ground return layout helps to ensure the rated performance. The AD5726 has a single ground pin that is internally connected to the digital section as the logic reference level. The user's first instinct may be to connect this pin to the digital ground; however, in large systems, the digital ground is often noisy because of the switching currents of other digital circuitry. Any noise introduced at the ground pin could couple into the analog output. Thus, to avoid error-causing digital noise in the sensitive analog circuitry, the ground pin should be connected to the system analog ground.

The ground path (circuit board trace) should be as wide as possible to reduce any effects of parasitic inductance and ohmic drops. A ground plane is recommended if possible. The noise immunity of the on-board digital circuitry, typically in the hundreds of millivolts, is well able to reject the common-mode noise typically seen between system analog and digital grounds. Finally, connect the analog and digital ground to each other at a single point in the system to provide a common reference. This connection is preferably done at the power supply.

Good grounding practice is essential to maintain analog performance in the surrounding analog support circuitry as well. With two reference inputs and four analog outputs capable of moderate bandwidth and output current, there is a significant potential for ground loops. Again, a ground plane is recommended as the most effective solution to minimize errors due to noise and ground offsets.

The AD5726 should have ample supply bypassing located as close to the package as possible. Recommended capacitor values are 10 µF in parallel with 0.1 µF. The 0.1 µF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. Isocouplers provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5726 makes it ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 29 shows a 4-channel isolated interface connected to the AD5726 using an ADuM1400.

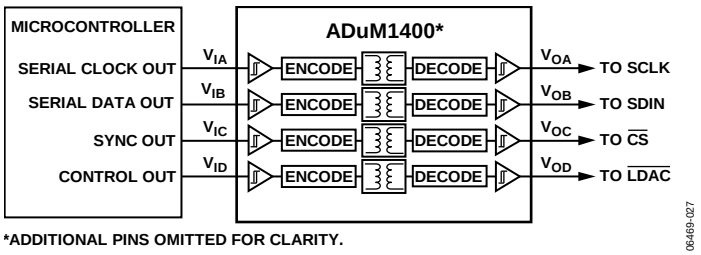


Figure 29. Isolated Interface

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5726 is via a serial bus that uses standard protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire interface (minimum) consisting of a clock signal, a data signal, and a synchronization signal. The AD5726 requires a 16-bit data-word with data valid on the falling edge of SCLK.

For all the interfaces, the DAC output update can be done automatically when all the data is clocked in, or it can be done under the control of $\overline{\text{LDAC}}$.

MC68HC11 Interface

Figure 30 shows an example of a serial interface between the AD5726 and the MC68HC11 microcontroller. The serial peripheral interface (SPI) on the MC68HC11 is configured for master mode (MSTR = 1); clock polarity bit (CPOL = 0), and the clock phase bit (CPHA = 1). The SPI is configured by writing to the SPI control register (SPCR); see the *68HC11 User Manual*. SCK of the MC68HC11 drives the SCLK of the AD5726, the MOSI output drives the serial data line (SDIN) of the AD5726. The $\overline{\text{CS}}$ is driven from one of the port lines, in this case, PC7.

When data is being transmitted to the AD5726, the $\overline{\text{CS}}$ line (PC7) is taken low and data is transmitted MSB first. Data appearing on the MOSI output is valid on the falling edge of SCK. Eight falling clock edges occur in the transmit cycle; thus, to load the required 16-bit word, PC7 is not brought high until the second 8-bit word has been transferred to the input shift register of the DAC.

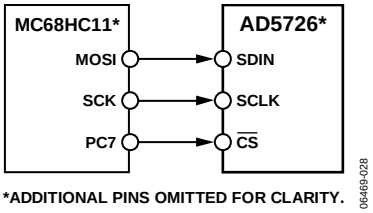


Figure 30. MC68HC11 to AD5726 Interface

8xC51 Interface

The AD5726 requires a clock synchronized to the serial data. For this reason, the 8xC51 must be operated in Mode 0. In this mode, serial data is transferred through RxD, and a shift clock is output on TxD.

P3.3 and P3.4 are bit-programmable pins on the serial port and are used to drive $\overline{\text{CS}}$ and $\overline{\text{LDAC}}$, respectively. The 8Cx51 provides the LSB of its SBUF register as the first bit in the data stream. The user must ensure that the data in the SBUF register is arranged correctly because the DAC expects MSB first. When data is to be transmitted to the DAC, P3.3 is taken low. Data on RxD is clocked out of the microcontroller on the rising edge of TxD and is valid on the falling edge. As a result, no glue logic is required between this DAC and the microcontroller interface.

The 8xC51 transmits data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Because the DAC expects a 16-bit word, $\overline{\text{CS}}$ (P3.3) must be left low after the first eight bits are transferred. After the second byte has been transferred, the P3.3 line is taken high. The DAC can be updated using $\overline{\text{LDAC}}$ via P3.4 of the 8xC51.

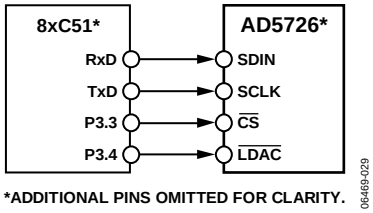


Figure 31. 8xC51 to AD5726 Interface

PIC16C6x/PIC16C7x Interface

The PIC16C6x/PIC16C7x synchronous serial port (SSP) is configured as an SPI master with the clock polarity bit set to 0. This is accomplished by writing to the synchronous serial port control register (SSPCON). See the *PIC16/17 Microcontroller User Manual*. In this example, I/O Port RA1 is used to pulse $\overline{\text{CS}}$ and enable the serial port of the AD5726. This microcontroller transfers only eight bits of data during each serial transfer operation; therefore, two consecutive write operations are needed. Figure 32 shows the connection diagram.

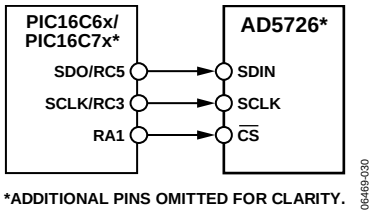


Figure 32. PIC16C6x/PIC16C7x to AD5726 Interface

Blackfin® DSP Interface

Figure 33 shows how the AD5726 can be interfaced to the Analog Devices Blackfin DSP. The Blackfin processor has an integrated SPI port that can be connected directly to the SPI pins of the AD5726. It also has programmable I/O pins that can be used to set the state of a digital input such as the $\overline{\text{LDAC}}$ pin.

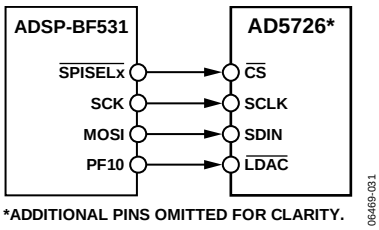
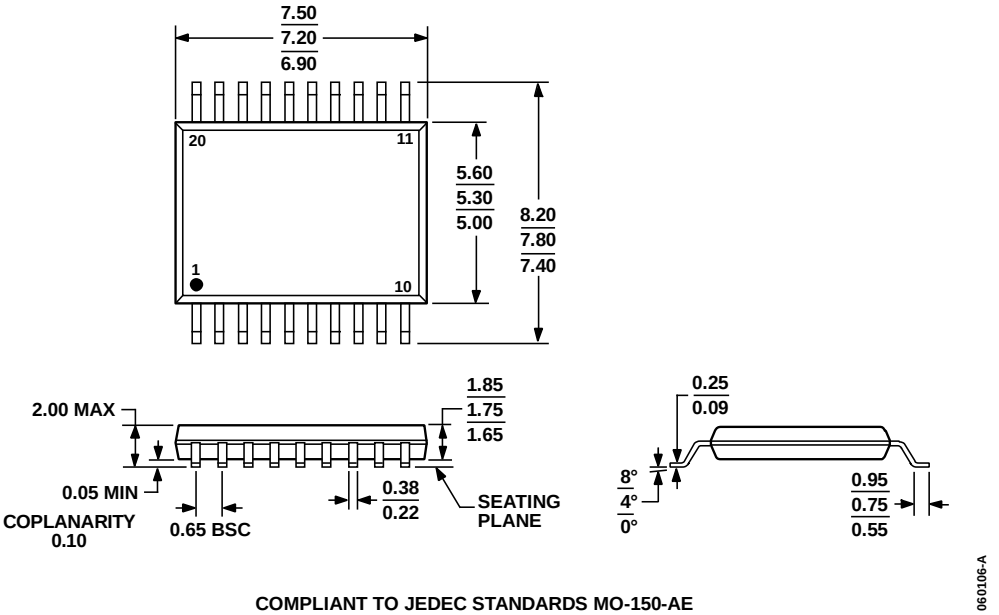


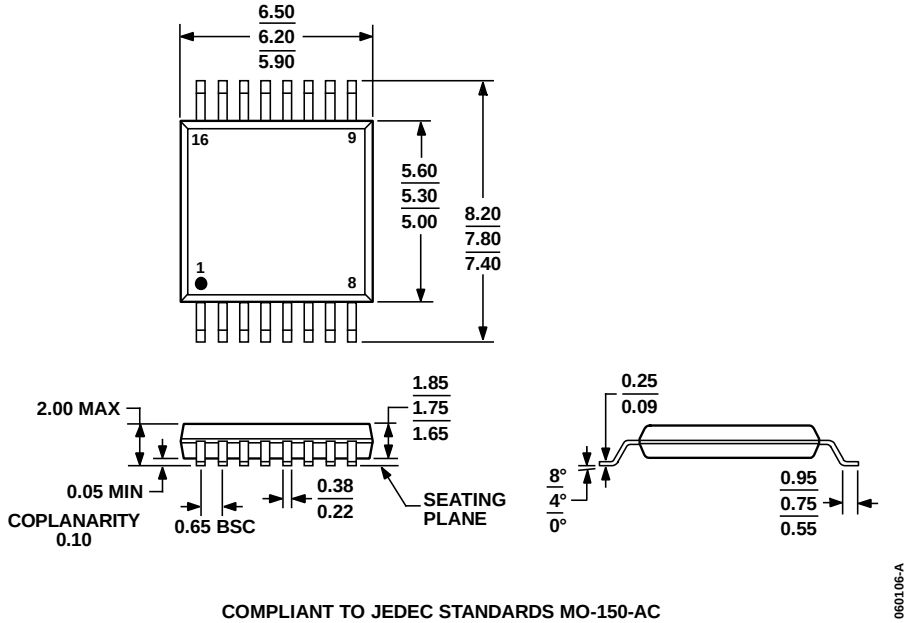
Figure 33. Blackfin DSP to AD5726 Interface

OUTLINE DIMENSIONS



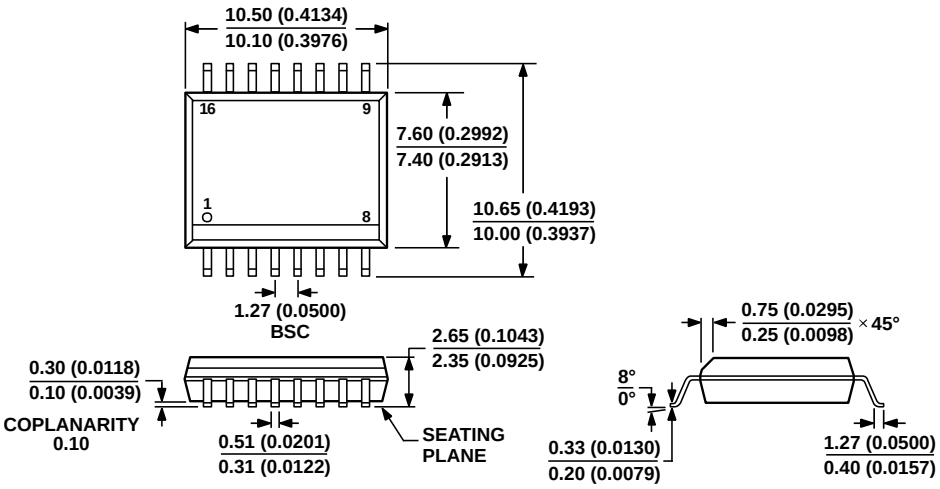
COMPLIANT TO JEDEC STANDARDS MO-150-AE

Figure 34. 20-Lead Shrink Small Outline Package [SSOP]
(RS-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-150-AC

Figure 35. 16-Lead Shrink Small Outline Package [SSOP]
(RS-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

03-27-2007-B

Figure 36. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD5726YRSZ-1REEL	−40°C to +125°C	20-Lead SSOP	RS-20
AD5726YRSZ-1500RL7	−40°C to +125°C	20-Lead SSOP	RS-20
AD5726YRSZ-500RL7	−40°C to +125°C	16-Lead SSOP	RS-16
AD5726YRSZ-REEL	−40°C to +125°C	16-Lead SSOP	RS-16
AD5726YRWZ-REEL	−40°C to +125°C	16-Lead SOIC_W	RW-16
AD5726YRWZ-REEL7	−40°C to +125°C	16-Lead SOIC_W	RW-16

[1] Z = RoHS Compliant Part.

NOTES

D06469-0-10/13(C)