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REVISION HISTORY

5/2016—Rev. B to Rev. C

Deleted WLCSP Package ... Universal
Changes to Figure 3 and Table 5 ... 6
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12/2005—Rev. A to Rev. B

Inserted Figure 4 and Table 6 ... 6
Inserted Figure 5 ... 7
Updated Outline Dimensions ... 15
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7/2005—Rev. 0 to Rev. A

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Updated Outline Dimensions ... 14
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12/2004—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, AGND = DGND = 0 V, load resistance R_L = 25 Ω connected to V_{DD}; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	B Version[1] Min	Typ	Max	Unit	Test Conditions/Comments
DC PERFORMANCE					V_{DD} = 3.6 V to 4.5 V; device operates over 2.7 V to 5.5 V with reduced performance
Resolution		10		Bits	117 µA/LSB
Relative Accuracy[2]		±1.5	±4	LSB	
Differential Nonlinearity[2, 3]			±1	LSB	Guaranteed monotonic over all codes
Zero Code Error[2, 4]	0	1	5	mA	All 0s loaded to DAC
Offset Error at Code 16[2]		0.5		mA	
Gain Error[2]			±0.6	% of FSR	At 25°C
Offset Error Drift[4, 5]		10		µA/°C	
Gain Error Drift[2, 5]		±0.2	±0.5	LSB/°C	
OUTPUT CHARACTERISTICS					
Minimum Sink Current[4]		3		mA	
Maximum Sink Current		120		mA	V_{DD} = 3.6 V to 4.5 V; device operates over 2.7 V to 5.5 V but specified maximum sink current might not be achieved
Output Current Durping PD		80		nA	PD = 1
Output Compliance[5]	0.6		V_{DD}	V	Output voltage range over which max sink current is available
Power-Up Time		20		µs	To 10% of FS, coming out of power-down mode; V_{DD} = 5 V
LOGIC INPUTS (PD)[5]					
Input Current			±1	µA	
Input Low Voltage, V_{INL}			0.8	V	V_{DD} = 2.7 V to 5.5 V
Input High Voltage, V_{INH}	0.7 V_{DD}			V	V_{DD} = 2.7 V to 5.5 V
Pin Capacitance		3		pF	
LOGIC INPUTS (SCL, SDA)[5]					
Input Low Voltage, V_{INL}	−0.3		0.3 V_{DD}	V	
Input High Voltage, V_{INH}	0.7 V_{DD}		V_{DD} + 0.3	V	
Input Leakage Current, I_{IN}			±1	µA	V_{IN} = 0 V to V_{DD}
Input Hysteresis, V_{HYST}	0.05 V_{DD}			V	
Digital Input Capacitance, C_{IN}		6		pF	
Glitch Rejection[6]			50	ns	Pulse width of spike suppressed
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
I_{DD} (Normal Mode)					I_{DD} specification is valid for all DAC codes
V_{DD} = 2.7 V to 5.5 V		2.5	4	mA	V_{IH} = V_{DD}, V_{IL} = GND, V_{DD} = 5.5 V
V_{DD} = 2.7 V to 4.5 V		2.3	3	mA	V_{IH} = V_{DD}, V_{IL} = GND, V_{DD} = 4.5 V
I_{DD} (Power-Down Mode)		0.5	1	µA	V_{IH} = V_{DD}, V_{IL} = GND

[1] Temperature range is as follows: B Version: −40°C to +85°C.
[2] See the Terminology section.
[3] Linearity is tested using a reduced code range: Codes 32 to 1023.
[4] To achieve near zero output current, use the power-down feature.
[5] Guaranteed by design and characterization; not production tested.
[6] Input filtering on both the SCL and SDA inputs suppresses noise spikes that are less than 50 ns.

AC SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, AGND = DGND = 0 V, load resistance R_L = 25 Ω connected to V_{DD}, unless otherwise noted.

Table 2.

Parameter	B Version[1, 2] Min	Typ	Max	Unit	Test Conditions/Comments
Output Current Settling Time		250		µs	V_{DD} = 5 V, R_L = 25 Ω, L_L = 680 µH ¼ scale to ¾ scale change (0x100 to 0x300)
Slew Rate		0.3		mA/µs	
Major Code Change Glitch Impulse		0.15		nA-s	1 LSB change around major carry
Digital Feedthrough[3]		0.06		nA-s	

[1] Temperature range is as follows: B Version: –40°C to +85°C.
[2] Guaranteed by design and characterization; not production tested.
[3] See the Terminology section.

TIMING SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1]	B Version Limit at T_{MIN}, T_{MAX}	Unit	Test Conditions/Comments
f_{SCL}	400	kHz max	SCL clock frequency
t_1	2.5	µs min	SCL cycle time
t_2	0.6	µs min	t_{HIGH}, SCL high time
t_3	1.3	µs min	t_{LOW}, SCL low time
t_4	0.6	µs min	$t_{HD, STA}$, start/repeated start condition hold time
t_5	100	ns min	$t_{SU, DAT}$, data setup time
t_6[2]	0.9	µs max	$t_{HD, DAT}$, data hold time
	0	µs min	
t_7	0.6	µs min	$t_{SU, STA}$, setup time for repeated start
t_8	0.6	µs min	$t_{SU, STO}$, stop condition setup time
t_9	1.3	µs min	t_{BUF}, bus free time between a stop condition and a start condition
t_{10}	300	ns max	t_R, rise time of both SCL and SDA when receiving
	0	ns min	May be CMOS driven
t_{11}	250	ns max	t_F, fall time of SDA when receiving
	300	ns max	t_F, fall time of both SCL and SDA when transmitting
	20 + 0.1 C_b[3]	ns min	
C_b	400	pF max	Capacitive load for each bus line

[1] Guaranteed by design and characterization; not production tested.
[2] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH\ MIN}$ of the SCL signal) in order to bridge the undefined region of SCL falling edge.
[3] C_b is the total capacitance of one bus line in pF. t_R and t_F are measured between 0.3 V_{DD} and 0.7 V_{DD}.

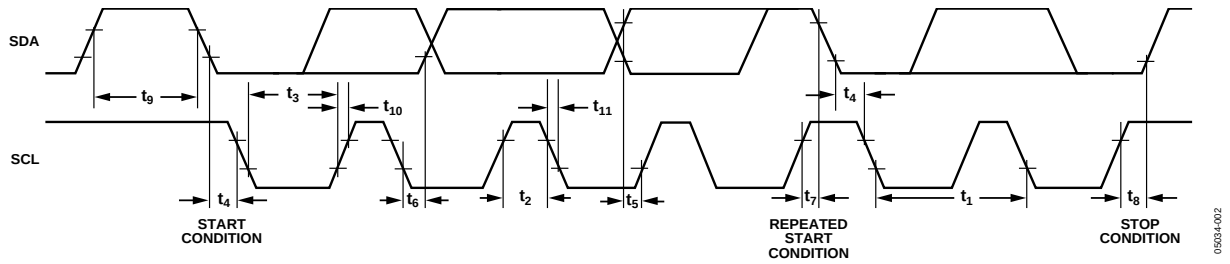

Figure 2. 2-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.[1]

Table 4.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +7 V
V_{DD} to DGND	−0.3 V to V_{DD} + 0.3 V
AGND to DGND	−0.3 V to +0.3 V
SCL, SDA to DGND	−0.3 V to V_{DD} + 0.3 V
PD to DGND	−0.3 V to V_{DD} + 0.3 V
I_{SINK} to AGND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
LFCSP Power Dissipation	(T_J max − T_A)/θ_{JA}
θ_{JA} Thermal Impedance[2]	
Mounted on 2-Layer Board	84°C/W
Mounted on 4-Layer Board	48°C/W
Lead Temperature, Soldering	
Max Peak Reflow Temperature[3]	260°C (±5°C)

[1] Transient currents of up to 100 mA do not cause SCR latch-up.
[2] To achieve the optimum θ_{JA}, it is recommended that the AD5398 is soldered on a 4-layer board. The AD5398 comes in an 8-lead LFCSP package with an exposed paddle that must be connected to the same potential as the AD5398 DGND pin.
[3] As per JEDEC J-STD-020C.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

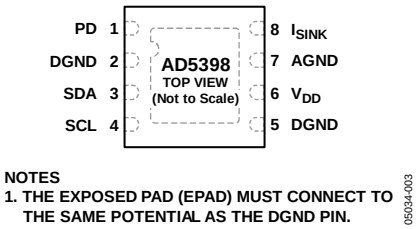

Figure 3. 8-Lead LFSCP Pin Configuration

Table 5. 8-Lead LFSCP Pin Function Description

Pin No.	Mnemonic	Description
1	PD	Power Down. Asynchronous power-down signal.
2	DGND	Digital Ground Pin.
3	SDA	I^2C Interface Signal.
4	SCL	I^2C Interface Signal.
5	DGND	Digital Ground Pin.
6	V_{DD}	Digital Supply Voltage.
7	AGND	Analog Ground Pin.
8	I_{SINK}	Output Current Sink.
	EPAD	Exposed Pad. The exposed pad (EPAD) must connect to the same potential as the DGND pin.

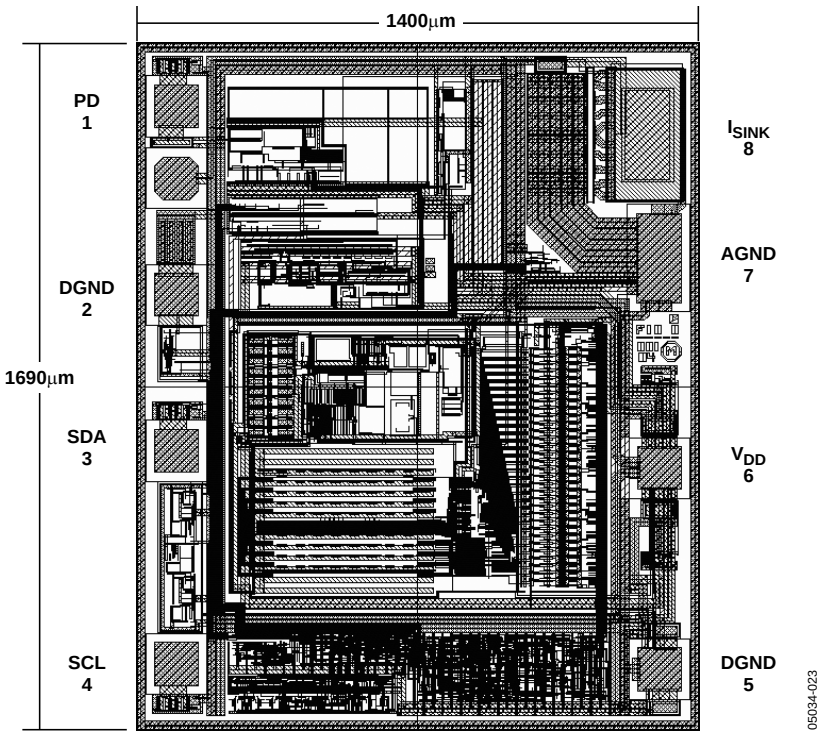

Figure 4. Metallization Photograph
Dimensions shown in µm
Contact Factory for Latest Dimensions

TYPICAL PERFORMANCE CHARACTERISTICS

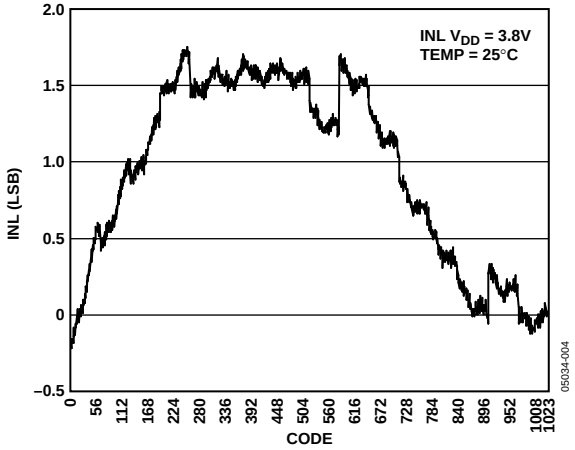

Figure 5. Typical INL Plot

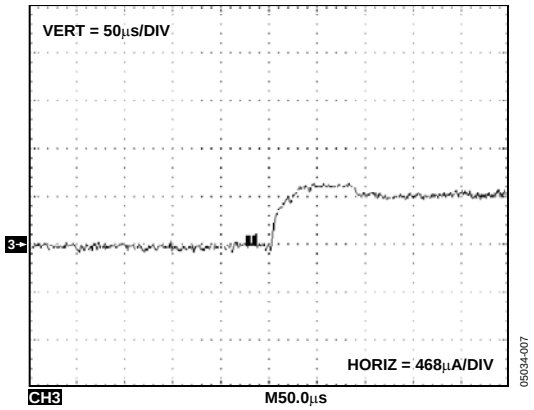

Figure 8. Settling Time for a 4-LSB Step (VDD = 3.6 V)

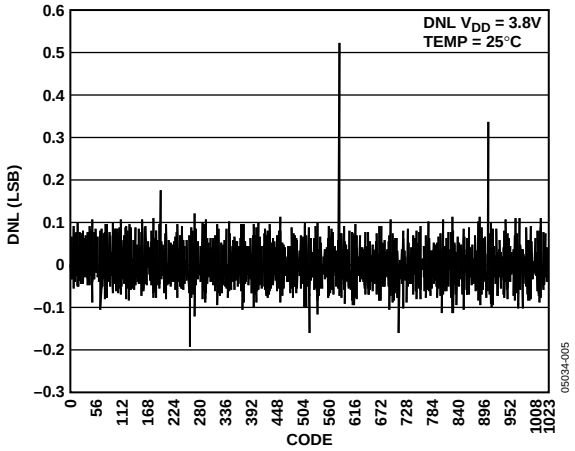

Figure 6. Typical DNL Plot

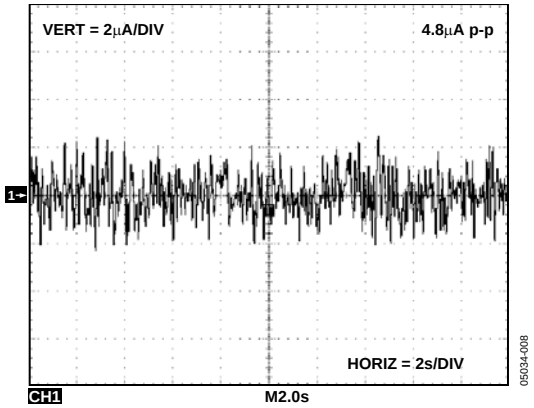

Figure 9. 0.1 Hz to 10 Hz Noise Plot (VDD = 3.6 V)

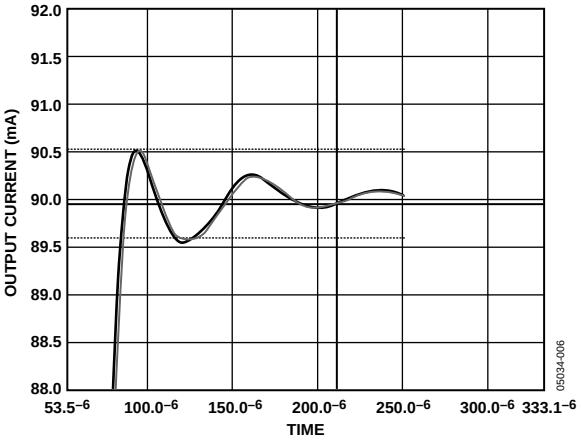

Figure 7. ¼ to ¾ Scale Settling Time (VDD = 3.6 V)

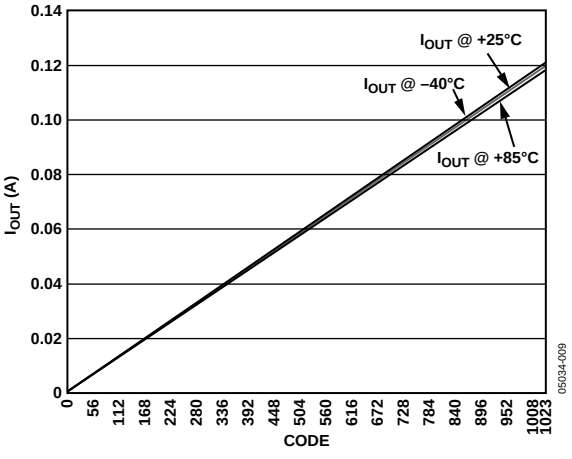

Figure 10. Sink Current vs. Code vs. Temperature (VDD = 3.6 V)

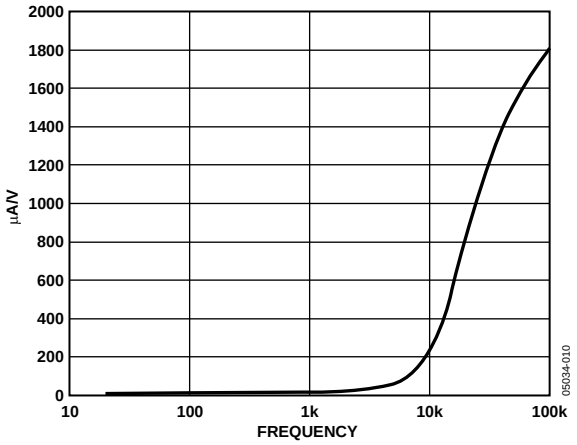

Figure 11. AC Power Supply Rejection (VDD = 3.6 V)

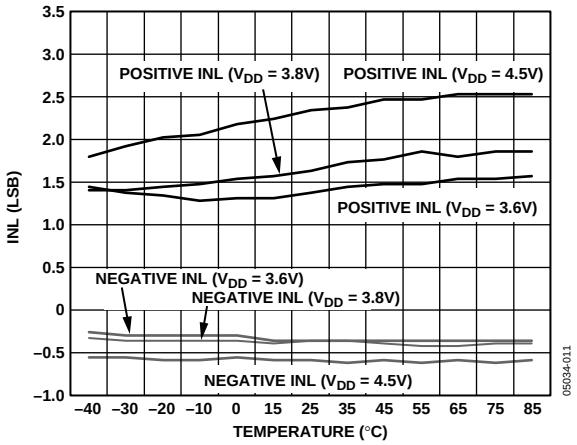

Figure 12. INL vs. Temperature vs. Supply

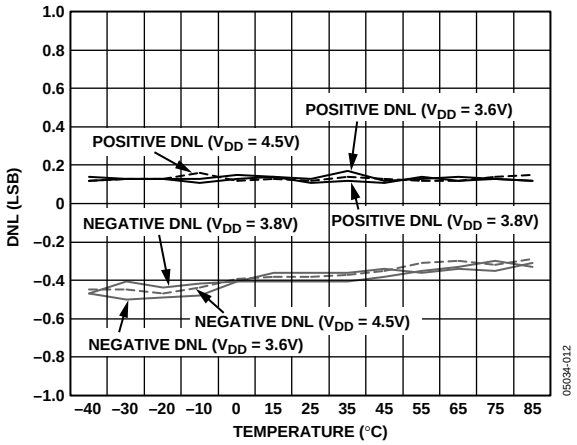

Figure 13. DNL vs. Temperature vs. Supply

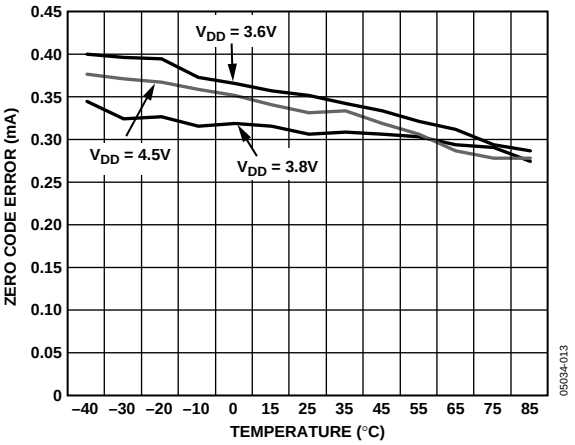

Figure 14. Zero Code Error vs. Supply Voltage vs. Temperature

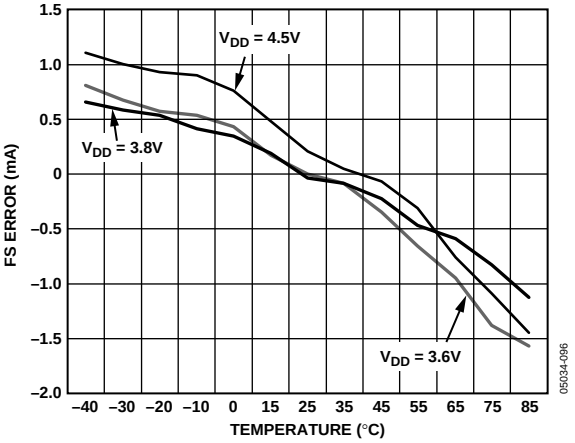

Figure 15. Full-Scale Error vs. Temperature vs. Supply

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSB, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot is shown in Figure 5.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot is shown in Figure 6.

Zero-Code Error
Zero-code error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output is 0 mA. The zero-code error is always positive in the AD5398 because the output of the DAC cannot go below 0 mA. This is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in mA.

Gain Error
This is a measurement of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percent of the full-scale range.

Gain Error Drift
This is a measurement of the change in gain error with changes in temperature. It is expressed in LSB/°C.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nA-s and is measured when the digital input code is changed by 1 LSB at the major carry transition.

Digital Feedthrough
Digital feedthrough is a measurement of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nA-s and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Offset Error
Offset error is a measurement of the difference between I_{SINK} (actual) and I_{OUT} (ideal) in the linear region of the transfer function, expressed in mA. Offset error is measured on the AD5398 with Code 16 loaded into the DAC register.

Offset Error Drift
This is a measurement of the change in offset error with a change in temperature. It is expressed in μV/°C.

THEORY OF OPERATION

The AD5398 is a fully integrated 10-bit DAC with 120 mA output current sink capability and is intended for driving voice coil actuators in applications such as lens autofocus, image stabilization, and optical zoom. The circuit diagram is shown in Figure 16. A 10-bit current output DAC coupled with Resistor R generates the voltage that drives the noninverting input of the operational amplifier. This voltage also appears across the R_{SENSE} resistor and generates the sink current required to drive the voice coil.

Resistors R and R_{SENSE} are interleaved and matched. Therefore, the temperature coefficient and any nonlinearities over temperature are matched and the output drift over temperature is minimized. Diode D1 is an output protection diode.

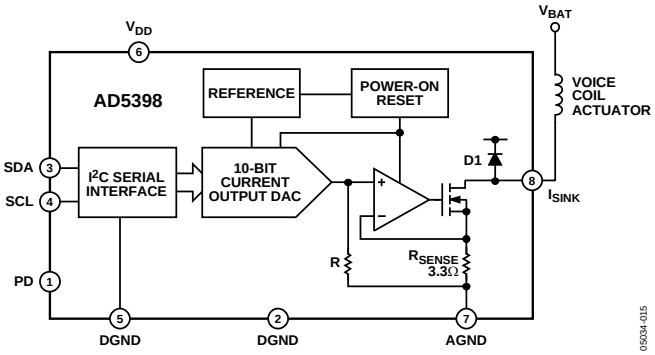

Figure 16. Block Diagram Showing Connection to Voice Coil

SERIAL INTERFACE

The AD5398 is controlled using the industry-standard I²C 2-wire serial protocol. Data can be written to or read from the DAC at data rates up to 400 kHz. After a read operation, the contents of the input register are reset to all zeros.

I²C BUS OPERATION

An I²C bus operates with one or more master devices that generate the serial clock (SCL), and read/write data on the serial data line (SDA) to/from slave devices such as the AD5398. All devices on an I²C bus have their SCL pin connected to the SDA line and their SCL pin connected to the SCL line. I²C devices can only pull the bus lines low; pulling high is achieved by pull-up resistors R_P. The value of R_P depends on the data rate, bus capacitance, and the maximum load current that the I²C device can sink (3 mA for a standard device).

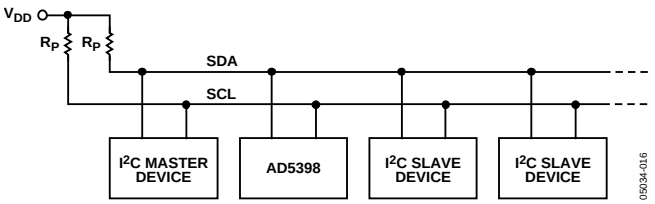

Figure 17. Typical I²C Bus

When the bus is idle, SCL and SDA are both high. The master device initiates a serial bus operation by generating a start condition, which is defined as a high-to-low transition on the SDA low while SCL is high. The slave device connected to the bus responds to the start condition and shifts in the next eight data bits under control of the serial clock. These eight data bits consist of a 7-bit address, plus a read/write bit, which is 0 if data is to be written to a device, and 1 if data is to be read from a device. Each slave device on an I²C bus must have a unique address. The address of the AD5398 is 0001100; however, 0001101, 0001110, and 0001111 address the device because the last two bits are unused/don't care (see Figure 18 and Figure 19). Since the address plus R/W bit always equals eight bits of data, another way of looking at it is that the write address of the AD5398 is 0001 1000 (0x18) and the read address is 0001 1001 (0x19). Again, Bit 6 and Bit 7 of the address are unused, and therefore the write addresses can also be 0x1A, 0x1C, and 0x1E, and the read address can be 0x1B, 0x1D, and 0x1F (see Figure 18 and Figure 19).

At the end of the address data, after the R/W bit, the slave device that recognizes the address responds by generating an acknowledge (ACK) condition. This is defined as the slave device pulling SDA low while SCL is low before the ninth clock pulse, and keeping it low during the ninth clock pulse. Upon receiving ACK, the master device can clock data into the AD5398 in a write operation, or it can clock it out in a read operation. Data must change either during the low period of the clock, because SDA transitions during the high period define a start condition as described previously, or during a stop condition as described in the Data Format section.

I²C data is divided into blocks of eight bits, and the slave generates an ACK at the end of each block. Since the AD5398 requires 10 bits of data, two data-words must be written to it when a write operation occurs, or read from it when a read operation occurs. At the end of a read or write operation, the AD5398 acknowledges the second data byte. The master generates a stop condition, defined as a low-to-high transition on SDA while SCL is high, to end the transaction.

DATA FORMAT

Data is written to the AD5398 high byte first, MSB first, and is shifted into the 16-bit input register. After all data is shifted in, data from the input register is transferred to the DAC register.

Because the DAC requires only 10 bits of data, not all bits of the input register data are used. The MSB is reserved for an active-high, software-controlled, power-down function. Bit 14 is unused; Bit 13 to Bit 4 correspond to the DAC data bits, Bit 9 to Bit 0. Bit 3 to Bit 0 are unused.

During a read operation, data is read in the same bit order.

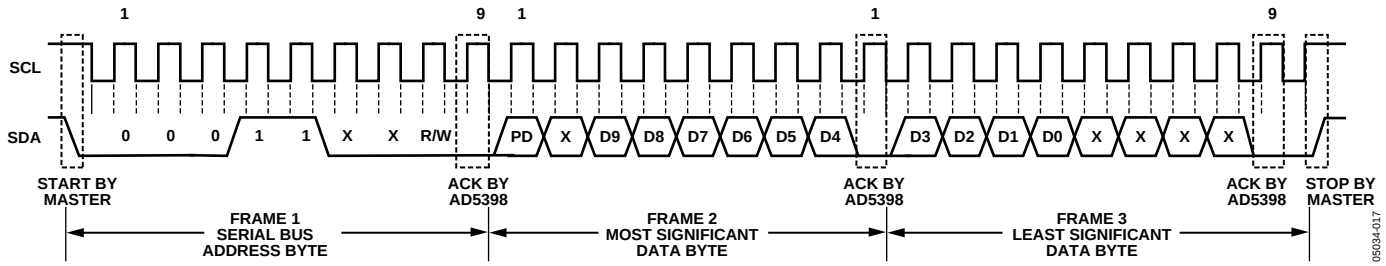

Figure 18. Write Operation

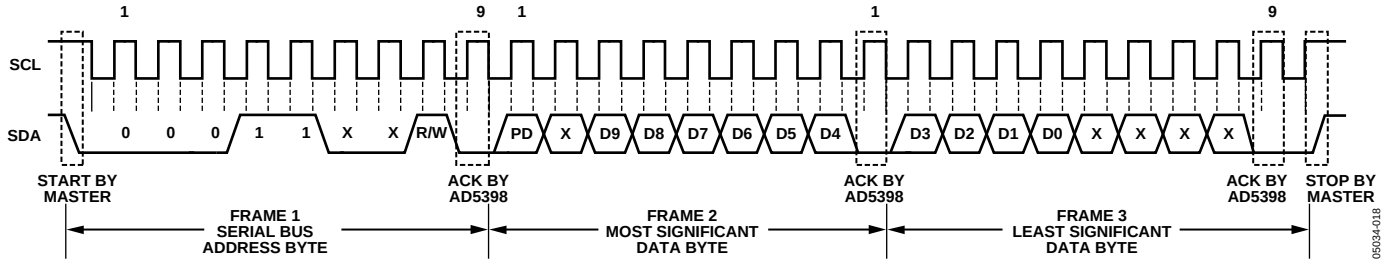

Figure 19. Read Operation

Table 6. Data Format[1]

Serial Data-Words	High Byte								Low Byte							
Serial Data Bits	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Input Register	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
Function	PD	X	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X

[1] PD = soft power-down; X = unused/don't care; D9 to D0 = DAC data.

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in an application, it is beneficial to consider power supply and ground return layout on the printed circuit board (PCB). The PCB for the AD5398 must have separate analog and digital power supply sections. Where shared AGND and DGND is necessary, the connection of grounds must be made at only one point, as close as possible to the AD5398.

Special attention must be paid to the layout of the AGND return path and track between the voice coil motor and I_{SINK} to minimize any series resistance. Figure 20 shows the output current sink of the AD5398 and illustrates the importance of reducing the effective series impedance of AGND, and the track resistance between the motor and I_{SINK}. The voice coil is modelled as inductor L_C and resistor R_C. The current through the voice coil is effectively a dc current that results in a voltage drop, V_C, when the AD5398 is sinking current; the effect of any series inductance is minimal. The maximum voltage drop allowed across R_{SENSE} is 400 mV, and the minimum drain to source voltage of Q1 is 200 mV. This means that the AD5398 output has a compliance voltage of 600 mV. If V_{DROP} falls below 600 mV, the output transistor, Q1, can no longer operate properly and I_{SINK} might not be maintained as a constant.

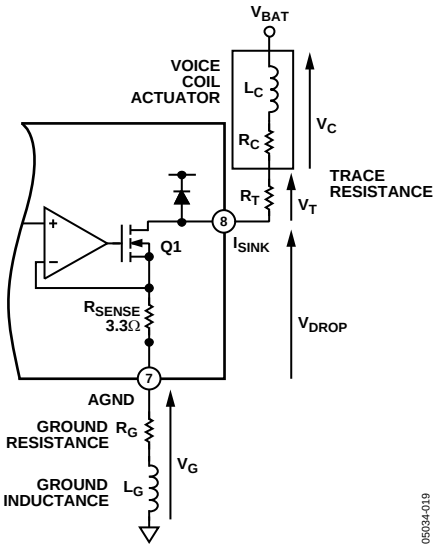

Figure 20. Effect of PCB Trace Resistance and Inductance

As the current increases through the voice coil, V_C increases and V_{DROP} decreases and eventually approaches the minimum specified compliance voltage of 600 mV. The ground return path is modelled by the components RG and LG. The track resistance between the voice coil and the AD5398 is modelled as R_T. The inductive effects of L_G influence R_{SENSE} and R_C equally, and because the current is maintained as a constant, it is not as critical as the purely resistive component of the ground return path.

When the maximum sink current is flowing through the motor, the resistive elements, R_T and R_G, might have an impact on the voltage headroom of Q1 and could, in turn, limit the maximum value of R_C because of voltage compliance.

For example:

V_{BAT} = 3.6 V

R_G = 0.5 Ω

R_T = 0.5 Ω

I_{SINK} = 120 mA

V_{DROP} = 600 mV (the compliance voltage)

Then the largest value of resistance of the voice coil, R_C, is

$$R_C = \frac{V_{BAT} - [V_{DROP} + (I_{SINK} \times R_T) + (I_{SINK} \times R_G)]}{I_{SINK}} =$$

$$\frac{3.6\text{ V} - [600\text{ mV} + 2 \times (120\text{ mA} \times 0.5\ \Omega)]}{120\text{ mA}} = 24\ \Omega$$

For this reason it is important to minimize any series impedance on both the ground return path and interconnect between the AD5398 and the motor.

The power supply of the AD5398 must be decoupled with 0.1 µF and 10 µF capacitors. These capacitors must be kept as physically close as possible, with the 0.1 µF capacitor serving as a local bypass capacitor, and therefore must be located as close as possible to the V_{DD} pin. The 10 µF capacitor must be a tantalum bead-type; the 0.1 µF capacitor must be a ceramic type with a low effective series resistance and effective series inductance. The 0.1 µF capacitor provides a low impedance path to ground for high transient currents.

The power supply line must have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals must be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is to use a multilayer board with ground and power planes, where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

The exposed paddle on the AD5398 must be soldered to ground to ensure the best possible thermal performance. The thermal impedance of the AD5398 LFCSP package is 48°C/W when soldered in a 4-layer board. It is defined in the Absolute Maximum Ratings section.

APPLICATIONS INFORMATION

The AD5398 is designed to drive both spring preloaded and nonspring linear motors used in applications such as lens autofocus, image stabilization, or optical zoom. The operation principle of the spring-preloaded motor is that the lens position is controlled by the balancing of a voice coil and spring. Figure 21 shows the transfer curve of a typical spring preloaded linear motor for autofocus. The key points of this transfer function are displacement or stroke, which is the actual distance the lens moves in mm, and the current through the motor in mA.

A start current is associated with spring-preloaded linear motors, which is effectively a threshold current that must be exceeded for any displacement in the lens to occur. The start current is usually 20 mA or greater; the rated stroke or displacement is usually 0.25 mm to 0.4 mm; and the slope of the transfer curve is approximately 10 µm/mA or less.

The AD5398 is designed to sink up to 120 mA, which is more than adequate for available commercial linear motors or voice coils. Another factor that makes the AD5398 the ideal solution for these applications is the monotonicity of the device, which ensures that lens positioning is repeatable for the application of a given digital word.

Figure 22 shows a typical application circuit for the AD5398.

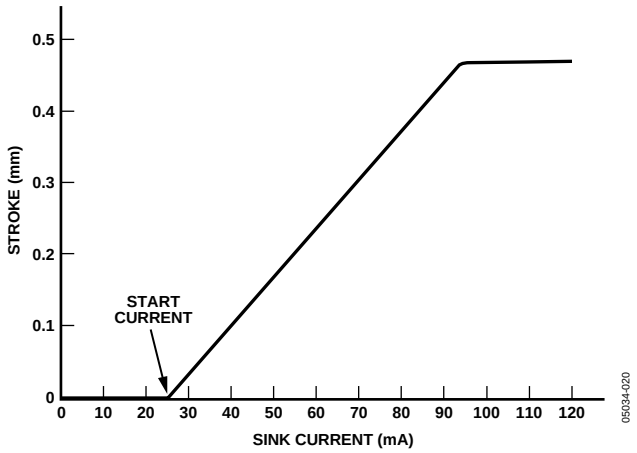

Figure 21. Spring Preloaded Voice Coil Stroke vs. Sink Current

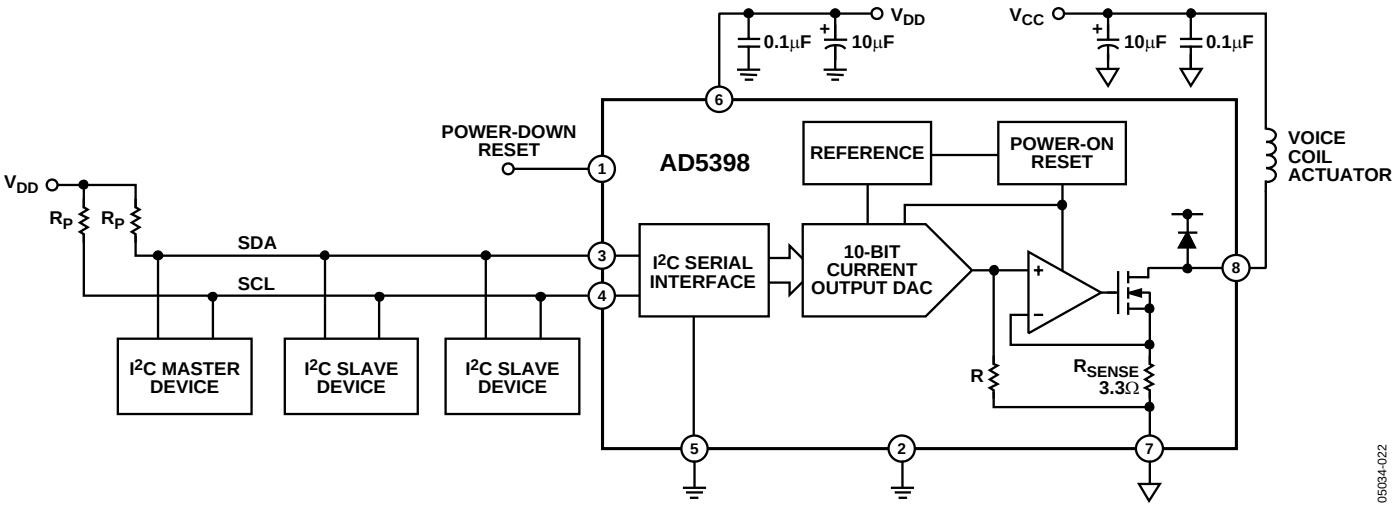

Figure 22. Typical Application Circuit

OUTLINE DIMENSIONS

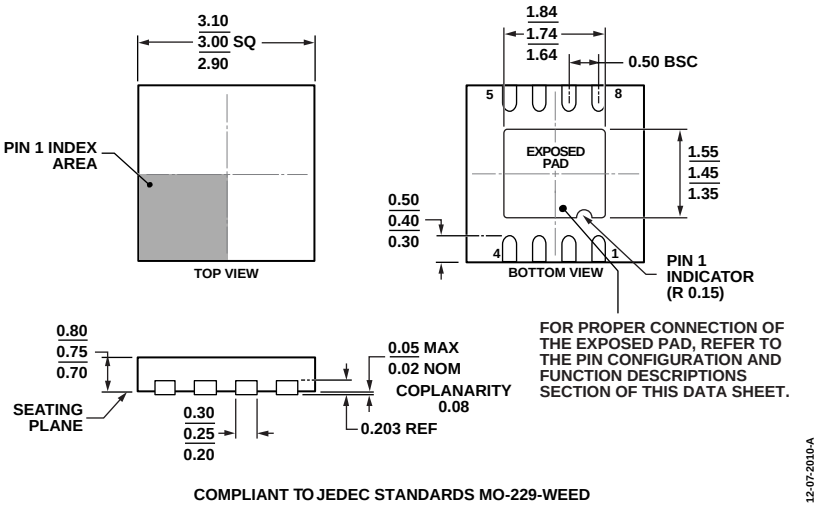

Figure 23. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD5398BCPZ-REEL	–40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-13
AD5398BCPZ-REEL7	–40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-13

[1] Z = RoHS Compliant Part.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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