

June 1998 Revised February 2001

74LCX112

Low Voltage Dual J-K Negative Edge-Triggered Flip-Flop with 5V Tolerant Inputs

General Description

The LCX112 is a dual J-K flip-flop. Each flip-flop has independent J, K, PRESET, CLEAR, and CLOCK inputs with Q, Q outputs. These devices are edge sensitive and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input. LCX devices are designed for low voltage (3.3V or 2.5) operation with the added capability of interfacing to a 5V signal environment.

The 74LCX112 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- 2.3V-3.6V V_{CC} specifications provided
- \blacksquare 7.5 ns t_{PD} max (V $_{CC}$ = 3.3V), 10 μA I_{CC} max
- Power down high impedance inputs and outputs
- \blacksquare ±24 mA output drive (V_{CC} = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:

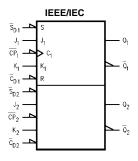
Human body model > 2000V Machine model > 2000V

Ordering Code:

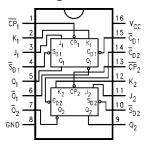
Order Number	Package Number	Package Description
74LCX112M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74LCX112SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX112MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
J ₁ , J ₂ , K ₁ , K ₂	Data Inputs
$\overline{CP}_1, \overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)
\overline{C}_{D1} , \overline{C}_{D2}	Direct Clear Inputs (Active LOW)
\overline{S}_{D1} , \overline{S}_{D2}	Direct Set Inputs (Active LOW)
$Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$	Outputs

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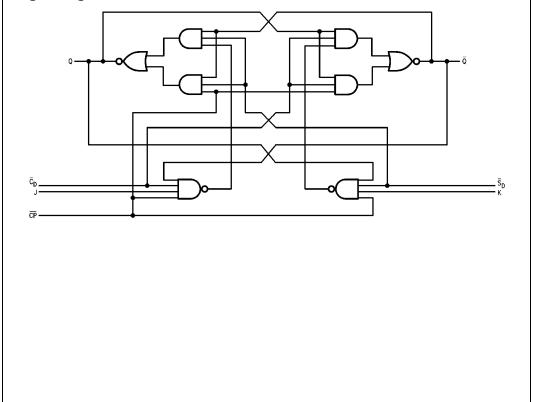
Truth Table

(Each half)

		Out	puts			
S _D		СР	J	К	Q	lα
L	Н	Х	Х	Х	Н	L
Н	L	Х	Х	Х	L	Н
L	L	Х	Х	Х	Н	Τ
Н	Н	7	h	h	\overline{Q}_{O}	Qo
Н	Н	/	I	h	L	Τ
Н	Н	7	h	- 1	Н	L
Н	Н	7	I	- 1	Q_O	\overline{Q}_{O}
Н	Н	Н	Х	Х	QO	Qo

H(h) = HIGH Voltage Level
L(l) = LOW Voltage Level
X = Immaterial
= HIGH-to-LOW Clock Transition
Q_O(\overline{O}_0) = Before HIGH-to-LOW Transition of Clock
Lower case letters indicate the state of the referenced input or output one setup time prior to the HIGH-to-LOW clock transition.

Logic Diagram



Absolute Maximum Ratings(Note 1) Parameter Units Symbol Value Conditions ٧ Supply Voltage -0.5 to +7.0 V_{CC} V V_{I} DC Input Voltage -0.5 to +7.0 Output in HIGH or LOW State (Note 2) ٧o DC Output Voltage -0.5 to $V_{CC} + 0.5$ V V_I < GND DC Input Diode Current -50 mΑ DC Output Diode Current V_O < GND I_{OK} mΑ +50 $V_O > V_{CC}$ ±50 DC Output Source/Sink Current mΑ ±100 DC Supple Current per Supply Pin mΑ DC Ground Current per Ground Pin ±100 I_{GND} mΑ Storage Temperature °C T_{STG} -65 to 150

Recommended Operating Conditions (Note 3)

Symbol	Parameter			Max	Units
V _{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	V
V _I	Input Voltage		0	5.5	V
Vo	Output Voltage	HIGH or LOW State	0	V _{CC}	V
I _{OH} /I _{OL}	Output Current	$V_{CC} = 3.0V - 3.6V$		±24	
		$V_{CC} = 2.7V - 3.0V$		±12	mA
		$V_{CC} = 2.3V - 2.7V$		±8	
T _A	Free-Air Operating Temperature		-40	85	°C
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V–2.0V, V _{CC} = 3.0V		0	10	ns/V

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum rating must be observed.

Note 3: Unused Inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC}	T _A = 40°C	$T_A = 40^{\circ}C \text{ to } +85^{\circ}C$	
Symbol		Conditions	(V)	Min	Max	Units
V _{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		V
V _{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	V
V _{OH}	HIGH Level Output Voltage	$I_{OH} = -100\mu A$	2.3 – 3.6	V _{CC} - 0.2	0.7	
		I _{OH} = -8 mA	2.3	1.8		1
		$I_{OH} = -12 \text{ mA}$	2.7	2.2		V
		$I_{OH} = -18 \text{ mA}$	3.0	2.4		1
		$I_{OH} = -24 \text{ mA}$	3.0	2.2		1
V _{OL}	LOW Level Output Voltage	I _{OL} = 100μA	2.3 – 3.6		0.6	
		I _{OL} = 8mA	2.3		0.2	1
		I _{OL} = 12 mA	2.7		0.4	V
		I _{OL} = 16 mA	3.0		0.4	1
		I _{OL} = 24 mA	3.0		0.55	1
I _I	Input Leakage Current	$0 \le I_1 \le 5.5V$	2.3 – 3.6		±5.0	μΑ
l _{OFF}	Power-Off Leakage Current	V_I or $V_O = 5.5V$	0		10	μΑ
Icc	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 – 3.6		10	μΑ
		$3.6 \text{V} \leq \text{V}_{\text{I}} \leq 5.5 \text{V}$	2.3 – 3.6		±10	μΑ
Δl _{CC}	Increase in I _{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.3 - 3.6		500	μΑ

AC Electrical Characteristics

		$T_A = 40^{\circ}\text{C}$ to 85°C , $R_L = 500\Omega$						
Symbol	Parameters	$\textrm{V}_{\textrm{CC}}=\textrm{3.3V}\pm\textrm{0.3V}$		$V_{CC} = 2.7V$		$\textrm{V}_{\textrm{CC}}{}_{=}\textrm{2.5V}\pm\textrm{0.2V}$		Units
	Parameters	C _L =	C _L =50 pF		C _L = 50 pF		C _L =30 pF	
		Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	150		150		150		MHz
t _{PHL}	Propagation Delay	1.5	7.5	1.5	8.0	1.5	9.0	
t _{PLH}	\overline{CP}_n to Q_n or \overline{Q}_n	1.5	7.5	1.5	8.0	1.5	9.0	ns
t _{PHL}	Propagation Delay	1.5	7.0	1.5	8.0	1.5	8.4	
t _{PLH}	\overline{C}_{Dn} or \overline{S}_{Dn} to Q_n or \overline{Q}_n	1.5	7.0	1.7	8.0	1.5	8.4	ns
t _S	Setup Time	2.5		2.5		4.0		ns
t _H	Hold Time	1.5		1.5		2.0		ns
t _W	Pulse Width CP	3.3		3.3		4.0		ns
t _W	Pulse Width $(\overline{C}_D, \overline{S}_D)$	3.3		3.3		4.0		ns
t _{REC}	Recovery Time	2.0		2.5		4.5		ns
t _{OSHL}	Output to Output Skew		1.0					
t _{OSLH}	(Note 4)		1.0					ns

Note 4: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}), or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C	Units
Symbol	Faiametei	Conditions	(V)	Typical	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$	3.3	0.8	V
		$C_L = 30 \text{ pF}, V_{IH} = 2.5 \text{V}, V_{IL} = 0 \text{V}$	2.5	0.6	V
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$	3.3	-0.8	V
		$C_L = 30 \text{ pF}, V_{IH} = 2.5 \text{V}, V_{IL} = 0 \text{V}$	2.5	-0.6	V

Capacitance

Symbol Parameter		Conditions	Typical	Units
C _{IN}	Input Capacitance	$V_{CC} = Open, V_I = 0V \text{ or } V_{CC}$	7	pF
C _{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC} , $f = 10$ MHz	25	pF

AC Loading and Waveforms Generic for LCX Family

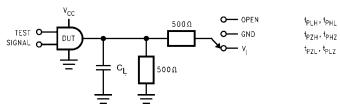
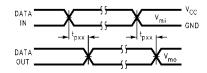
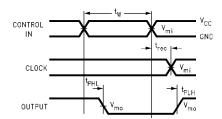


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

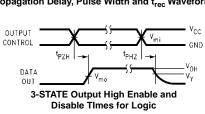
Test	Switch
t _{PLH} , t _{PHL}	Open
t _{PZL} , t _{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$ V_{CC} x 2 at $V_{CC} = 2.5 \pm 0.2V$
t _{PZH} ,t _{PHZ}	GND

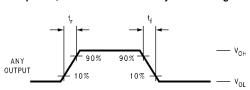


Waveform for Inverting and Non-Inverting Functions



Propagation Delay, Pulse Width and $t_{\rm rec}$ Waveforms

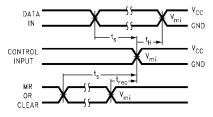




Symbol	V _{cc}				
- Cymbon	$3.3V \pm 0.3V$	2.7V	2.5V ± 0.2V		
V _{mi}	1.5V	1.5V	V _{CC} /2		
V_{mo}	1.5V	1.5V	V _{CC} /2		
V _x	V _{OL} + 0.3V	V _{OL} + 0.3V	V _{OL} + 0.15V		
V _y	V _{OH} – 0.3V	V _{OH} – 0.3V	V _{OH} – 0.15V		

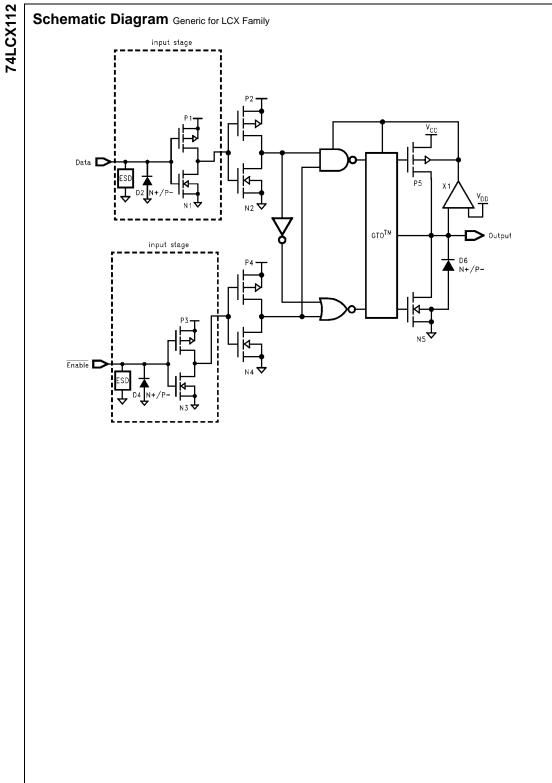
OUTPUT CONTROL DATA OUT

3-STATE Output Low Enable and **Disable Times for Logic**



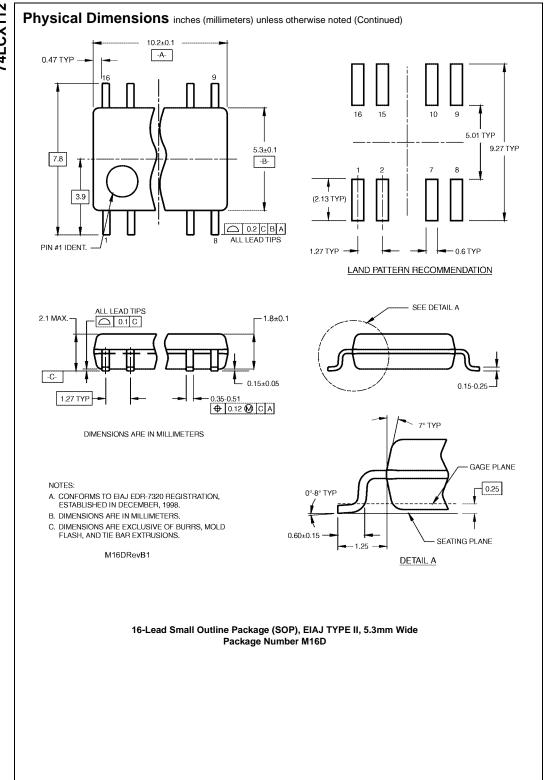
Setup Time, Hold Time and Recovery Time for Logic

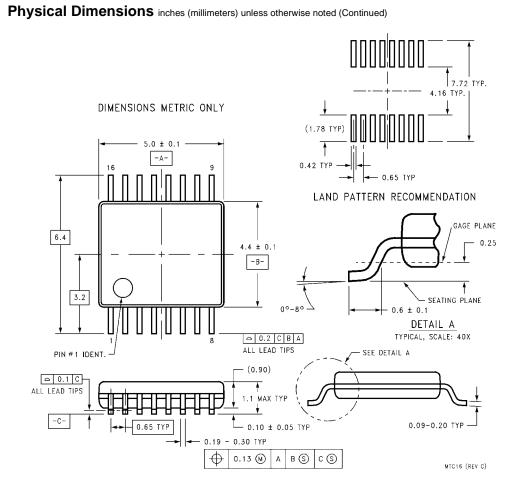
Symbol	65					
Oybo.	3.3V \pm 0.3V	2.7V	2.5V ± 0.2V			
V_{mi}	1.5V	1.5V	V _{CC} /2			
V_{mo}	1.5V	1.5V	V _{CC} /2			
V _x	V _{OL} + 0.3V	V _{OL} + 0.3V	V _{OL} + 0.15V			
V _v	V _{OH} – 0.3V	V _{OH} – 0.3V	V _{OH} – 0.15V			



Physical Dimensions inches (millimeters) unless otherwise noted $\frac{0.386-0.394}{(9.804-10.00)}$ 13 Ĥ 12 11 A A $\frac{0.228 - 0.244}{(5.791 - 6.198)}$ LEAD NO.1 $\frac{0.150 - 0.157}{(3.810 - 3.988)}$ $\frac{0.053 - 0.069}{(1.346 - 1.753)}$ $\frac{0.010 - 0.020}{(0.254 - 0.508)}$ $\frac{0.004 - 0.010}{(0.102 - 0.254)}$ 8° MAX TYP ALL LEADS SEATING PLANE 0.014 (0.356) 0.008 - 0.010 (0.203 - 0.254) TYP ALL LEADS 0.050 (1.270) TYP - 0.014 - 0.020 TYP (0.356 - 0.508) 0.016 - 0.050 (0.406 - 1.270) TYP ALL LEADS 0.004 (0.102) All Lead TIPS 0.008 (0.203) TYP M16A (REV H) 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A







16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC16

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