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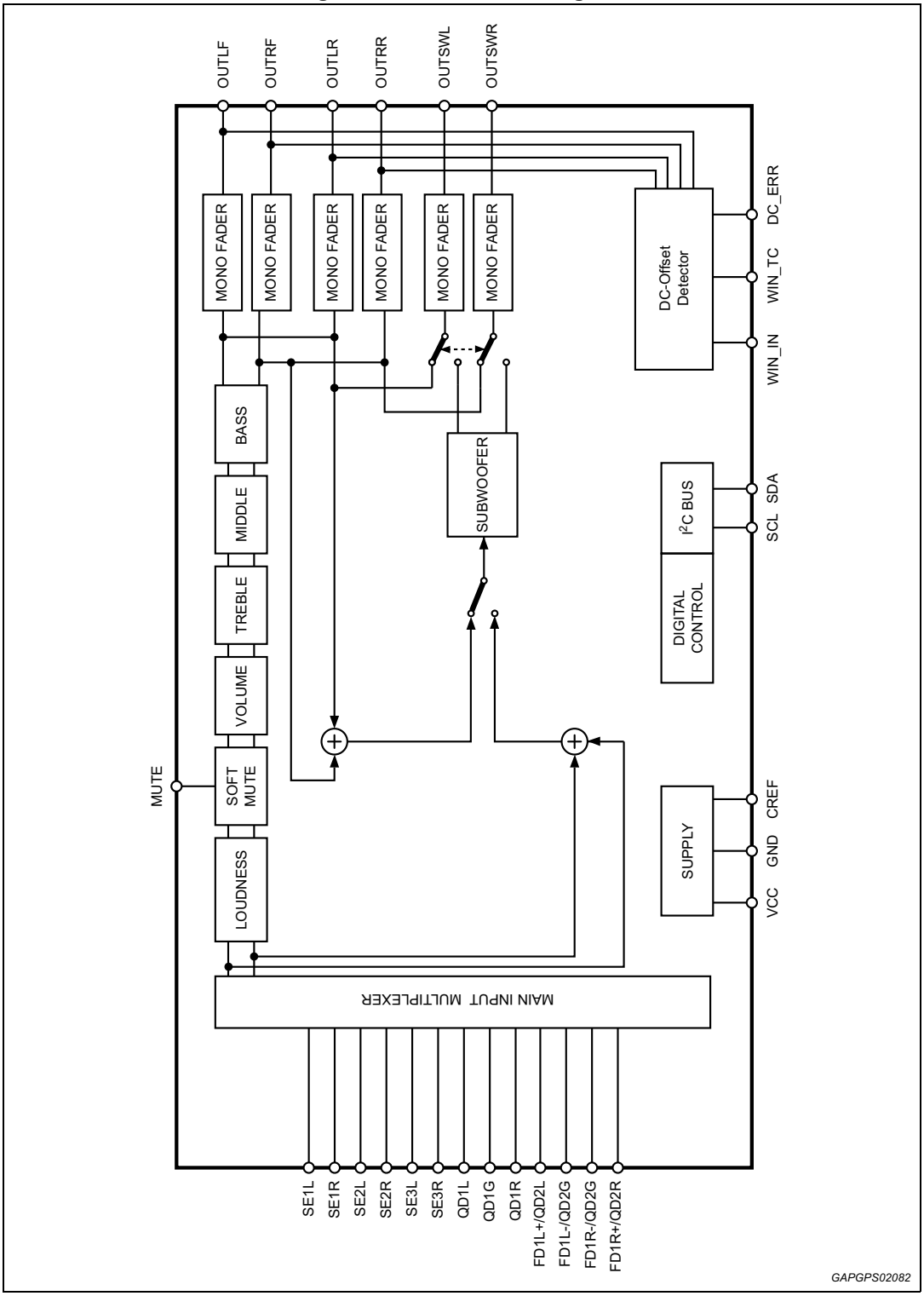
1 Block circuit diagram

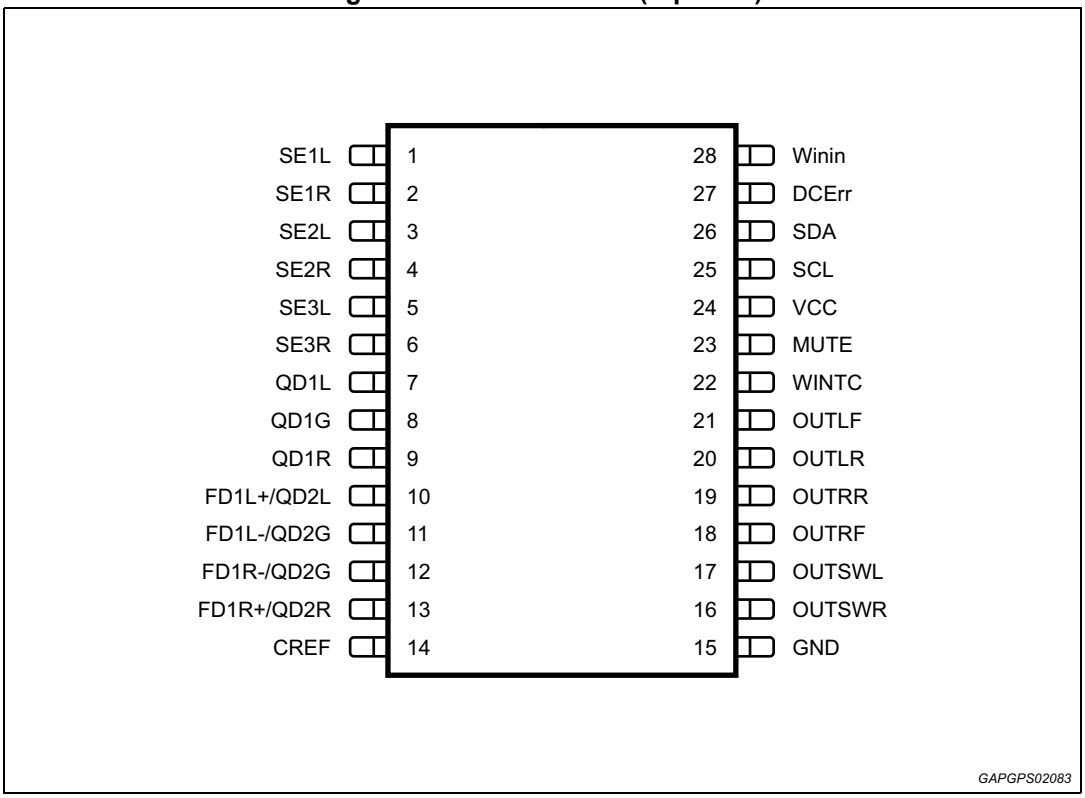
Figure 1. Block circuit diagram



2 Pin connection and pin description

2.1 Pin connection

Figure 2. Pin connection (top view)



2.2 Pin description

Table 2. Pin description

No.	Pin name	Description	I/O
1	SE1L	Single-end input left	I
2	SE1R	Single-end input right	I
3	SE2L	Single-end input left	I
4	SE2R	Single-end input right	I
5	SE3L	Single-end input left	I
6	SE3R	Single-end input right	I
7	QD1L	quasi-differential stereo inputs left	I
8	QD1G	quasi-differential stereo inputs common	I
9	QD1R	quasi-differential stereo inputs right	I
10	FD1L+/QD2L	Full differential + input left or quasi-differential left	I

Table 2. Pin description (continued)

No.	Pin name	Description	I/O
11	FD1L-/QD2G	Full differential - input left or quasi-differential ground	I
12	FD1R-/QD2G	Full differential - input right or quasi-differential ground	I
13	FD1R+/QD2R	Full differential + input right or quasi-differential right	I
14	CREF	Reference capacitor	O
15	GND	Ground	S
16	OUTSWR	Subwoofer right output	O
17	OUTSWL	Subwoofer left output	O
18	OUTRF	Front right output	O
19	OUTRR	Rear right output	O
20	OUTLR	Rear left output	O
21	OUTLF	Front left output	O
22	WinTC	DC offset detector filter output	O
23	MUTE	External mute pin	I
24	VCC	Supply	S
25	SCL	I^2C bus clock	I
26	SDA	I^2C bus data	I/O
27	DC_ERR	DC offset detector output	O
28	WIN_IN	DC offset detector input	I

Note: The L & R channels may be swapped as per the user's wishes making use of proper connections to the device pins, with no impact on electrical performance. Software control has to take into account the external routing and be designed accordingly.

3 Electrical specifications

3.1 Thermal data

Table 3. Thermal data

Symbol	Description	Value	Unit
$R_{th\text{-}j\ amb}$	Thermal resistance junction-to-ambient	114	°C/W

3.2 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Operating supply voltage	10.5	V
V_{in_max}	Maximum voltage for signal input pins	7	V
T_{amb}	Operating ambient temperature	-40 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

3.3 Electrical characteristics

V_S = 8.5 V; T_{amb}= 25 °C; R_L= 10 kΩ; all gains = 0 dB; f = 1 kHz; unless otherwise specified

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply						
V_s	Supply voltage	-	7.5	8.5	10	V
I_s	Supply current	-	23	29	35	mA
Input selector						
R_{in}	Input resistance	All single ended inputs	70	100	130	kΩ
V_{CL}	Clipping level	Input gain = 0 dB	2	-	-	V_{RMS}
S_{IN}	Input separation	-	-	95	-	dB
Differential stereo inputs						
R_{in}	Input resistance	Differential	70	100	-	kΩ
CMRR	Common mode rejection ratio for main source	V_{CM} = 1 V_{RMS} @ 1 kHz	44	60	-	dB
		V_{CM} = 1 V_{RMS} @ 10 kHz	44	60	-	dB
e_{No}	Output noise @ speaker outputs	20 Hz - 20 kHz, A-weighted; all stages 0 dB	-	12	22	µV

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Loudness control						
A_{MAX}	Max attenuation	-	14	15	16	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
f_{Peak}	Peak frequency	f_{P1}	-	400	-	Hz
		f_{P2}	-	800	-	Hz
		f_{P3}	-	2400	-	Hz
Volume control						
G_{MAX}	Max gain	-	22	23	24	dB
A_{MAX}	Max attenuation	-	-	-31	-30	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
E_A	Attenuation set error	-	-0.75	0	+0.75	dB
E_T	Tracking error	-	-	-	2	dB
V_{DC}	DC steps	Adjacent attenuation steps	-3	0.1	3	mV
		From 0 dB to G_{MIN}	-5	0.5	5	mV
Soft-mute						
A_{MUTE}	Mute attenuation	-	80	100	-	dB
T_D	Delay time	T1	0.35	0.48	0.65	ms
		T2	0.7	0.96	1.3	ms
		T3	5.6	7.6	9.6	ms
		T4	12.3	15.3	18.3	ms
$V_{TH\ Low}$	Low threshold for SM pin	-	-	-	1	V
$V_{TH\ High}$	High threshold for SM pin	-	2.5	-	-	V
R_{PU}	Internal pull-up resistor	-	32	45	58	kΩ
V_{PU}	Internal pull-up voltage	-	3	3.3	3.6	V
Bass control						
Fc	Center frequency	f_{C1}	-	60	-	Hz
		f_{C2}	-	80	-	Hz
		f_{C3}	-	100	-	Hz
		f_{C4}	-	200	-	Hz
Q_{BASS}	Quality factor	Q_1	-	1	-	-
		Q_2	-	1.25	-	-
		Q_3	-	1.5	-	-
		Q_4	-	2	-	-
C_{RANGE}	Control range	-	±14	±15	±16	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
DC_{GAIN}	Bass-DC-gain	DC = off	-1	0	+1	dB
		DC = on, gain = ±15 dB	±4.3	±4.7	±5.1	dB

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Middle control						
C_{RANGE}	Control range	-	±14	±15	±16	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
f_c	Center frequency	f_{C1}	-	500	-	Hz
		f_{C2}	-	1	-	kHz
		f_{C3}	-	1.5	-	kHz
		f_{C4}	-	2.5	-	kHz
Q_{MIDDLE}	Quality factor	Q_1	-	0.75	-	-
		Q_2	-	1	-	-
		Q_3	-	1.25	-	-
Treble control						
C_{RANGE}	Clipping level	-	±14	±15	±16	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
f_c	Center frequency	f_{C1}	-	10	-	kHz
		f_{C2}	-	12.5	-	kHz
		f_{C3}	-	15	-	kHz
		f_{C4}	-	17.5	-	kHz
Speaker attenuators						
G_{MAX}	Max gain	-	14	15	16	dB
A_{MAX}	Max attenuation	-	-	-79	-74	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
A_{MUTE}	Mute attenuation	-	80	90	-	dB
E_E	Attenuation set error	-	-	-	2	dB
V_{DC}	DC steps	Adjacent attenuation steps	-	0.1	5	mV
Audio outputs						
V_{CL}	Clipping level	d = 0.3 %; byte8_D6=1	2	-	-	V_{RMS}
		d = 1 %; byte8_D6=0	2.2	-	-	V_{RMS}
R_{OUT}	Output impedance	-	-	20	100	W
R_L	Output load resistance	-	2	-	-	kΩ
C_L	Output load capacitor	-	-	-	10	nF
V_{DC}	DC voltage level	-	3.8	4.0	4.2	V
Subwoofer lowpass						
f_{LP}	Lowpass corner frequency	f_{LP1}	-	55	-	Hz
		f_{LP2}	-	85	-	Hz
		f_{LP3}	-	120	-	Hz
		f_{LP4}	-	160	-	Hz

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
DC offset detection circuit						
V_{th}	Zero comp. window size	V1	±10	±25	±40	mV
		V2	±30	±50	±70	mV
		V3	±50	±75	±100	mV
		V4	±70	±100	±130	mV
t_{sp}	Max rejected spike length	-	2	11	30	µs
		-	5	22	50	µs
		-	10	33	70	µs
		-	15	44	90	µs
$I_{CHDCErr}$	DCErr charge current	-	2	5	8	µA
$I_{DISDCErr}$	DCErr discharge current	-	4	5	9	mA
V_{OutH}	DCErr high voltage	-	3	3.3	3.6	V
V_{OutL}	DCErr low voltage	-	-	100	300	mV
General						
e_{NO}	Output noise	BW=20 Hz to 20 kHz A-Weighted, all gain = 0 dB	-	12	22	µV
		BW=20 Hz - 20 kHz A-Weighted, Output muted	-	7	12	µV
S/N	Signal to noise ratio	all gain = 0 dB, A-weighted; V_o = 2 V_{RMS}	98	104	-	dB
D	Distortion	V_{IN} =1 $V_{RMS;}$ all stages 0 dB	-	0.01	0.1	%
S_C	Channel separation left/right	-	-	90	-	dB

4 Description of the audioprocessor

4.1 Input stages

One quasi-differential stereo input, one full-differential/quasi-differential stereo input and three single-ended inputs are available.

4.1.1 Quasi-differential stereo input (QD1)

The QD input is implemented as a buffered quasi-differential stereo stage with 100 kΩ input-impedance at each input. There is -3 dB attenuation at QD input stage.

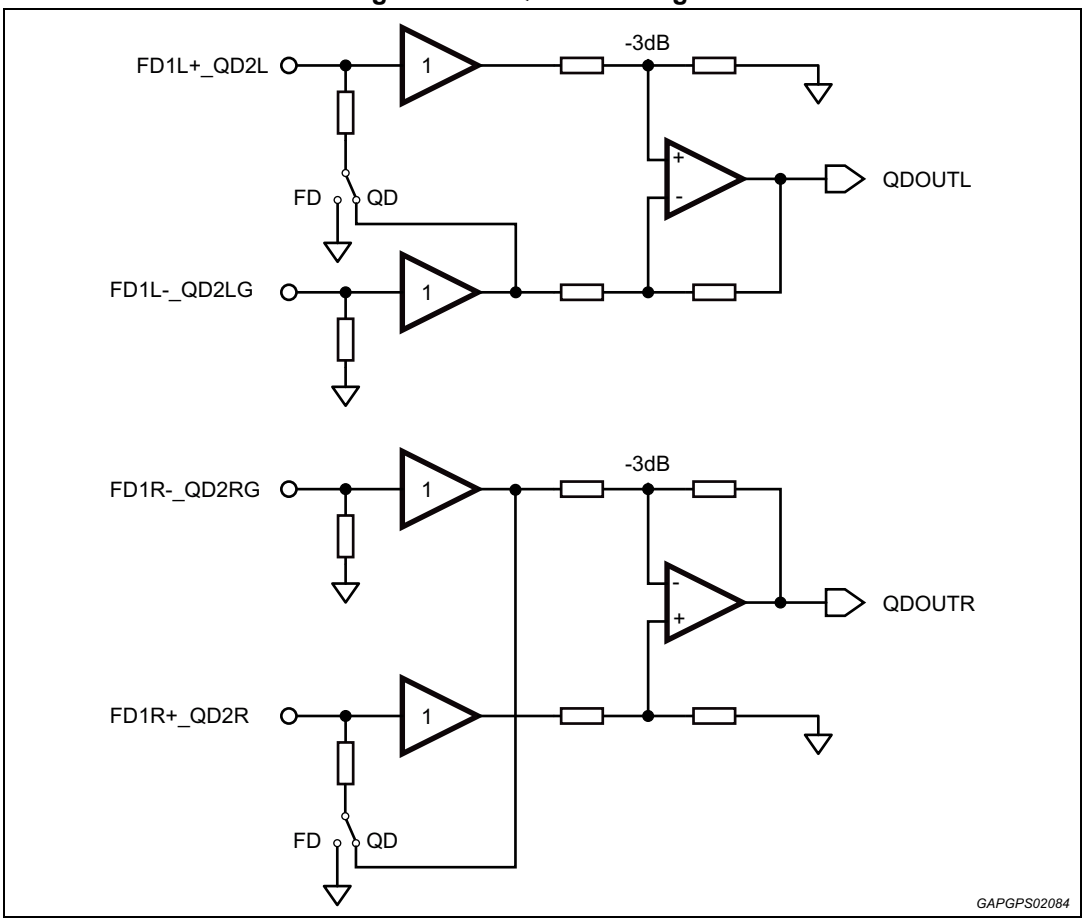
4.1.2 Single-ended stereo input (SE1, SE2, SE3)

The input-impedance at each input is 100 kΩ and the attenuation is fixed to -3 dB for incoming signals.

4.1.3 Full-differential or quasi-differential stereo input (FD/QD2)

This device provides a full-differential stereo input stage (FD) or 2nd quasi-differential stereo input stage. The full differential is a buffered full-differential stereo stage with 100 kΩ input-impedance at each input. When using as QD2 application, it needs to connect the two QD2G pins together from external and the input impedance at QDG becomes 50 kΩ. There is -3 dB attenuation at the input stage. *Figure 3* shows the block diagram of this input stage.

Figure 3. FD/QD block diagram



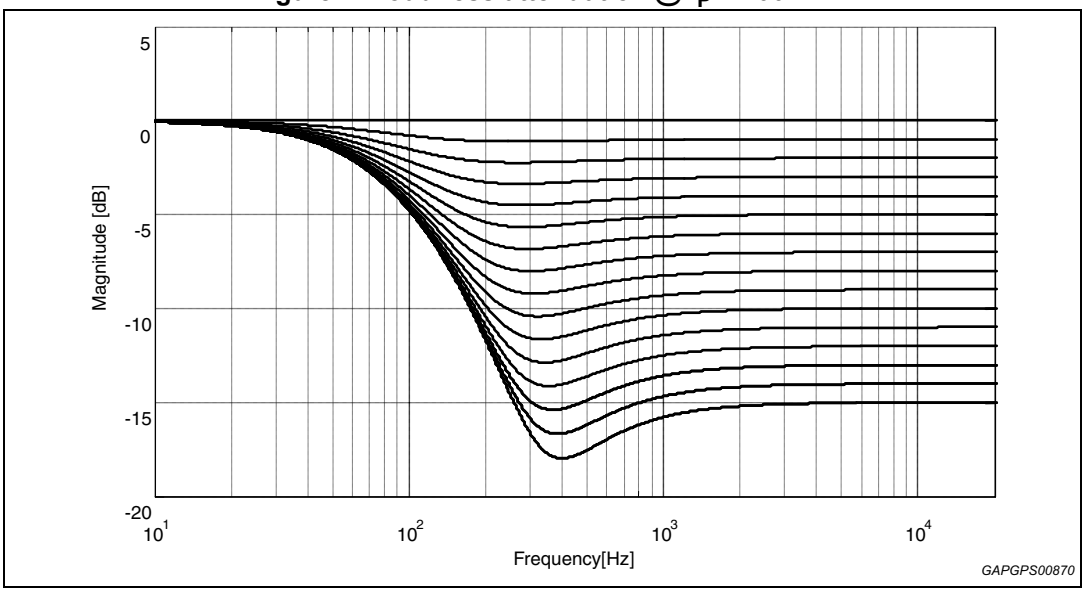
4.2 Loudness

There are four parameters programmable in the loudness stage.

4.2.1 Loudness attenuation

Figure 4 shows the attenuation as a function of frequency at f_P = 400 Hz.

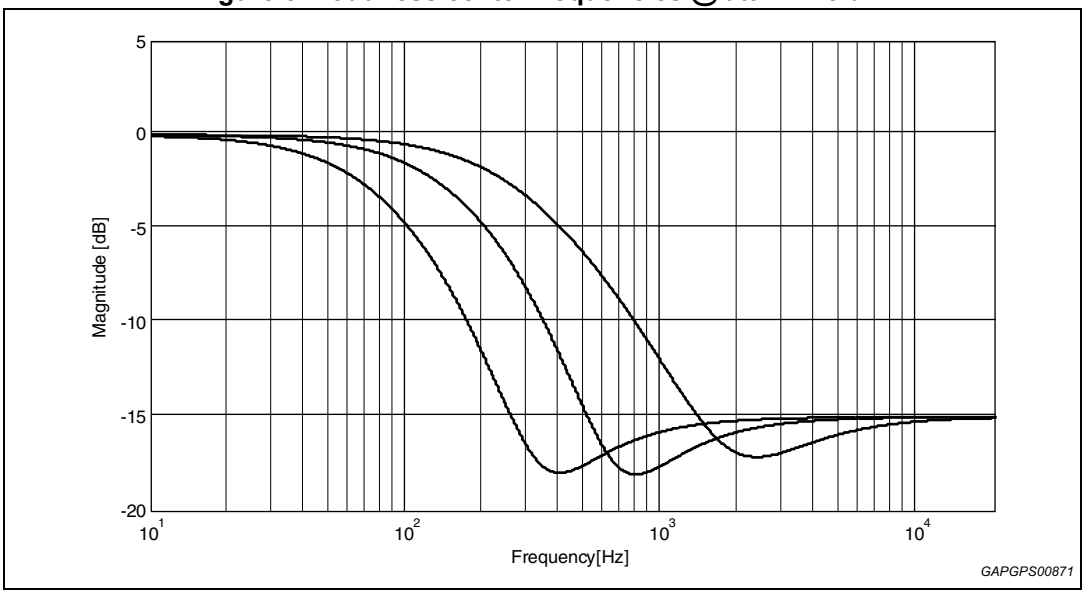
Figure 4. Loudness attenuation @ f_P = 400 Hz.



4.2.2 Peak frequency

Figure 5 shows the four possible peak-frequencies at 400, 800 and 2400 Hz.

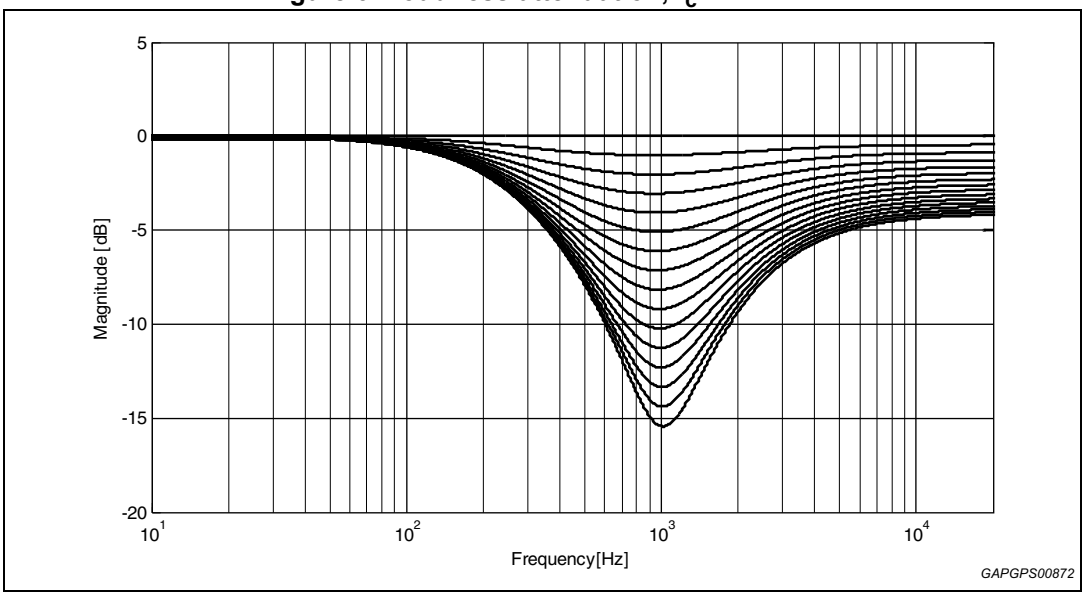
Figure 5. Loudness center frequencies @ attn. = 15 dB.



4.2.3 High frequency boost

Figure 6 shows the different Loudness shapes in low and high frequency boost.

Figure 6. Loudness attenuation, f_c = 2.4 kHz



4.2.4 Flat mode

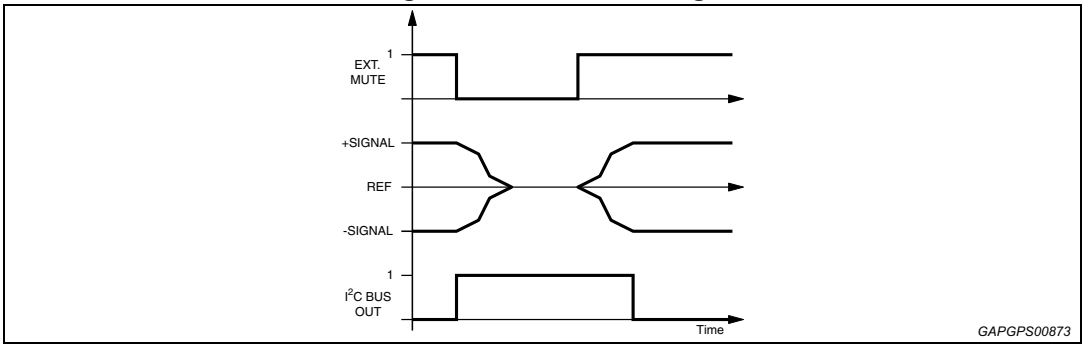
In flat mode the loudness stage works as a 0 dB to -15 dB attenuator.

4.3 Soft-mute

The digitally controlled soft-mute stage allows muting/demuting the signal with a I^2C bus programmable slope. The mute process can either be activated by the soft-mute pin or by the I^2C bus. This slope is realized in a special S-shaped curve to mute slow in the critical regions (see *Figure 7*).

For timing purposes the bit 0 of the I^2C bus output register is set to 1 from the start of muting until the end of demuting.

Figure 7. Soft-mute timing



Note: Please notice that a started mute-action is always terminated and could not be interrupted by a change of the mute –signal.

4.4 Soft-step volume

When the volume-level is changed audible clicks could appear at the output. The root cause of those clicks could either be a DC-offset before the volume-stage or the sudden change of the envelope of the audio signal. With the soft-step-feature both kinds of clicks could be reduced to a minimum and are no more audible. The blend-time from one step to the next is programmable as 5 ms or 10 ms. The soft-step control is described in detail in *Chapter 4.9*.

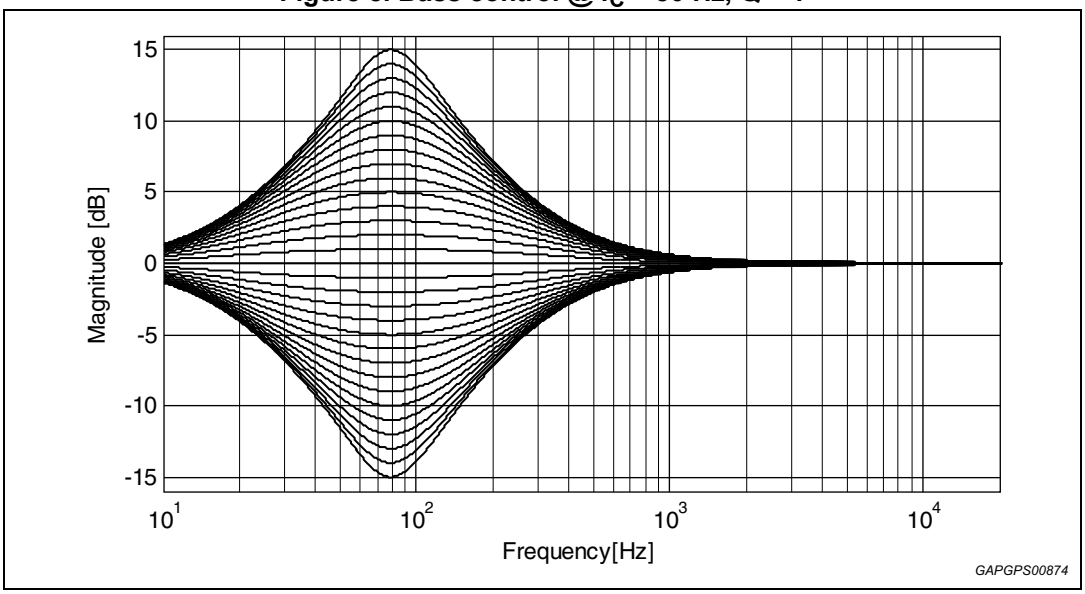
4.5 Bass

There are four parameters programmable in the bass stage:

4.5.1 Bass attenuation

Figure 8 shows the attenuation as a function of frequency at a center frequency of 80 Hz.

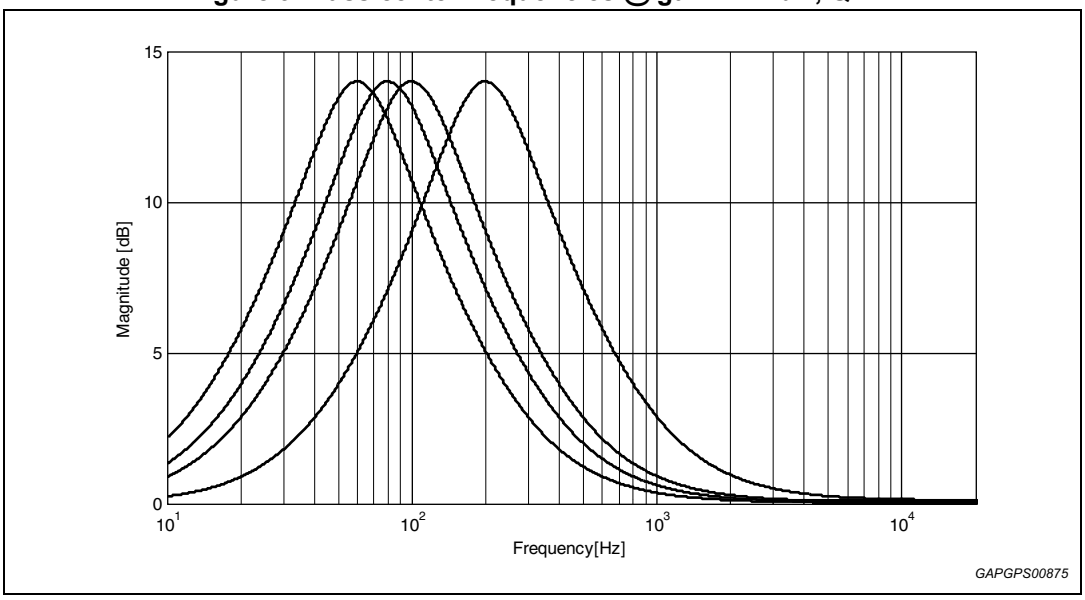
Figure 8. Bass control @ f_C = 80 Hz, Q = 1



4.5.2 Bass center frequency

Figure 9 shows the four possible center frequencies 60, 80, 100 and 200 Hz.

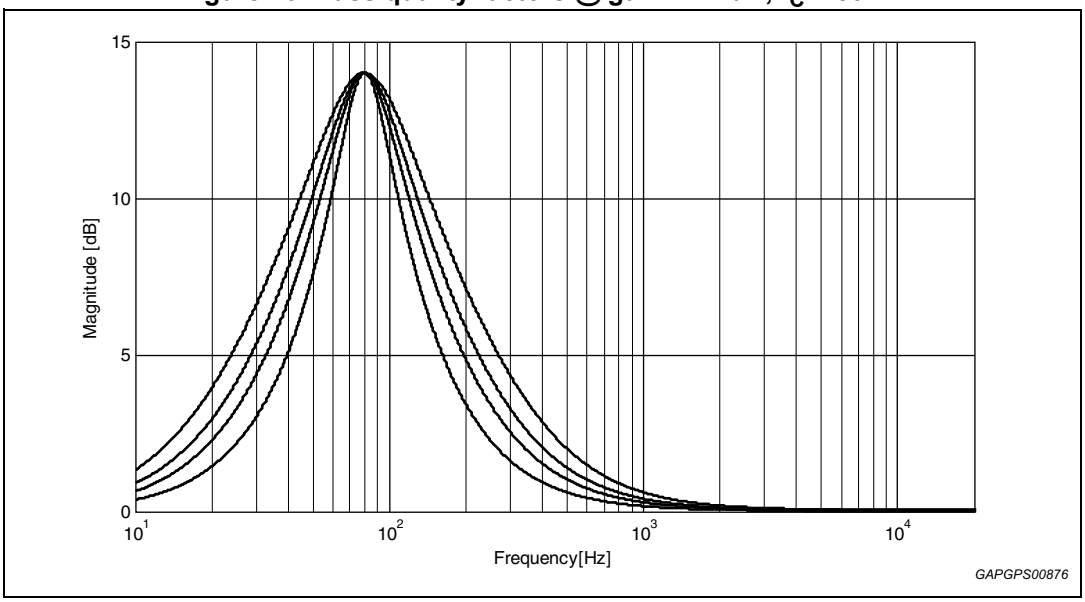
Figure 9. Bass center frequencies @ gain = 14 dB, Q = 1



4.5.3 Quality factors

Figure 10 shows the four possible quality factors 1, 1.25, 1.5 and 2.

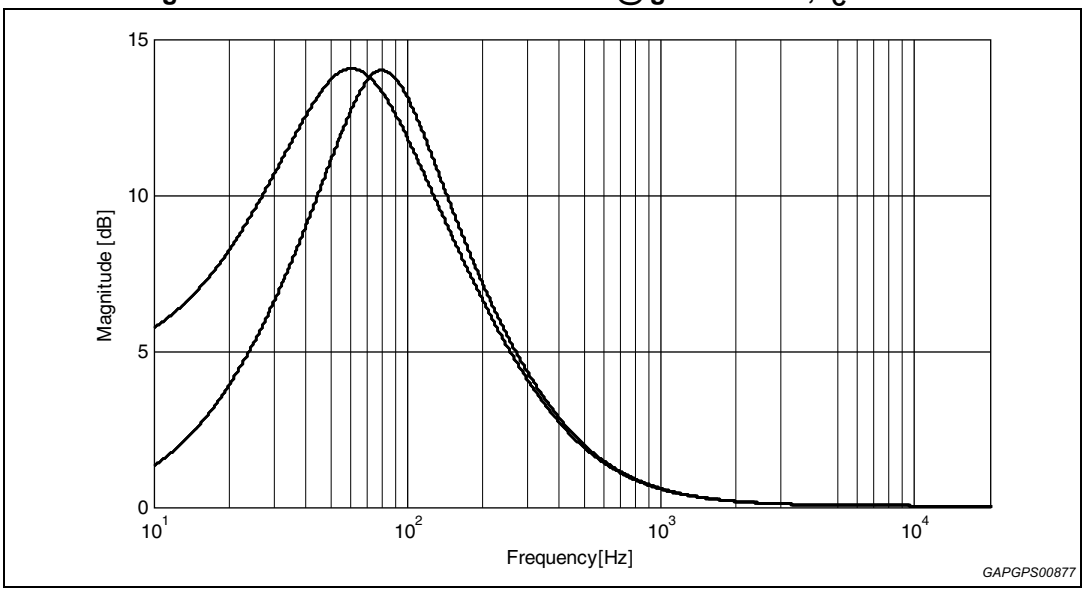
Figure 10. Bass quality factors @ gain = 14 dB, f_C = 80 Hz



4.5.4 DC mode

In this mode the DC-gain is increased by 4.4 dB. In addition the programmed center frequency and quality factor is decreased by 25 % which can be used to reach alternative center frequencies or quality factors.

Figure 11. Bass normal and DC mode @ gain = 14 dB, f_C = 80 Hz



1. The center frequency, Q and DC-mode can be set fully independently.

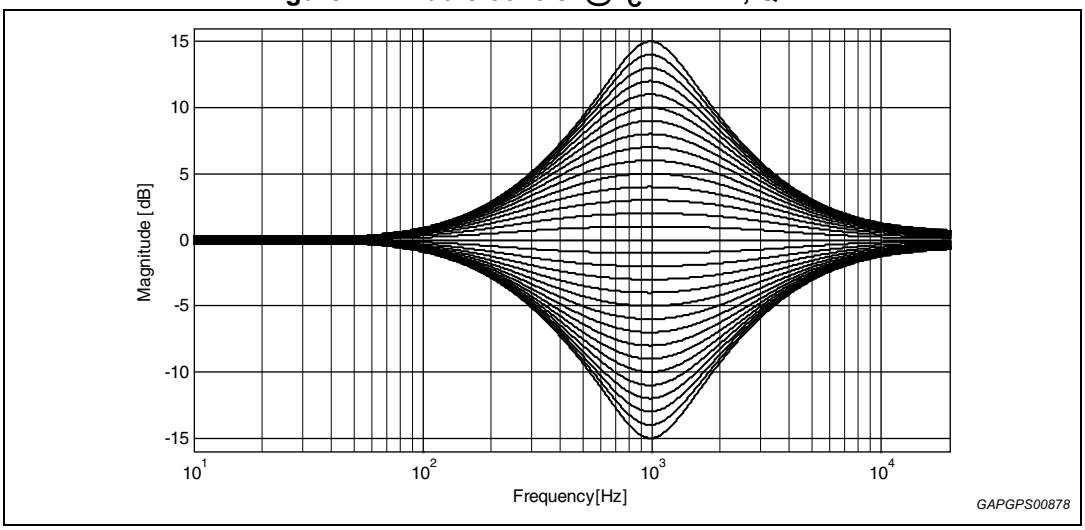
4.6 Middle

There are three parameters programmable in the middle stage:

4.6.1 Middle attenuation

Figure 12 shows the attenuation as a function of frequency at a center frequency of 1 kHz.

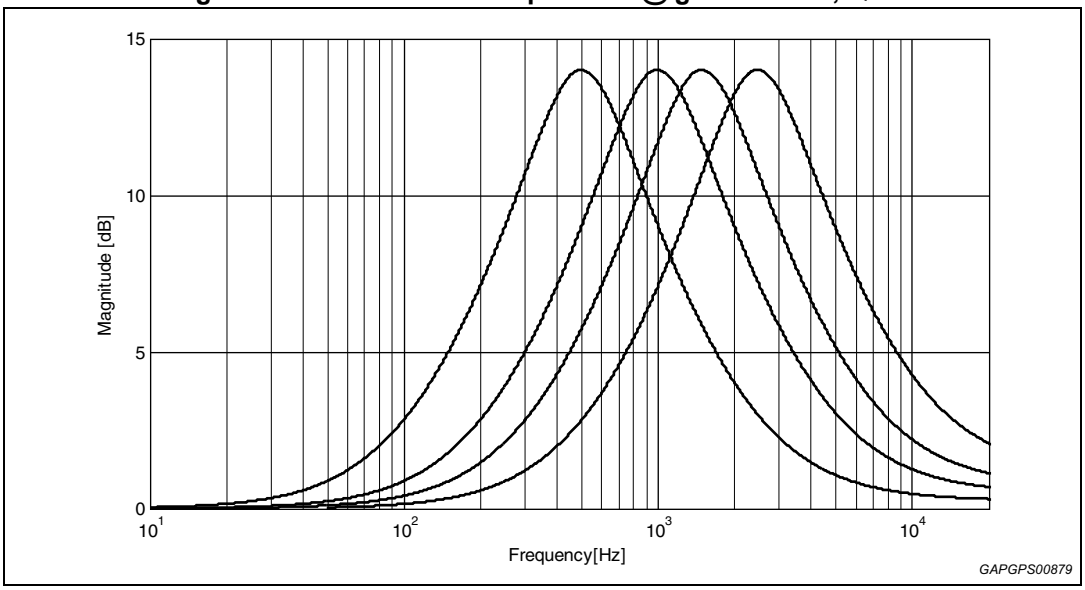
Figure 12. Middle control @ f_C = 1 kHz, Q = 1



4.6.2 Middle center frequency

Figure 13 shows the four possible center frequencies 500 Hz, 1 kHz, 1.5 kHz and 2.5 kHz.

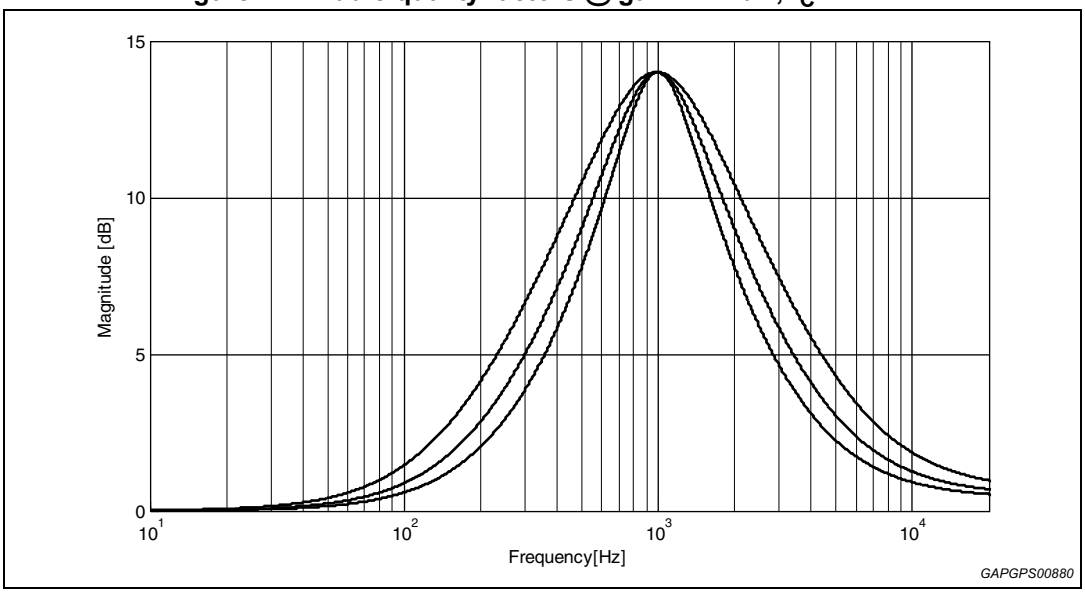
Figure 13. Middle center frequencies @ gain = 14 dB, Q = 1



4.6.3 Quality factors

Figure 14 shows the three possible quality factors 0.75, 1 and 1.25.

Figure 14. Middle quality factors @ gain = 14 dB, f_C = 1 kHz



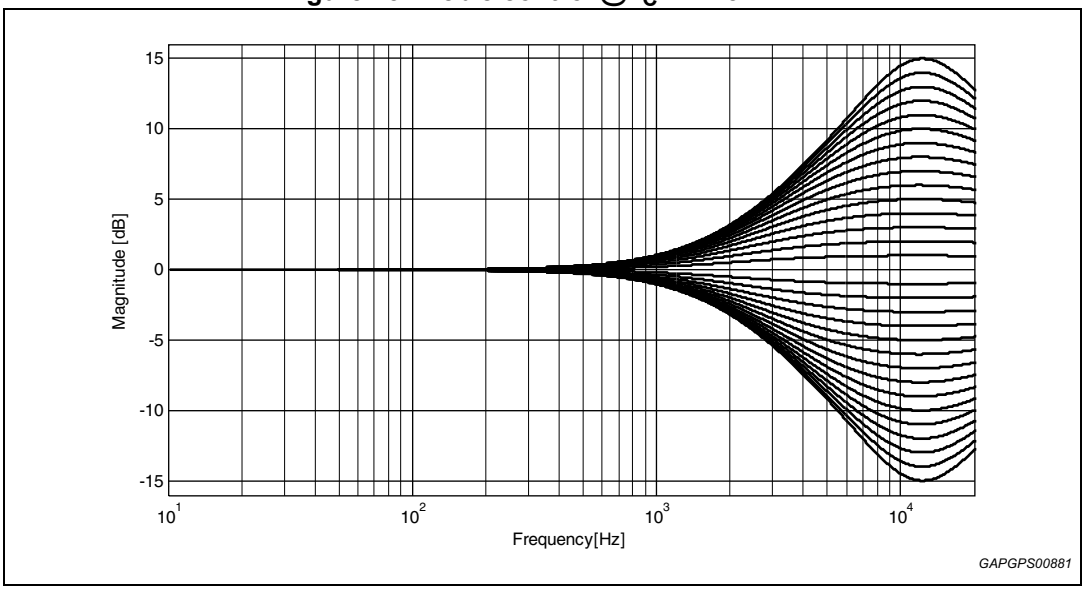
4.7 Treble

There are two parameters programmable in the treble stage:

4.7.1 Treble attenuation

Figure 15 shows the attenuation as a function of frequency at a center frequency of 17.5 kHz.

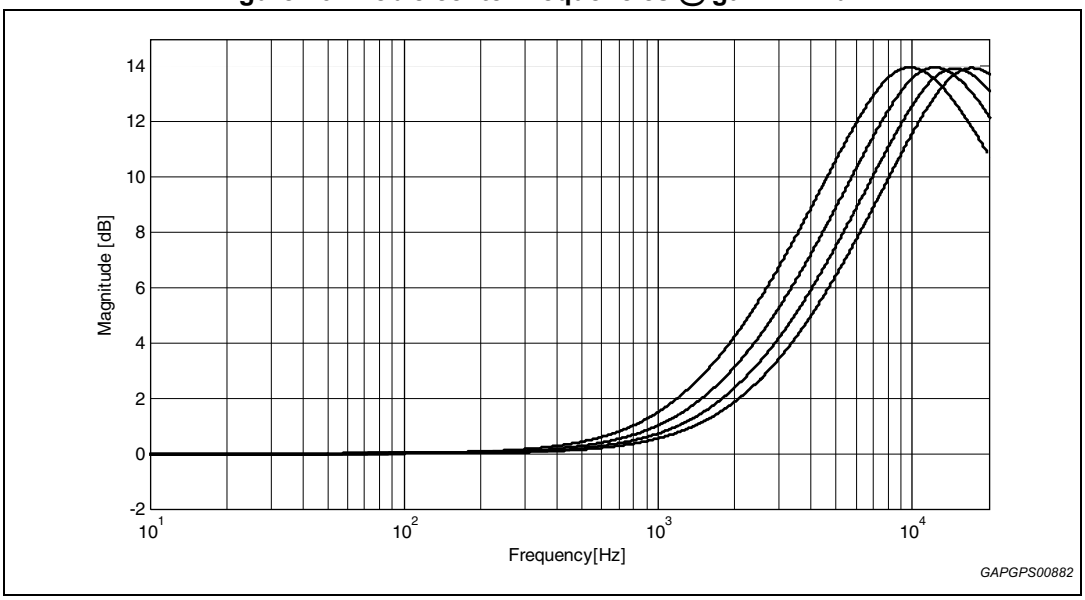
Figure 15. Treble control @ f_C = 17.5 kHz.



4.7.2 Center frequency

Figure 16 shows the four possible center frequencies 10 k, 12.5 k, 15 k and 17.5 kHz.

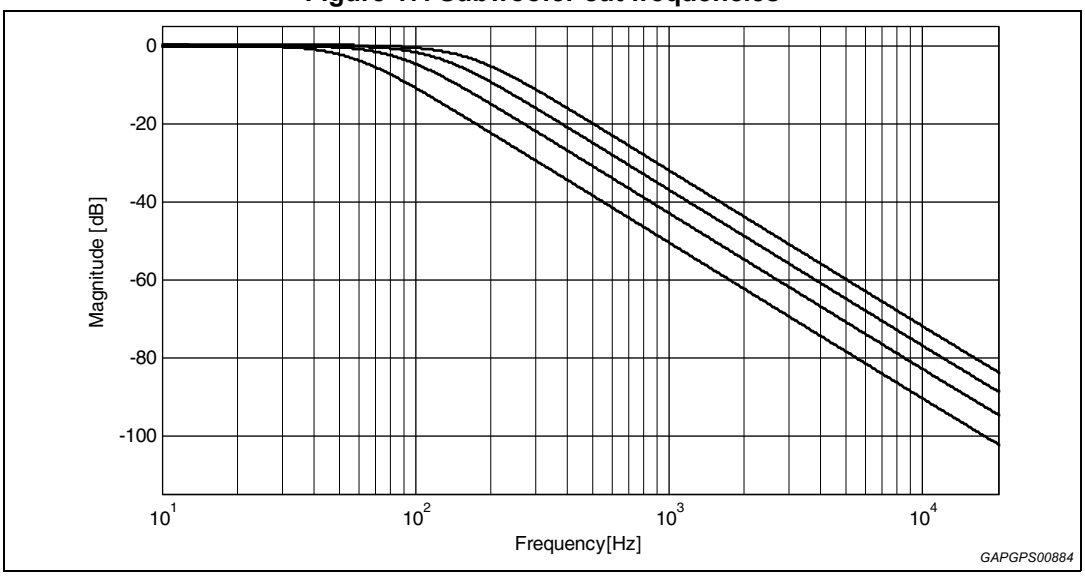
Figure 16. Treble center frequencies @ gain = 14 dB



4.8 Subwoofer filter

The subwoofer lowpass filter has Butterworth characteristics with programmable cut-off frequency (55 Hz / 85 Hz / 120 Hz / 160 Hz). The output phase can be selected between 0 deg and 180 deg. The input of subwoofer takes signal from bass filter output or output of input mux.

Figure 17. Subwoofer cut frequencies



4.9 Soft-step control

In this device, the soft-step function is available for volume, speaker, loudness, treble, middle and bass block. With soft-step function, the audible noise of DC offset or the sudden change of signal can be avoided when adjusting gain setting of the block.

For each block, the soft-step function is controlled by soft-step soft-step on/off control bit in the control table. The soft-step transient time selection (5 ms or 10 ms) is common for all blocks and it is controlled by soft-step time control bit. The soft-step operation of all blocks has a common centralized control. In this case, a new soft-step operation can not be started before the completion previous soft-step.

There are two different modes to activate the soft-step operation. The soft-step operation can be started right after I^2C data sending, or the soft-step can be activated in parallel after data sending of several different blocks. The two modes are controlled by the ‘act bit’ (it is normally bit7 of the byte.) of each byte. When act bit is ‘0’, which means action, the soft-step is activated right after the date byte is sent. When the act bit is ‘1’, which means wait, the block goes to wait for soft-step status. In this case, the block will wait for some other block to activate the operation. The soft-step operation of all blocks in wait status will be done together with the block which activate the soft-step. With this mode, all specific blocks can do the soft-step in parallel. This avoids waiting when the soft-step is operated one by one.

Chip Addr	Sub Addr	0xxxxxxx

|← Soft-step start here

Chip Addr	Sub Addr	1xxxxxxx	1xxxxxxx	.....	0xxxxxxx

|← Soft-step start here for all

4.10 DC offset detector

Using the DC offset detection circuit (*Figure 18*) an offset voltage difference between the audio power amplifier and the APR's Front and Rear outputs can be detected, preventing serious damage to the loudspeakers. The circuit compares whether the signal crosses the zero level inside the audio power at the same time as in the speaker cell. The output of the zero-window-comparator of the power amplifier must be connected with the WinIn-input of the APR. The WinIn-input has an 50kΩ internal pull-up resistor connected to 3.3 V. It is recommended to drive this pin with open-collector outputs only.

To compensate for errors at low frequencies the WinTC-pin are implemented, with external capacitors introducing the same delay τ = 7.5 kΩ * C_{ext} as the AC-coupling between the APR and the power amplifier introduces. For the zero window comparators, the time constant for spike rejection as well as the threshold are programmable.

For electrical characteristics see *Chapter 3 on page 9*.

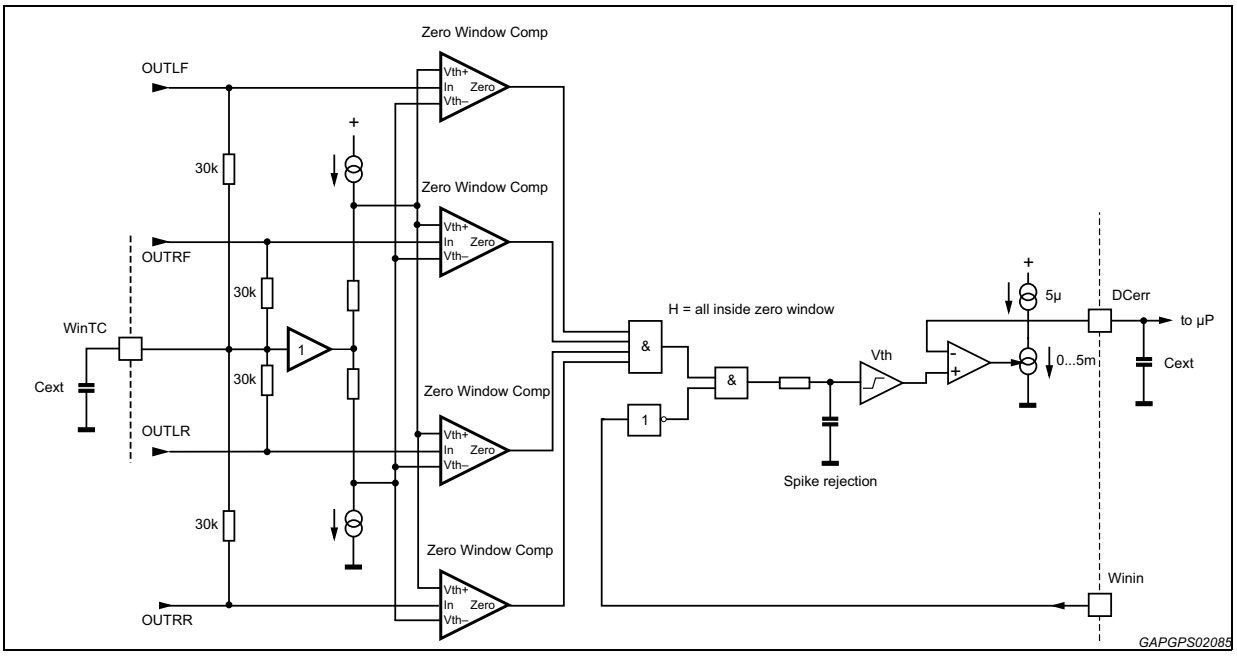
A low-active DC-offset error signal appears at the DCErr output if the next conditions are both true:

a) Front and rear outputs are inside zero crossing windows.

b) The Input voltage VWinIn is logic low whenever at least one output of the power amplifier is outside the zero crossing windows.

After power-on, the external attached capacitor is rapidly charged (fast-charge) to overcome a false indication.

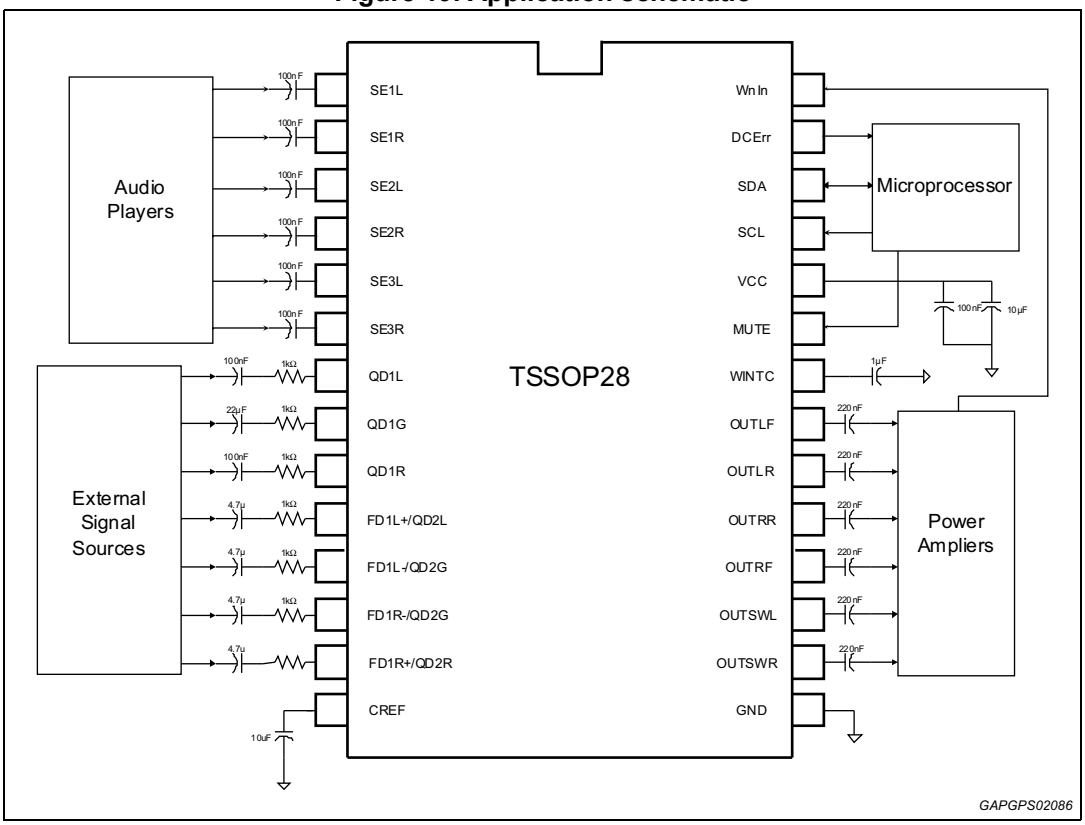
Figure 18. DC offset detection circuit (simplified)



4.11 Audioprocessor testing

In the test mode, which can be activated by setting bit D7 of the I^2C subaddress byte and bit D0 of the testing audioprocessor byte, several internal signals are available at the SE1L pin. In this mode, the input resistance of 100 kΩ is disconnected from the pin. Internal signals available for testing are listed in the data-byte specification.

Figure 19. Application schematic



4.12 Application note

Above application schematic shows a proposal typical application that QD1 and FD/QD2 is used as external signal sources. To limit the leakage current from signal source a 1 kΩ resistor is recommended to put between de-coupling capacitor and pin if the output impedance of external signal source is less than 1 kΩ.

It's guaranteed that all input pins (pin 1~13) will not be broken even if 2Vrms input signal is applied to the pins when CSP is power off.

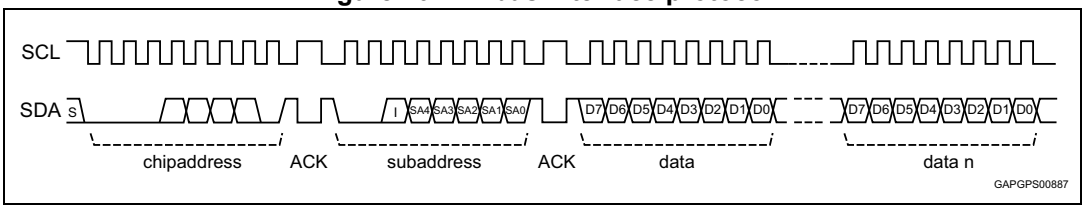
5 I²C bus specification

5.1 Interface protocol

The interface protocol comprises:

- a start condition (S)
- a chip address byte (the LSB determines read/write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)
- the max. clock speed is 400 kbit/s
- 3.3 V logic compatible

Figure 20. I²C bus interface protocol



S = Start

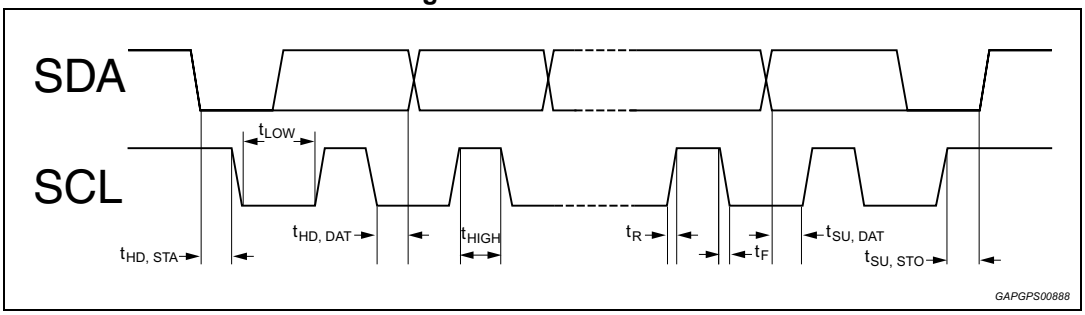
ACK = Acknowledge

5.2 I²C bus electrical characteristics

Table 6. I²C bus electrical characteristics

Symbol	Parameter	Min	Max	Unit
f_{SCL}	SCL clock frequency	-	400	kHz
VIH	High level input voltage	2.4	-	V
VIL	Low level input voltage	-	0.8	V
$t_{HD,STA}$	Hold time for START	0.6	-	µs
$t_{SU,STO}$	Setup time for STOP	0.6	-	µs
t_{LOW}	Low period for SCL clock	1.3	-	µs
t_{HIGH}	High period for SCL clock	0.6	-	µs
t_F	Fall time for SCL/SDA	-	300	ns
t_R	Rise time for SCL/SDA	-	300	ns
$t_{HD,DAT}$	Data hold time	0	-	ns
$t_{SU,DAT}$	Data setup time	100	-	ns

Figure 21. I²C bus data



5.2.1 Receive mode

S	1	0	0	0	1	0	0	R/W	ACK	TS	X	AI	A4	A3	A2	A1	A0	ACK	DATA	ACK	P

S = Start

R/W = "0" -> Receive Mode (Chip can be programmed by µP)

"1" -> Transmission Mode (Data could be received by µP)

ACK = Acknowledge

P = Stop

TS = Testing mode

AI = Auto increment

5.2.2 Transmission mode

S	1	0	0	0	1	0	0	R/W	ACK	X	X	X	X	X	X	BZ	SM	ACK	P

SM = Soft-mute activated for main channel

BZ = Soft-step Busy (‘0’ = Busy)

X = Not used

The transmitted data is automatic updated after each ACK. Transmission can be repeated without new chip address.

5.2.3 Reset condition

A Power-On-Reset is invoked if the supply voltage is below than 3.5 V. After that the registers are initialized to the default data written in following tables.

Table 7. Subaddress (receive mode)

MSB							LSB	Function
I2	I1	I0	A4	A3	A2	A1	A0	
0 1	-	-	-	-	-	-	-	Testing mode Off On
-	x	-	-	-	-	-	-	Not used
-	-	0 1	-	-	-	-	-	Auto increment mode Off On
-	-	-	0	0	0	0	0	Main selector
-	-	-	0	0	0	0	1	Not used
-	-	-	0	0	0	1	0	Not used
-	-	-	0	0	0	1	1	Not used
-	-	-	0	0	1	0	0	Soft-mute / others
-	-	-	0	0	1	0	1	Soft-step I
-	-	-	0	0	1	1	0	Soft-step II / DC-detector
-	-	-	0	0	1	1	1	Loudness
-	-	-	0	1	0	0	0	Volume / output gain
-	-	-	0	1	0	0	1	Treble
-	-	-	0	1	0	1	0	Middle
-	-	-	0	1	0	1	1	Bass
-	-	-	0	1	1	0	0	Subwoofer / middle / bass
-	-	-	0	1	1	0	1	Speaker attenuator left front
-	-	-	0	1	1	1	0	Speaker attenuator right front
-	-	-	0	1	1	1	1	Speaker attenuator left rear
-	-	-	1	0	0	0	0	Speaker attenuator right rear
-	-	-	1	0	0	0	1	Subwoofer attenuator left
-	-	-	1	0	0	1	0	Subwoofer attenuator right
-	-	-	1	0	0	1	1	Testing audio processor 1
-	-	-	1	0	1	0	0	Testing audio processor 2
-	-	-	1	0	1	0	1	Testing audio processor 3

5.3 Data byte specification

Table 8. Main selector (0)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Main source selector
					0	0	0	SE1
					0	0	1	SE3
					0	1	0	QD1
-	-	-	-	-	0	1	1	FD/ QD2
					1	0	0	SE2
					1	0	1	Mute
					1	1	0	Mute
					1	1	1	Mute
-	-	-	-	0	-	-	-	**FD / QD2 selection**
				1				FD
								QD2
-	-	-	0	-	-	-	-	**Main source input gain select**
			1					0 dB
								3 dB
-	-	0	-	-	-	-	-	**Subwoofer flat**
		1						Off
								On
x	x	-	-	-	-	-	-	**Not used**

Not used (1-3)

Table 9. Soft-mute / others (4)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**Soft-mute** On Off
-	-	-	-	-	-	0 1	-	**Pin influence for mute** Pin and IIC IIC
-	-	-	-	0 0 1 1	0 1 0 1	-	-	**Soft-mute time** 0.48 ms 0.96 ms 7.68 ms 15.36 ms
-	-	-	0 1	-	-	-	-	**Subwoofer input source** Input mux Bass output
-	-	0 1	-	-	-	-	-	**Subwoofer enable (OUTSWL & OUTSWR)** On Off
-	0 1	-	-	-	-	-	-	**Fast charge** On Off
0 1	-	-	-	-	-	-	-	**Anti-alias filter** On Off (bypass)

Table 10. Soft-step I (5)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**Loudness soft-step** On Off
-	-	-	-	-	-	0 1	-	**Volume soft-step** On Off
-	-	-	-	-	0 1	-	-	**Treble soft-step** On Off
-	-	-	-	0 1	-	-	-	**Middle soft-step** On Off
-	-	-	0 1	-	-	-	-	**Bass soft-step** On Off
-	-	0 1	-	-	-	-	-	**Speaker LF soft-step** On Off
-	0 1	-	-	-	-	-	-	**Speaker RF soft-step** On Off
0 1	-	-	-	-	-	-	-	**Speaker LR soft-step** On Off

Table 11. Soft-step II / DC detector (6)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**Speaker RR soft-step** On Off
-	-	-	-	-	-	0 1	-	**Subwoofer left soft-step** On Off
-	-	-	-	-	0 1	-	-	**Subwoofer right soft-step** On Off
-	-	-	-	0 1	-	-	-	**Soft-step time** 5 ms 10 ms
-	-	0 0 1 1	0 1 0 1	-	-	-	-	**Zero-comparator window size** ±100 mV ±75 mV ±50 mV ±25 mV
0 0 1 1	0 1 0 1	-	-	-	-	-	-	**Spike rejection time constant** 11 µs 22 µs 33 µs 44 µs

Table 12. Loudness (7)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Attenuation
				0	0	0	0	0 dB
				0	0	0	1	-1 dB
-	-	-	-	:	:	:	:	:
				1	1	1	0	-14 dB
				1	1	1	1	-15 dB
								Center frequency
		0	0					Flat
-	-	0	1	-	-	-	-	400 Hz
		1	0					800 Hz
		1	1					2400 Hz
								High boost
-	0	-	-	-	-	-	-	On
	1							Off
								Soft-step action
0	-	-	-	-	-	-	-	Act
1								Wait

Table 13. Volume / output gain (8)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/attenuation
		0	0	0	0	0	0	+0 dB
		0	0	0	0	0	1	+1 dB
		:	:	:	:	:	:	:
		0	0	1	1	1	1	+15 dB
		0	1	0	0	0	0	+16 dB
		:	:	:	:	:	:	:
		0	1	0	1	1	1	+23 dB
-	-	0	1	1	0	0	0	Not used
		:	:	:	:	:	:	:
		0	1	1	1	1	1	Not used
		1	0	0	0	0	0	-0 dB
		:	:	:	:	:	:	:
		1	0	1	1	1	1	-15 dB
		:	:	:	:	:	:	:
		1	1	1	1	1	1	-31 dB
								Output gain
-	0	-	-	-	-	-	-	1 dB
	1							0 dB
								Soft-step action
0	-	-	-	-	-	-	-	Act
1								Wait

Table 14. Treble filter (9)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/attenuation
			0	0	0	0	0	-15 dB
			0	0	0	0	1	-14 dB
			:	:	:	:	:	:
			0	1	1	1	0	-1 dB
-	-	-	0	1	1	1	1	0 dB
			1	1	1	1	1	0 dB
			1	1	1	1	0	+1 dB
			:	:	:	:	:	:
			1	0	0	0	1	+14 dB
			1	0	0	0	0	+15 dB
								Treble center frequency
	0	0						10.0 kHz
-	0	1	-	-	-	-	-	12.5 kHz
	1	0						15.0 kHz
	1	1						17.5 kHz
								Soft-step action
0	-	-	-	-	-	-	-	Act
1								Wait

Table 15. Middle filter (10)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/attenuation
			0	0	0	0	0	-15 dB
			0	0	0	0	1	-14 dB
			:	:	:	:	:	:
			0	1	1	1	0	-1 dB
-	-	-	0	1	1	1	1	0 dB
			1	1	1	1	1	0 dB
			1	1	1	1	0	+1 dB
			:	:	:	:	:	:
			1	0	0	0	1	+14 dB
			1	0	0	0	0	+15 dB
								Middle Q factor
	0	0						0.75
-	0	1	-	-	-	-	-	1
	1	0						1.25
	1	1						Reserved
								Soft-step action
0	-	-	-	-	-	-	-	Act
1								Wait

Table 16. Bass filter (11)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/attenuation
			0	0	0	0	0	-15 dB
			0	0	0	0	1	-14 dB
			:	:	:	:	:	:
			0	1	1	1	0	-1 dB
-	-	-	0	1	1	1	1	0 dB
			1	1	1	1	1	0 dB
			1	1	1	1	0	+1 dB
			:	:	:	:	:	:
			1	0	0	0	1	+14 dB
			1	0	0	0	0	+15 dB
								Bass Q factor
	0	0						1.0
-	0	1	-	-	-	-	-	1.25
	1	0						1.5
	1	1						2.0
								Soft-step action
0	-	-	-	-	-	-	-	Act
1								Wait

Table 17. Subwoofer / middle / bass (12)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Subwoofer cut-off frequency
						0	0	55 Hz
-	-	-	-	-	-	0	1	85 Hz
						1	0	120 Hz
						1	1	160 Hz
								Subwoofer output phase
-	-	-	-	-	0	-	-	180 deg
					1			0 deg
								Middle center frequency
			0	0				500 Hz
-	-	-	0	1	-	-	-	1000 Hz
			1	0				1500 Hz
			1	1				2500 Hz
								Bass center frequency
	0	0						60 Hz
-	0	1	-	-	-	-	-	80 Hz
	1	0						100 Hz
	1	1						200 Hz
								Bass DC mode
0	-	-	-	-	-	-	-	On
1								Off

Table 18. Speaker attenuation (FL/FR/RL/RR/SWL/SWR) (13-18)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/attenuation
	0	0	0	0	0	0	0	0 dB
	0	0	0	0	0	0	1	1 dB
	:	:	:	:	:	:	:	:
	0	0	0	1	1	1	1	+15 dB
-	0	0	1	0	0	0	0	-0 dB
	0	0	1	0	0	0	1	-1 dB
	:	:	:	:	:	:	:	:
	1	0	1	1	1	1	0	-78 dB
	1	0	1	1	1	1	1	-79 dB
	1	1	x	x	x	x	x	mute
								Soft-step action
0	-	-	-	-	-	-	-	Act
1								Wait

Table 19. Testing audio processor 1 (19)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Audio processor testing mode
-	-	-	-	-	-	-	0	Off
							1	On
								Test multiplexer at SE1L (1)
			0	0	0	0		SSCLK
			0	0	0	1		REQ
			0	0	1	0		SMCLK
			0	0	1	1		DCDet Vth High
			0	1	0	0		DCDet Vth Low
-	-	-	0	1	0	1	-	IntZeroErr
			0	1	1	0		Ref5V5
			0	1	1	1		VGB1.95
			1	0	0	0		Clock200k
			1	0	0	1		SDCLK
			1	0	1	0		VrefDCO
								Clock fast mode (2)
-	-	0	-	-	-	-	-	On
		1						Off
								Clock source (2)
-	0	-	-	-	-	-	-	External
	1							Internal (200 kHz)
								Attenuator gain clock control (2)
0	-	-	-	-	-	-	-	On
1								Off

1. The control bit needs both I²C test mode on & sub-address test mode on.
2. The control bit does not depend on test mode.

Table 20. Testing audio processor 2 (20)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**Test architecture** (1) <u>Normal</u> Split
-	-	-	-	-	-	0 1	-	**Oscillator clock** (2) 400 kHz <u>800 kHz</u>
-	-	-	-	-	0 1	-	-	**Soft-step curve** (2) S-Curve <u>Linear curve</u>
-	-	-	0 0 1 1	0 1 0 1	-	-	-	**Manual set busy signal** (1) Auto Auto 0 <u>1</u>
-	-	-	0 0 1 1	0 1 0 1	-	-	-	**Request for clk generator** (1) Allow Allow Stopped <u>Stopped</u>
-	-	0 1	-	-	-	-	-	**No DCO spike rejection**(1) On <u>Off</u>
x	x	-	-	-	-	-	-	Not used

1. The control bit needs sub-address test mode on.
2. The control bit does not depend on test mode.

Table 21. Testing audio processor 3 (21)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**Enable clock for FL/FR/RL/RR/SWL/SWR** On <u>Off</u>
-	-	-	-	-	-	0 1	-	**Enable clock for volume** On <u>Off</u>
-	-	-	-	-	0 1	-	-	**Enable clock for treble and bass** On <u>Off</u>
-	-	-	-	0 1	-	-	-	**Enable clock for loudness and middle** On <u>Off</u>
x	x	x	x	-	-	-	-	**Not used**

6 Package information

n order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

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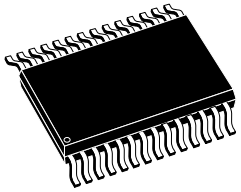
Figure 22. TSSOP28 mechanical data and package dimensions

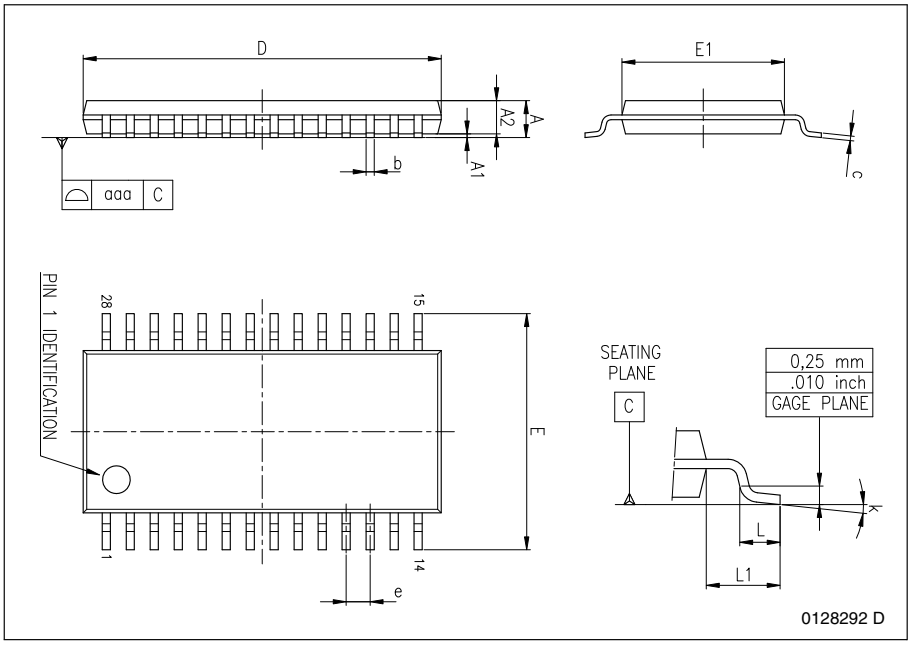
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.200			0.047
A1	0.050		0.150	0.002		0.006
A2	0.800	1.000	1.050	0.031	0.039	0.041
b	0.190		0.300	0.007		0.012
c	0.090		0.200	0.004		0.008
D (1)	9.600	9.700	9.800	0.378	0.382	0.386
E	6.200	6.400	6.600	0.244	0.252	0.260
E1 (1)	4.300	4.400	4.500	0.170	0.173	0.177
e		0.650			0.026	
L	0.450	0.600	0.750	0.018	0.024	0.030
L1		1.000			0.039	
k	0° (min.), 8° (max.)					
aaa			0.100			0.004

Note: 1. D and E1 does not include mold flash or protrusions. Mold flash or po trusions shall not exceed 0.1 5mm (.006inch) per side.

OUTLINE AND MECHANICAL DAT A



TSSOP28
Thin Shrink Small Outline Package
JEDEC MO-153-AC



GAPGPS00889

7 Revision history

Table 22. Document revision history

Date	Revision	Changes
10-Dec-2010	1	Initial release.
26-Feb-2013	2	Added “Note” on page 8.
24-Sep-2013	3	Updated disclaimer.

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