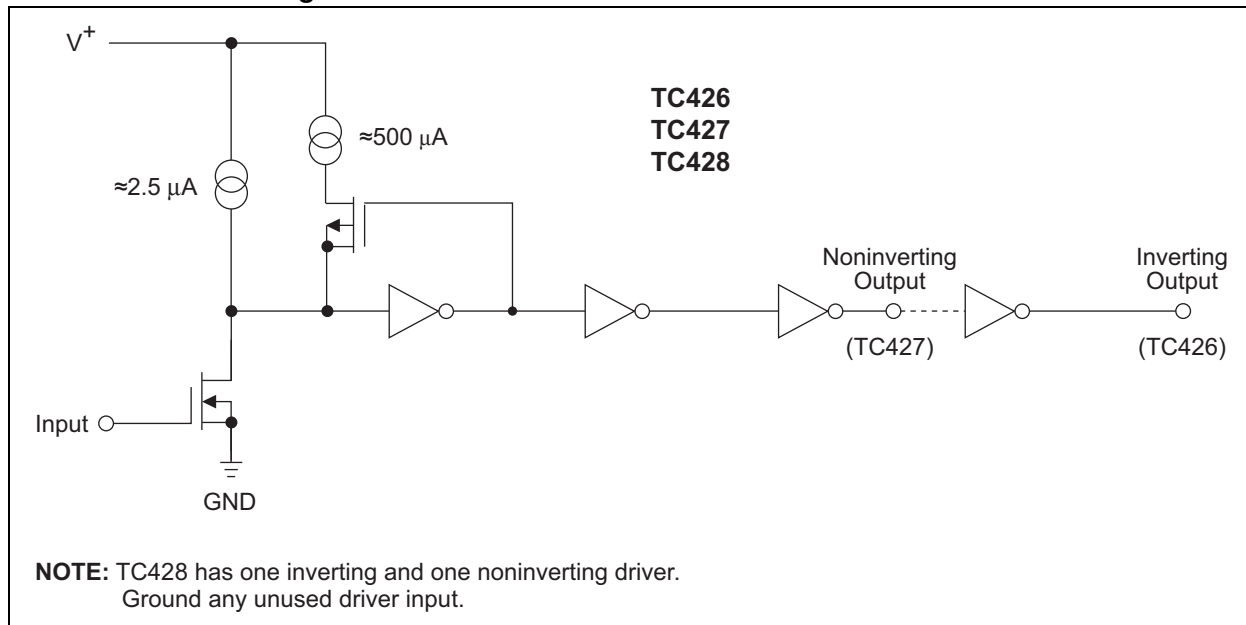


TC426/TC427/TC428

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage	+20V
Input Voltage, Any Terminal	$V_{DD} + 0.3V$ to $GND - 0.3V$
Power Dissipation ($T_A \leq 70^\circ C$)	
PDIP	730 mW
CERDIP	800 mW
SOIC	470 mW
Derating Factor	
PDIP	8 mW/ $^\circ C$
CERDIP	6.4 mW/ $^\circ C$
SOIC	4 mW/ $^\circ C$
Operating Temperature Range	
C Version	$0^\circ C$ to $+70^\circ C$
I Version	$-25^\circ C$ to $+85^\circ C$
E Version	$-40^\circ C$ to $+85^\circ C$
M Version	$-55^\circ C$ to $+125^\circ C$
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC426/TC427/TC428 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: $T_A = +25^\circ C$ with $4.5V \leq V_{DD} \leq 18V$, unless otherwise noted.						
Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
Input						
V_{IH}	Logic 1, High Input Voltage	2.4	—	—	V	
V_{IL}	Logic 0, Low Input Voltage	—	—	0.8	V	
I_{IN}	Input Current	-1	—	1	μA	$0V \leq V_{IN} \leq V_{DD}$
Output						
V_{OH}	High Output Voltage	$V_{DD} - 0.025$	—	—	V	
V_{OL}	Low Output Voltage	—	—	0.025	V	
R_{OH}	High Output Resistance	—	10	15	Ω	$I_{OUT} = 10\text{ mA}$, $V_{DD} = 18V$
R_{OL}	Low Output Resistance	—	6	10	Ω	$I_{OUT} = 10\text{ mA}$, $V_{DD} = 18V$
I_{PK}	Peak Output Current	—	1.5	—	A	
Switching Time (Note 1)						
t_R	Rise Time	—	—	30	nsec	Figure 3-1, Figure 3-2
t_F	Fall Time	—	—	30	nsec	Figure 3-1, Figure 3-2
t_{D1}	Delay Time	—	—	50	nsec	Figure 3-1, Figure 3-2
t_{D2}	Delay Time	—	—	75	nsec	Figure 3-1, Figure 3-2
Power Supply						
I_S	Power Supply Current	—	—	8 0.4	mA	$V_{IN} = 3V$ (Both Inputs) $V_{IN} = 0V$ (Both Inputs)

Note 1: Switching times ensured by design.

TC426/TC427/TC428

TC426/TC427/TC428 ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Over operating temperature range with $4.5V \leq V_{DD} \leq 18V$, unless otherwise noted.

Input

V_{IH}	Logic 1, High Input Voltage	2.4	—	—	V	
V_{IL}	Logic 0, Low Input Voltage	—	—	0.8	V	
I_{IN}	Input Current	-10	—	10	μA	$0V \leq V_{IN} \leq V_{DD}$

Output

V_{OH}	High Output Voltage	$V_{DD} - 0.025$	—	—	V	
V_{OL}	Low Output Voltage	—	—	0.025	V	
R_{OH}	High Output Resistance	—	13	20	Ω	$I_{OUT} = 10 \text{ mA}, V_{DD} = 18V$
R_{OL}	Low Output Resistance	—	8	15	Ω	$I_{OUT} = 10 \text{ mA}, V_{DD} = 18V$

Switching Time (Note 1)

t_R	Rise Time	—	—	60	nsec	Figure 3-1, Figure 3-2
t_F	Fall Time	—	—	60	nsec	Figure 3-1, Figure 3-2
t_{D1}	Delay Time	—	—	75	nsec	Figure 3-1, Figure 3-2
t_{D2}	Delay Time	—	—	120	nsec	Figure 3-1, Figure 3-2

Power Supply

I_S	Power Supply Current	—	—	12	mA	$V_{IN} = 3V$ (Both Inputs)
		—	—	0.6		$V_{IN} = 0V$ (Both Inputs)

Note 1: Switching times ensured by design.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin No. (8-Pin PDIP, SOIC, CERDIP)	Symbol	Description
1	NC	No Internal Connection.
2	IN A	Control Input A, TTL/CMOS compatible logic input.
3	GND	Ground.
4	IN B	Control Input B, TTL/CMOS compatible logic input.
5	OUT B	CMOS totem-pole output.
6	V _{DD}	Supply input, 4.5V to 18V.
7	OUT A	CMOS totem-pole output.
8	NC	No internal Connection.

TC426/TC427/TC428

3.0 APPLICATIONS INFORMATION

3.1 Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging a 1000 pF load to 18V in 25 nsec requires an 0.72A current from the device power supply.

To ensure low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low-inductance ceramic disk capacitors with short lead lengths (< 0.5 in.) should be used. A 1 μ F film capacitor in parallel with one or two 0.1 μ F ceramic disk capacitors normally provides adequate bypassing.

3.2 Grounding

The TC426 and TC428 contain inverting drivers. Ground potential drops developed in common ground impedances from input to output will appear as negative feedback and degrade switching speed characteristics.

Individual ground returns for the input and output circuits or a ground plane should be used.

3.3 Input Stage

The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 2.5 mA current source load. With a logic '1' input, the maximum quiescent supply current is 8 mA. Logic '0' input level signals reduce quiescent current to 0.4 mA maximum. Minimum power dissipation occurs for logic '0' inputs for the TC426/TC427/TC428. **Unused driver inputs must be connected to V_{DD} or GND.**

The drivers are designed with 100 mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5V, making the device TTL compatible over the 4.5V to 18V supply operating range. Input current is less than 1 μ A over this range.

The TC426/TC427/TC428 may be directly driven by the TL494, SG1526/1527, SG1524, SE5560, and similar switch-mode power supply integrated circuits.

3.4 Power Dissipation

The supply current vs frequency and supply current vs capacitive load characteristic curves will aid in determining power dissipation calculations.

The TC426/TC427/TC428 CMOS drivers have greatly reduced quiescent DC power consumption. Maximum quiescent current is 8 mA compared to the DS0026 40 mA specification. For a 15V supply, power dissipation is typically 40 mW.

Two other power dissipation components are:

- Output stage AC and DC load power.
- Transition state power.

Output stage power is:

$$P_o = P_{DC} + P_{AC} \\ = V_o (I_{DC}) + f C_L V_S^2$$

Where:

- V_o = DC output voltage
- I_{DC} = DC output load current
- f = Switching frequency
- V_s = Supply voltage

In power MOSFET drive applications the P_{DC} term is negligible. MOSFET power transistors are high-impedance, capacitive input devices. In applications where resistive loads or relays are driven, the P_{DC} component will normally dominate.

The magnitude of P_{AC} is readily estimated for several cases:

- | A. | B. |
|-----------------------------|-----------------------------|
| 1. f = 200 kHz | 1. f = 200 kHz |
| 2. C _L = 1000 pf | 2. C _L = 1000 pf |
| 3. V _s = 18V | 3. V _s = 15V |
| 4. P _{AC} = 65 mW | 4. P _{AC} = 45 mW |

During output level state changes, a current surge will flow through the series connected N and P channel output MOSFETS as one device is turning "ON" while the other is turning "OFF". The current spike flows only during output transitions. The input levels should not be maintained between the logic '0' and logic '1' levels. **Unused driver inputs must be tied to ground and not be allowed to float.** Average power dissipation will be reduced by minimizing input rise times. As shown in the characteristic curves, average supply current is frequency dependent.

TC426/TC427/TC428

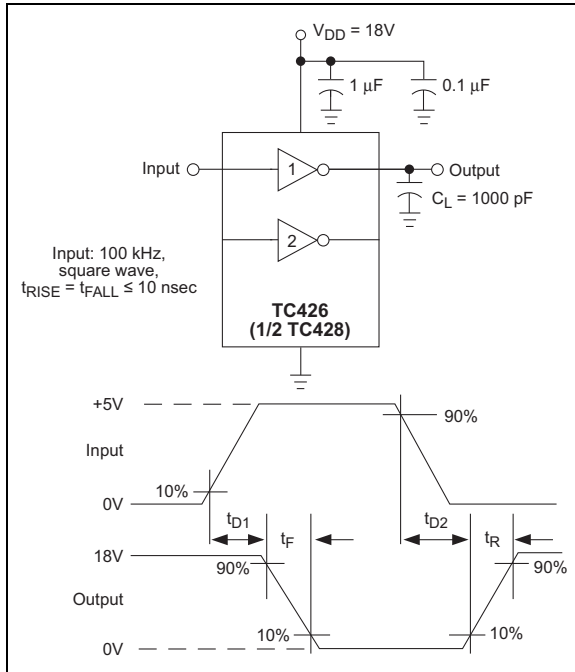


FIGURE 3-1: Inverting Driver Switching Time Test Circuit

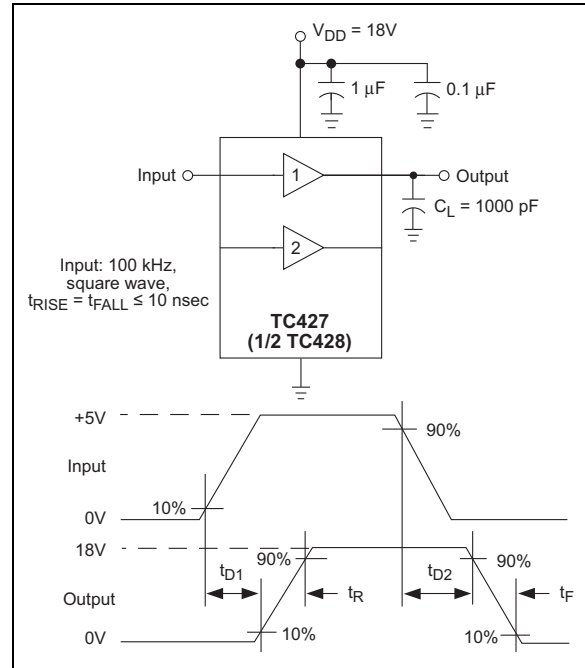


FIGURE 3-2: Noninverting Driver Switching Time Test Circuit

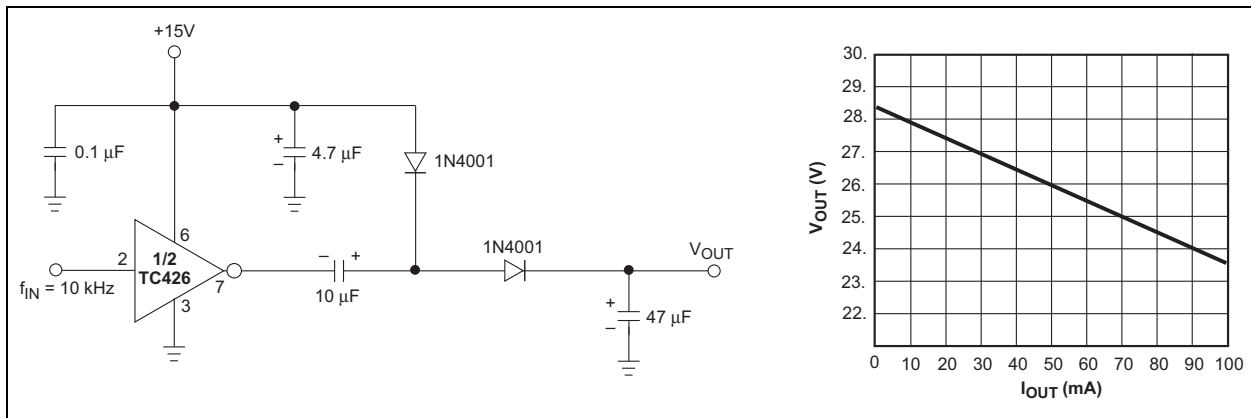


FIGURE 3-3: Voltage Doubler

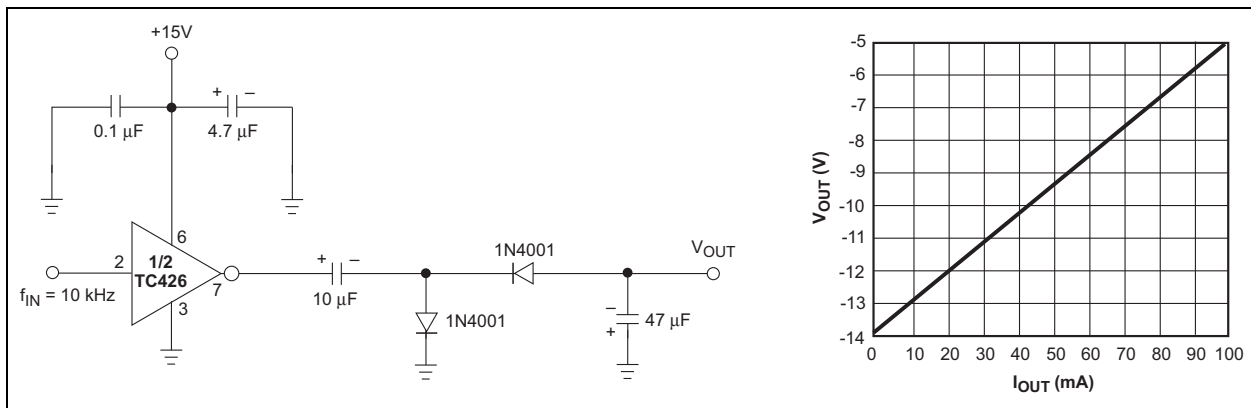
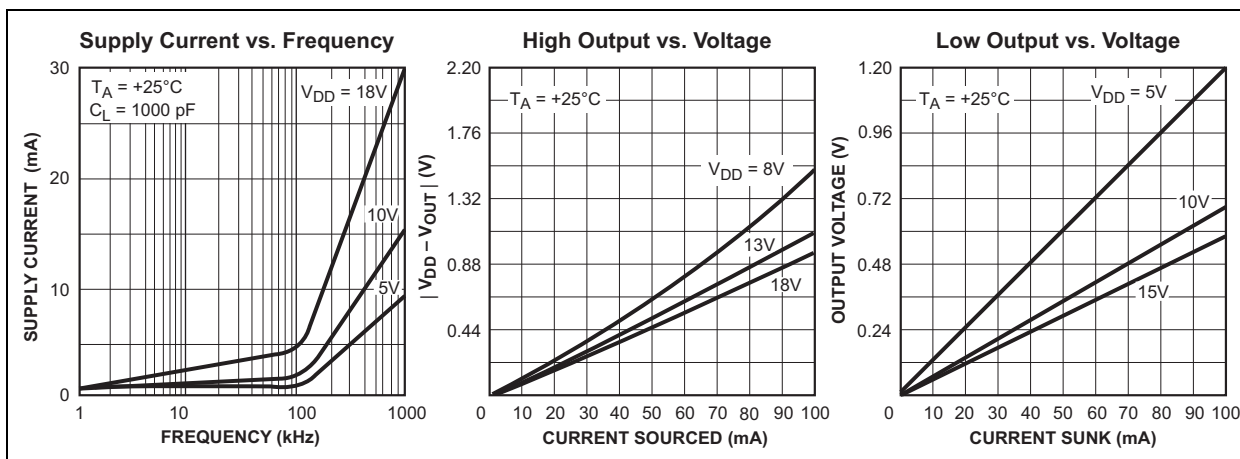
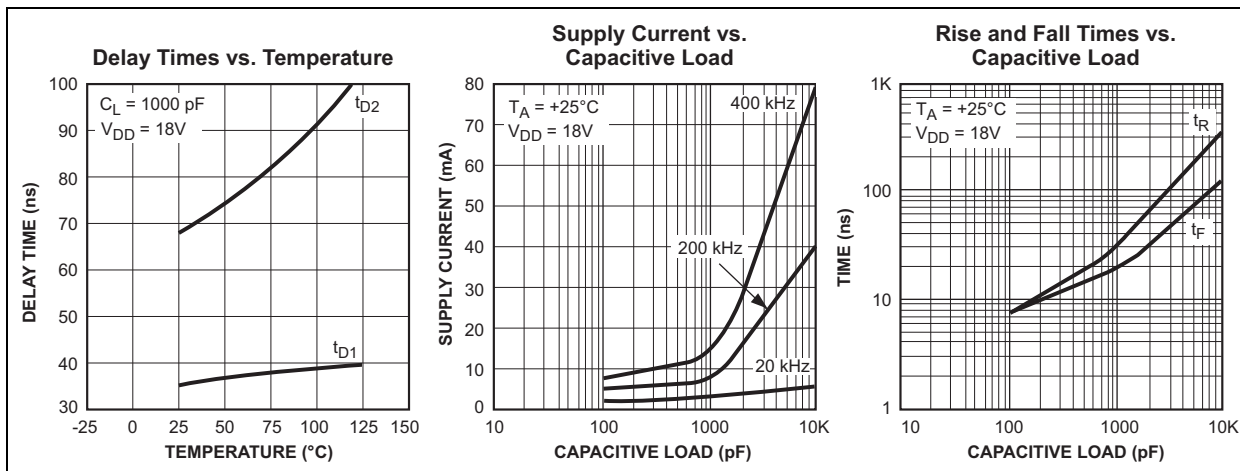
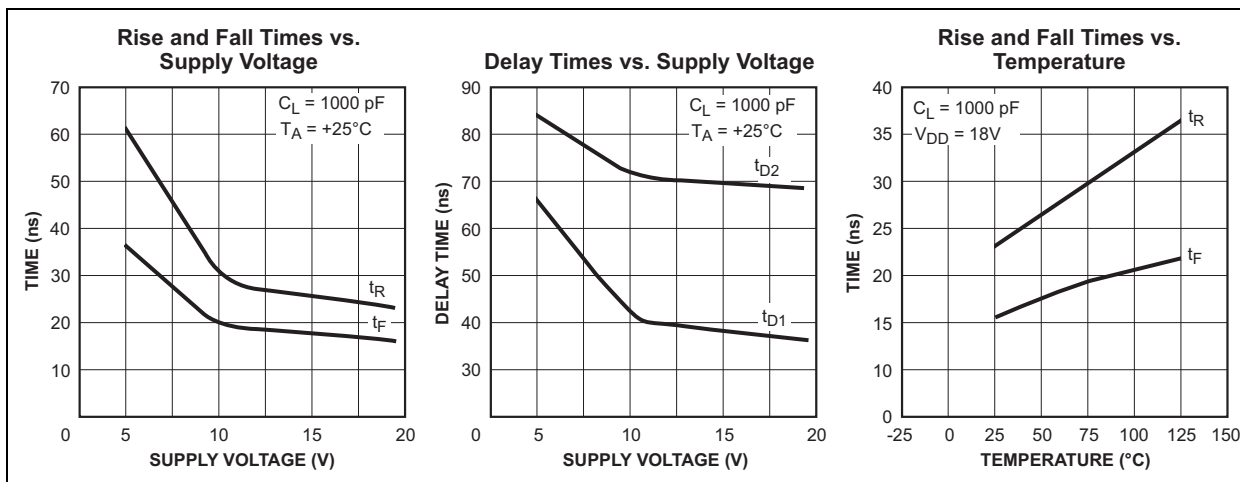


FIGURE 3-4: Voltage Inverter

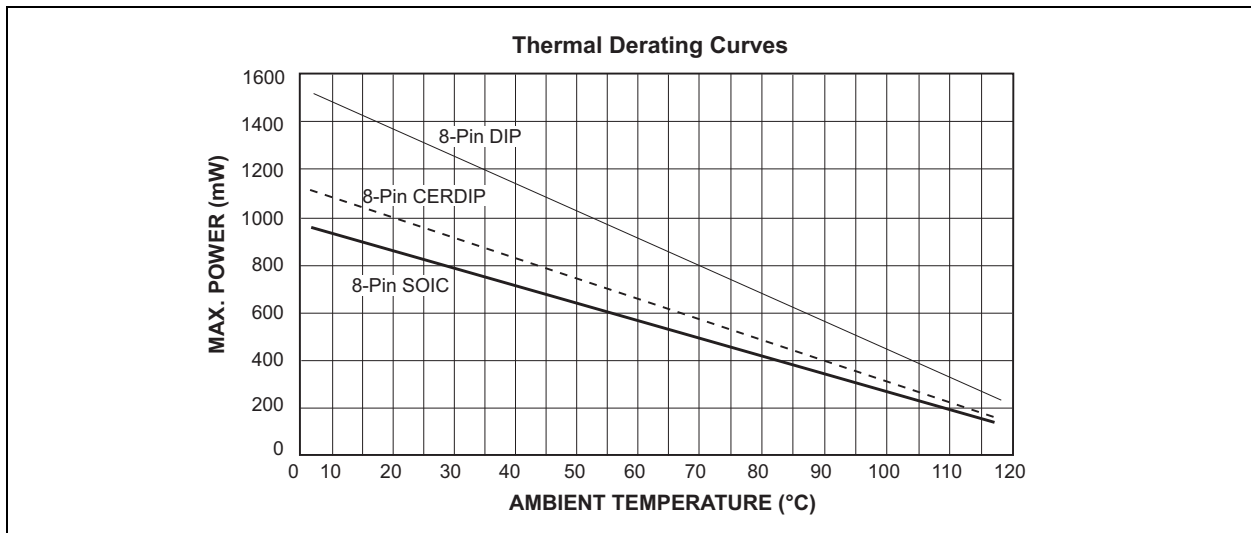
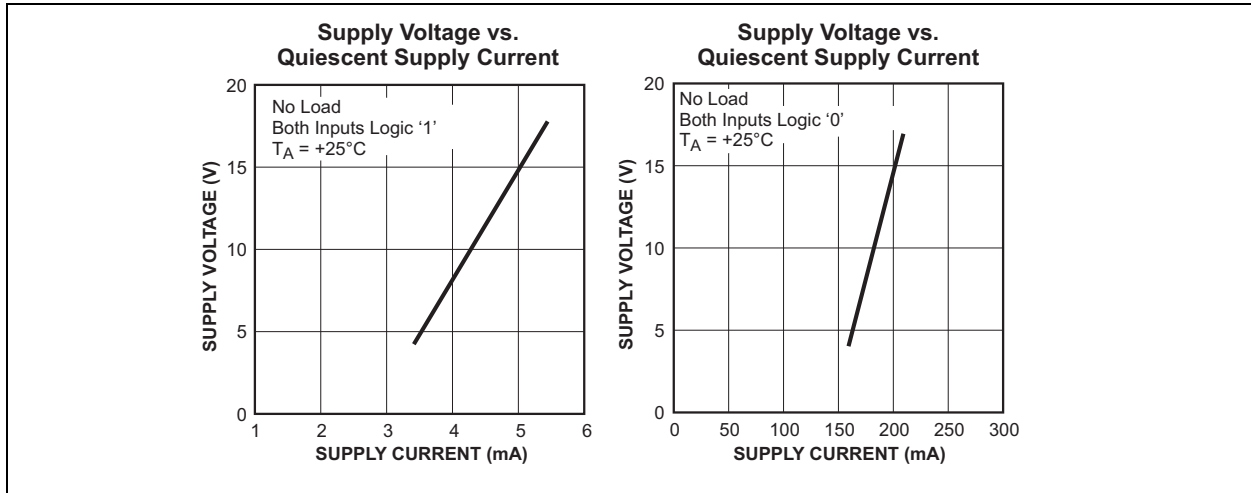
TC426/TC427/TC428

4.0 TYPICAL CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.



TYPICAL CHARACTERISTICS (CONTINUED)



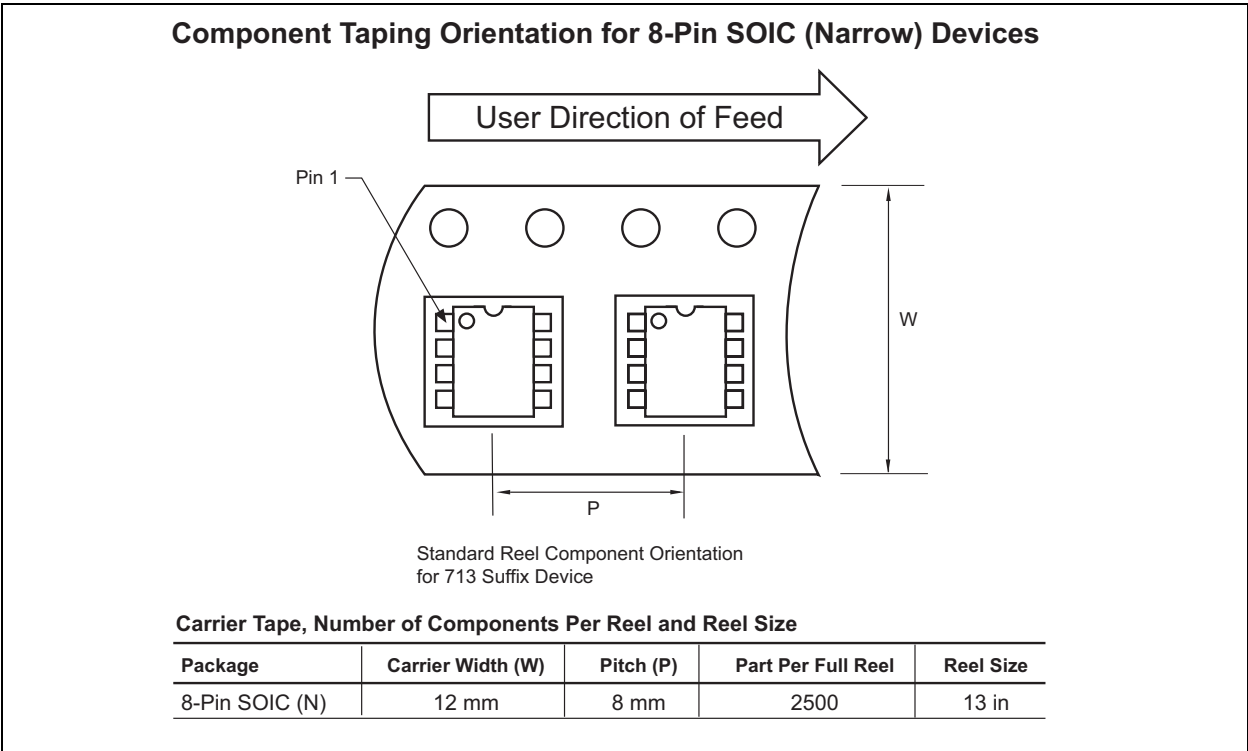
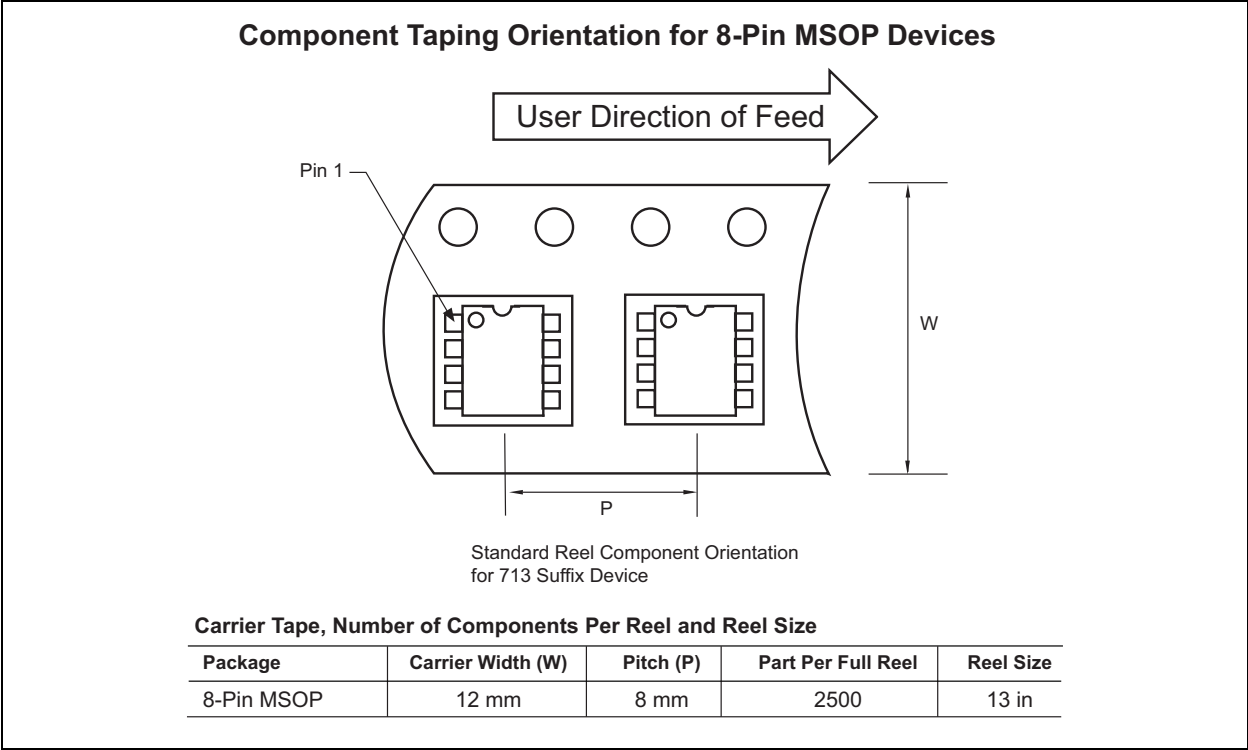
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5.0 PACKAGING INFORMATION

5.1 Package Marking Information

Package marking data not available at this time.

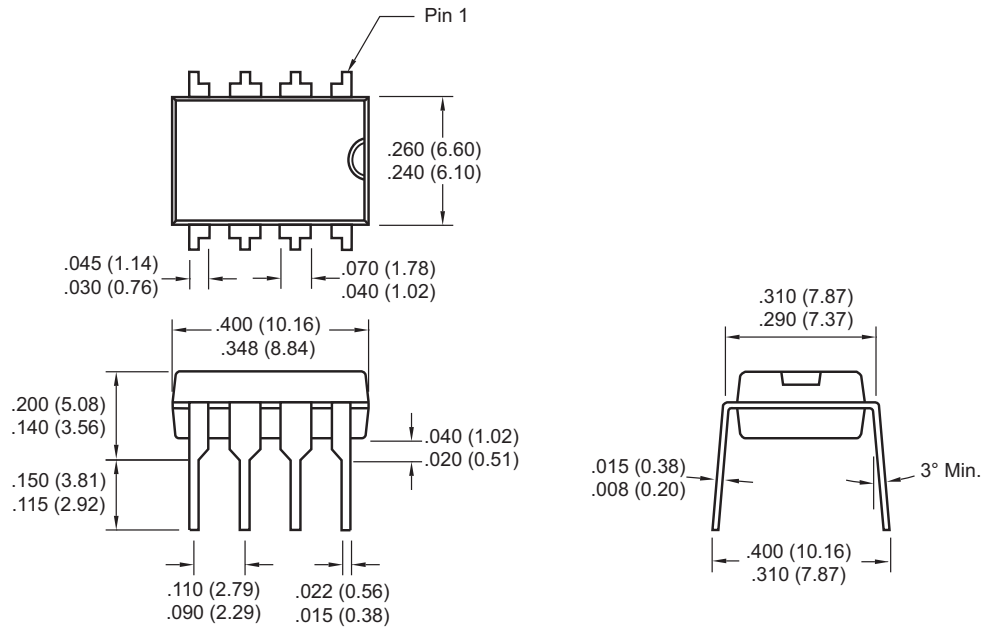
5.2 Taping Form



5.3 Package Dimensions

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

8-Pin Plastic DIP



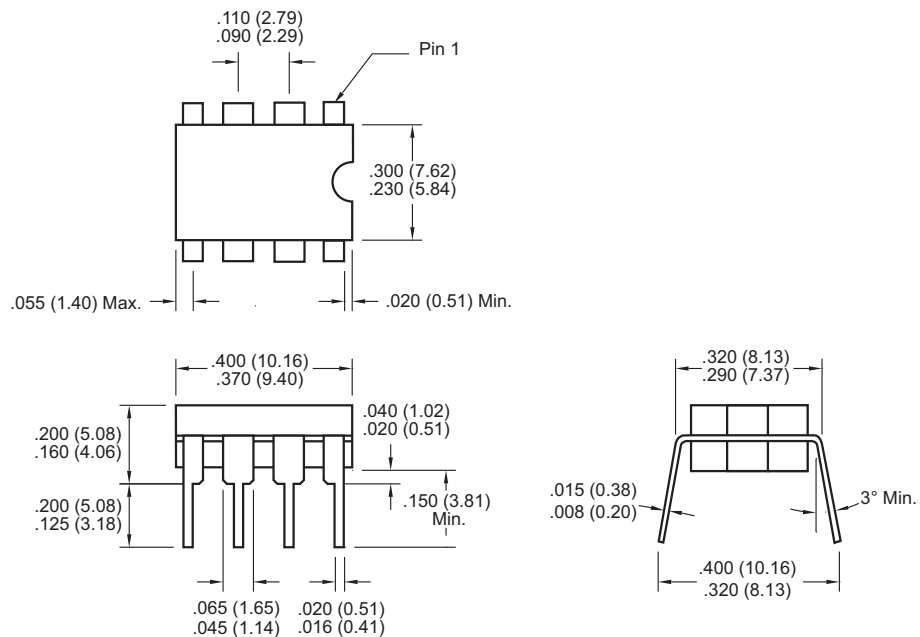
Dimensions: inches (mm)

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Package Dimensions (Continued)

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8-Pin Cerdip (Narrow)

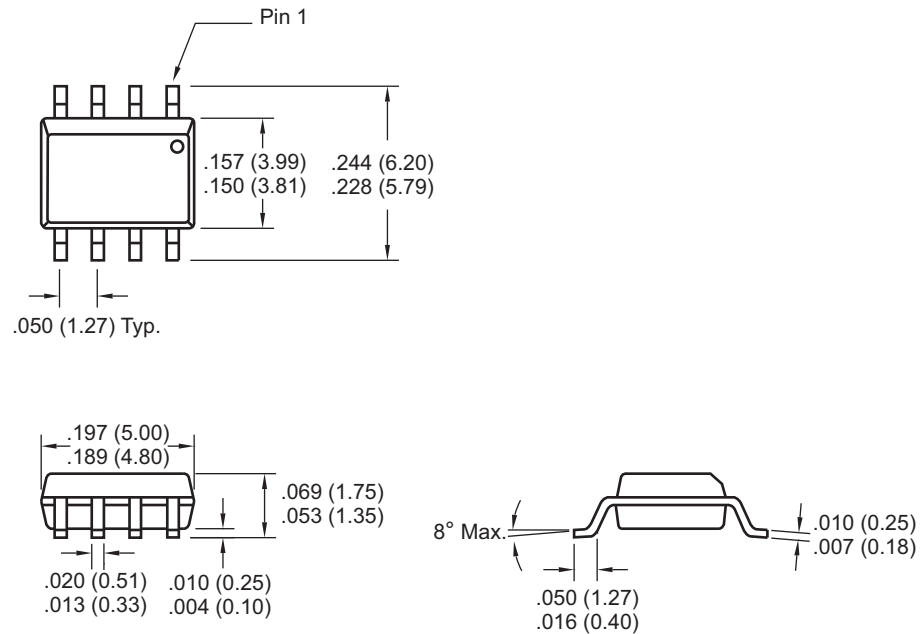


Dimensions: inches (mm)

Package Dimensions (Continued)

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8-Pin SOIC



Dimensions: inches (mm)

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6.0 REVISION HISTORY

Revision D (December 2012)

Added a note to each package outline drawing.

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