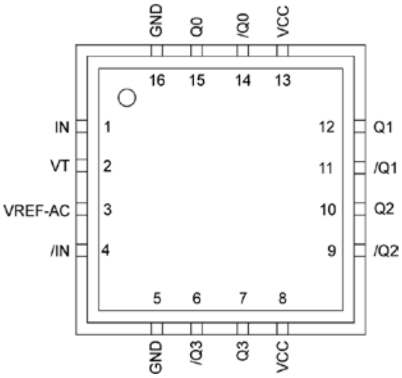
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89854UMG	QFN-16	Industrial	854U with Pb-free bar-line indicator	Pb-Free NiPdAu
SY89854UMGTR[2]	QFN-16	Industrial	854U with Pb-free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals Only.
2. Tape and Reel.

Pin Configuration

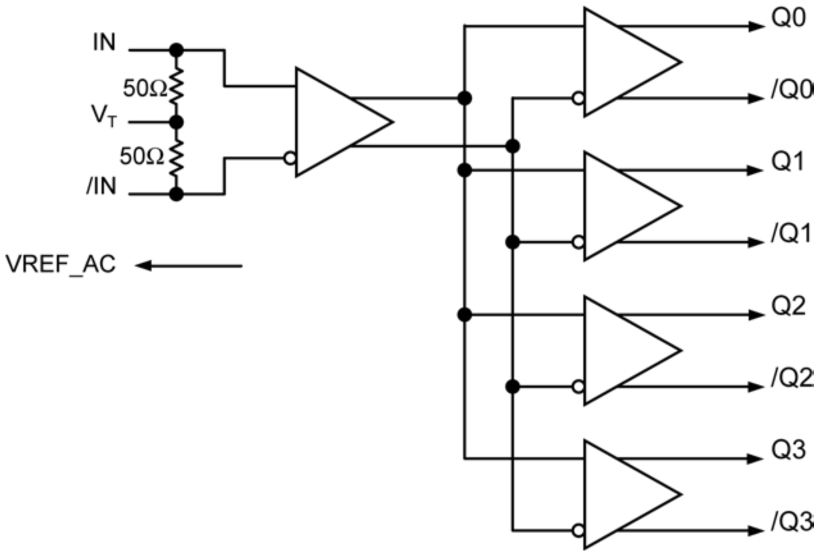


16-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
1, 4	IN, /IN	Differential Input: This input pair is the signal to be buffered. These inputs accept AC- or DC-coupled differential signals as small as 100mV (200mV$_{PP}$). Each pin of this pair internally terminates to a VT pin through 50Ω. Note that this input will default to an indeterminate state if left open. Please refer to the “Input Interface Applications” section for more details.
2	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to this pin. The VT pin provides a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section for more details.
8,13	VCC	Positive Power Supply. Bypass with 0.1µF||0.01µF low ESR capacitors as close to the VCC pin as possible.
15, 14 12, 11 10, 9 7, 6	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3	Differential 100K LVPECL Output: These LVPECL outputs are the precision, low skew copies of the input signal. Terminate with 50Ω to V_{CC}–2V. Unused output pairs may be left floating with no impact on jitter. See “Output Interface Applications” section.
5, 16	GND, Exposed Pad	Ground. Ground pin and exposed pad must be connected to the same ground plane.
3	VREF-AC	Reference Voltage: This output biases to V_{CC}–1.2V. It is used when AC coupling the inputs (IN, /IN). Connect V_{REF-AC} to the VT pin. Bypass VREF-AF pin with a 0.01µF low ESR capacitor to V_{CC}. Maximum sink/source capability is 1.5mA. See “Input Interface Applications” section for more details.

Functional Block Diagram



Absolute Maximum Ratings(1)

Supply Voltage (V_{CC})	–0.5V to +4.0V
Input Voltage (V_{IN})	–0.5V to V_{CC}
LVPECL Output Current (I_{OUT})	
Continuous	50mA
Surge	100mA
Termination Current(3)	
Source or sink current on V_T	±50mA
Input Current	
Source or sink current on IN, /IN	±50mA
VREF-AC Current(3)	
Source or sink current	±2mA
Lead Temperature (soldering, 20sec.)	+260°C
Storage Temperature (T_s)	–65°C to 150°C

Operating Ratings(2)

Supply Voltage (V_{CC})	+2.375V to +2.625V
	+3.0V to +3.6V
Ambient Temperature (T_A)	–40°C to +85°C
Package Thermal Resistance(4)	
QFN (θ_{JA})	
Still-Air	60°C/W
QFN (ψ_{JB})	
Junction-to-Board	38°C/W

DC Electrical Characteristics (5)

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		2.375	2.5	2.625	V
			3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}		55	78	mA
R_{DIFF_IN}	Differential Input Resistance (IN, /IN)		90	100	110	Ω
R_{IN}	Input Resistance (IN-to-V_T)		45	50	55	Ω
V_{IH}	Input High Voltage (IN, /IN)	Note 6	V_{CC} –1.6		V_{CC}	V
V_{IL}	Input Low Voltage (IN, /IN)		0		V_{IH} –0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing (IN, /IN)	See Figure 1b.	0.2			V
V_{T_IN}	IN-to-V_T				1.28	V

Notes:

1. Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability use for input of the same package only.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and ψ_{JB} are calculated based on a 4-layer board in still air, unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.\
6. V_{IH} (min) not lower than 1.2V.

LVPECL Outputs DC Electrical Characteristics(7)

V_{CC} = +2.5V ±5% or +3.3V ±10%; T_A = –40°C to + 85°C; R_L = 50Ω to V_{CC} –2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage Q, /Q		V_{CC}–1.145		V_{CC}–0.895	V
V_{OL}	Output LOW Voltage Q, /Q		V_{CC}–1.945		V_{CC}–1.695	V
V_{OUT}	Output Voltage Swing Q, /Q	See Figure 1a.	550	800		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing Q,/Q	See Figure 1b.	1100	1600		mV

Note:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics[8]

V_{CC} = +2.5V ±5% or +3.3V ±10%; T_A = –40°C to + 85°C, R_L = 50Ω to V_{CC}–2V, unless otherwise stated.

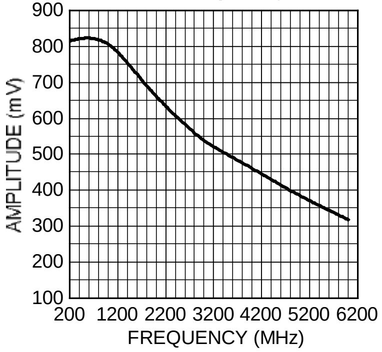
Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	Clock, V_{OUT} ≥ 400mV	2.0	3.5		GHz
		NRZ Data		2.5		Gbps
t_{pd}	Propagation Delay (IN-to-Q)	V_{IN} ≥ 100mV_{pk}	140	220	340	ps
t_{pd} Tempco	Differential Propagation Delay Temperature Coefficient			100		fs/°C
t_{SKEW}	Output-to-Output Skew	Note 9		4	20	ps
	Part-to-Part Skew	Note 10			150	ps
t_{Jitter}	Random Jitter (RJ) Deterministic Jitter (DJ)	Note 11 Note 12			1 10	ps_{RMS} ps_{PP}
	Cycle-to-Cycle Jitter Total Jitter	Note 13 Note 14			1 10	ps_{RMS} ps_{PP}
t_r, t_f	Output Rise/Fall Time (20% to 80%)	At full output swing.	50	100	180	ps

Notes:

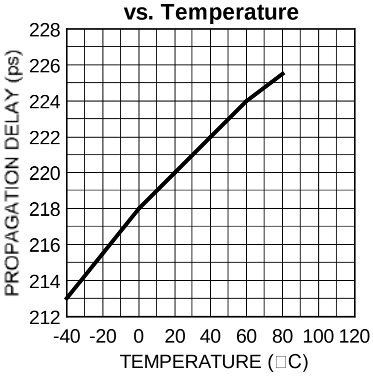
8. High-frequency AC-parameters are guaranteed by design and characterization.
9. Output-to-output skew is measured between outputs under identical conditions.
10. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs. Part-to-part skew includes variation in t_{pd}.
11. Random jitter is measured with a K28.7 character pattern, measured at 2.5Gbps.
12. DJ is measured at 2.5Gbps, with both K28.5 and 2^{23} – 1 PRBS pattern.
13. Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles, T_n – T_{n-1} where T is the time between rising edges of the output signal.
14. Total jitter definition: with an ideal clock input of frequency <f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

Typical Operating Characteristics

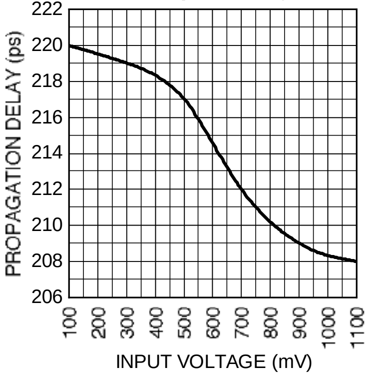
V_{CC} = 2.5V, V_{IN} = 100mV_{pk}, T_A = 25°C, unless otherwise stated.



Amplitude vs. Frequency



Propagation Delay vs. Temperature

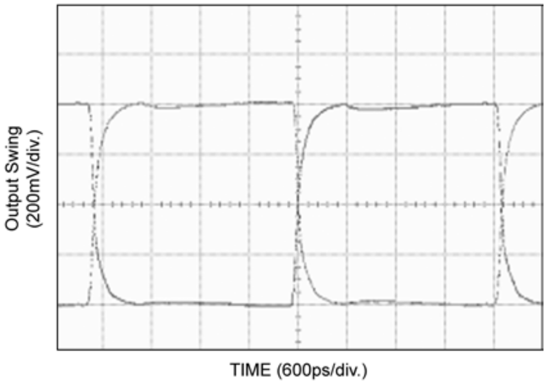


Propagation Delay vs. Input Voltage

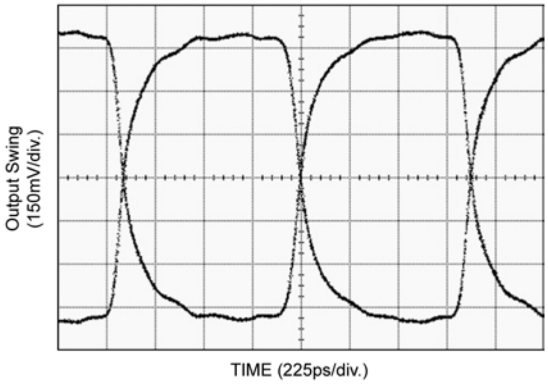
Functional Characteristics

V_{CC} = 2.5V, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.

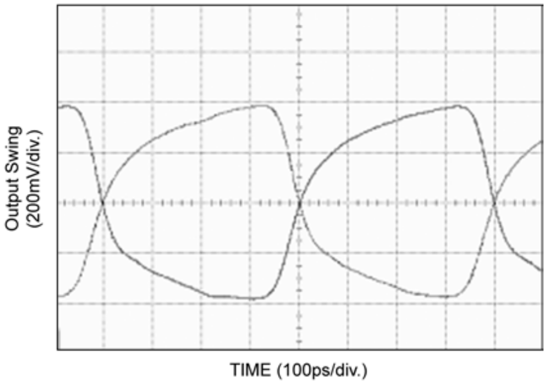
200MHz (Q - /Q)



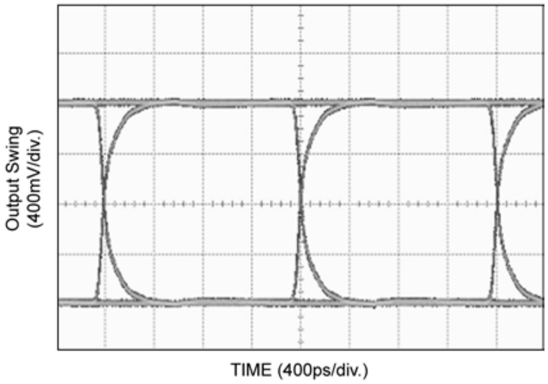
622MHz (Q - /Q)



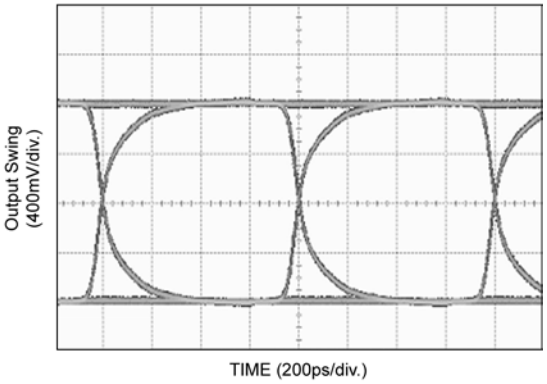
1.25GHz (Q - /Q)



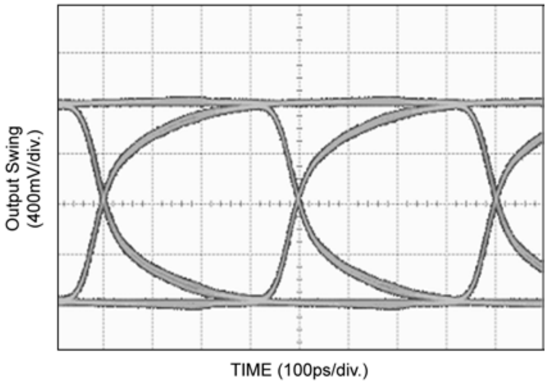
622Mbps (Q - /Q)



1.25Gbps (Q - /Q)



2.5Gbps (Q - /Q)



Single-Ended and Differential Swings

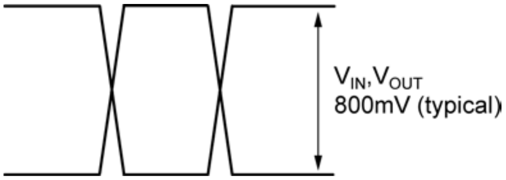


Figure 1a. Singled-Ended Voltage Swing

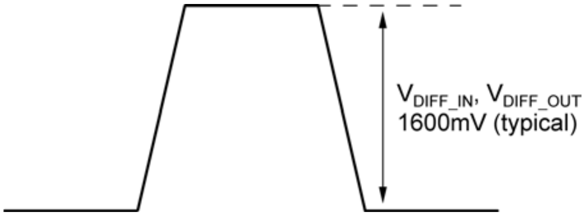
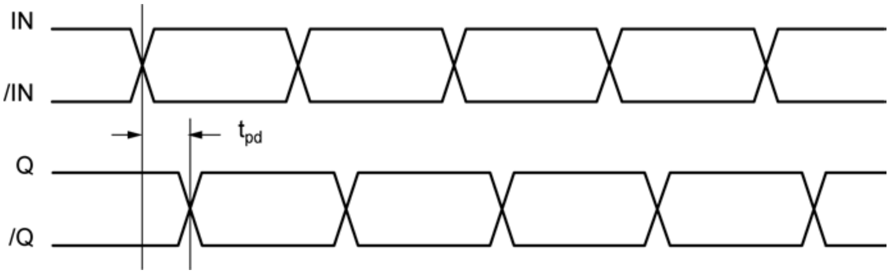


Figure1b. Differential Voltage Swing

Timing Diagrams



Input and Output Stages

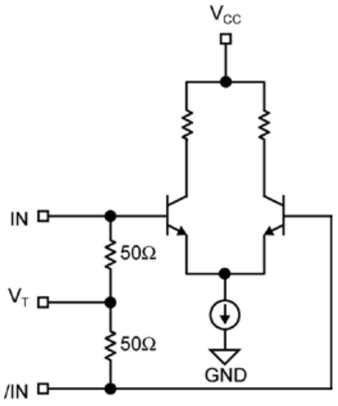


Figure 2a. Simplified Differential Input Stage

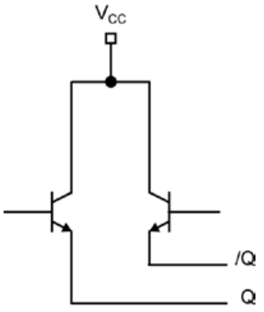
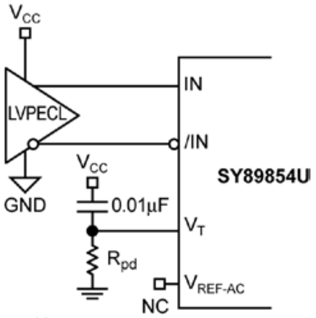


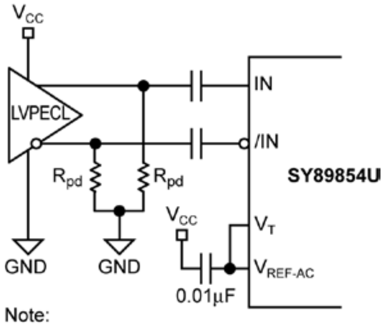
Figure 2b. Simplified LVPECL Output Stage

Input Interface Applications



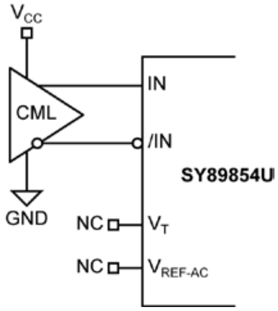
Note:
For 3.3V, R_{pd} = 50Ω.
For 2.5V, R_{pd} = 19Ω.

3a. LVPECL Interface (DC-Coupled)



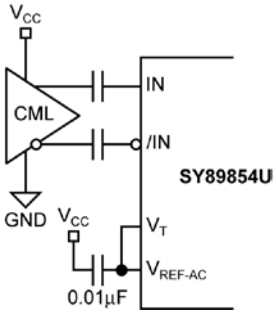
Note:
For 3.3V, R_{pd} = 100Ω.
For 2.5V, R_{pd} = 50Ω.

3b. LVPECL Interface (AC-Coupled)

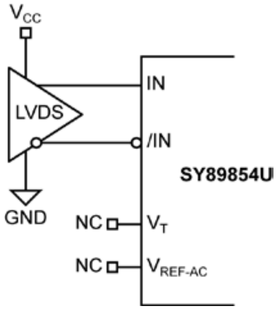


Option: may connect V_T to V_{CC}

3c. CML Interface (DC-Coupled)

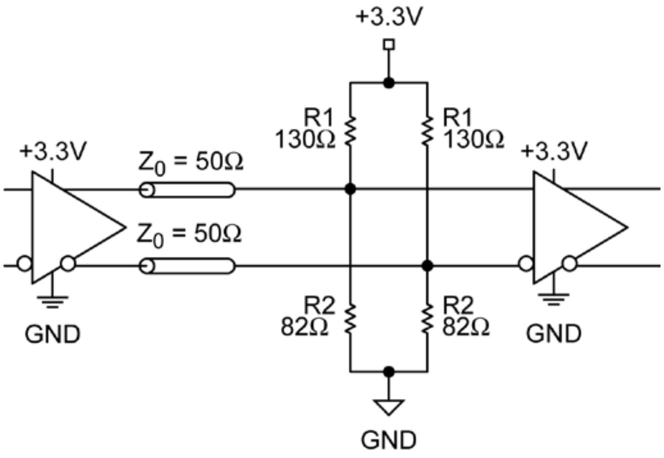


3d. CML Interface (AC-Coupled)



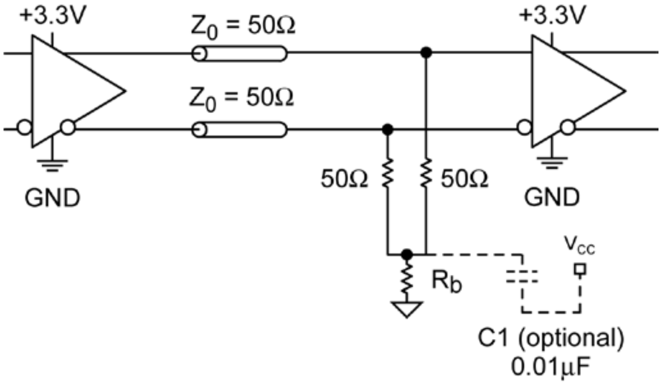
3e. LVDS Interface

Output Interface Applications



Note:
For +2.5V systems, R1 = 250Ω, R2 = 82.5Ω

Figure 4a. Parallel Thevenin-Equivalent Termination



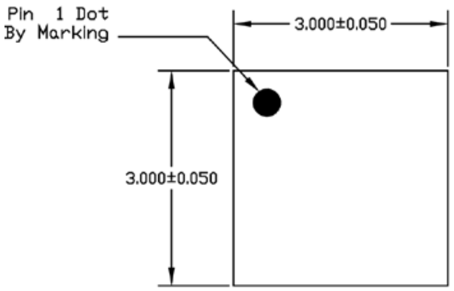
Note:
For +2.5V systems, Rb = 19Ω
For +3.3V systems, Rb = 50Ω

Figure 4b. Parallel Termination (3-Resistor)

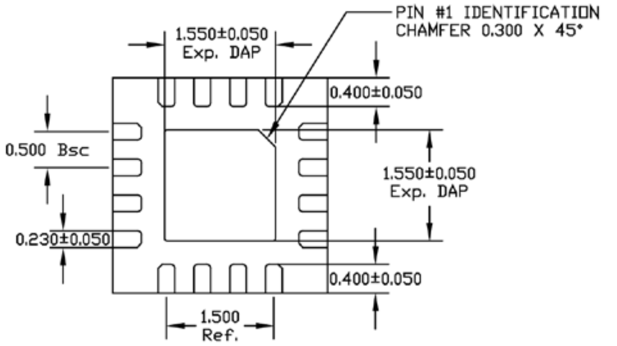
Related Product and Support Documentation

Part Number	Function	Data Sheet Link
SY58021U	4GHz, 1:4 LVPECL Fanout Buffer/Translator with Internal Termination	www.micrel.com/product-info/products/sy58021u.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

16-Pin QFN

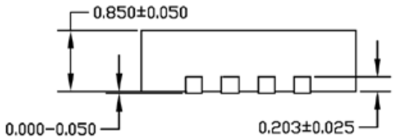


TOP VIEW



BOTTOM VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



SIDE VIEW

Package Notes:

(1) Package meets Level 2 Moisture Sensitivity Classification.
(2) All parts are dry-packaged before shipment.
(3) Exposed pad must be soldered to a ground for proper thermal management.

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