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1 Overview

STA8088FG is a highly integrated System-On-Chip device designed for positioning systems applications.

The low power consumption and minimum BOM make STA8088FG the ideal solution for low-cost and battery-operated portable products such handheld, computers, cameras, data loggers and sports accessories, as well as automotive application.

It combines a high performance ARM946 microprocessor with embedded enhanced peripherals and I/O capabilities with ST next generation triple-constellation positioning engine. The RF front-end and base band processor are able to support GPS/Galileo and Glonass navigation systems. The device is offered with a complete firmware which performs all positioning operations including tracking, acquisition, navigation and data output with no need of external memories.

It also provides clock generation via PLL, backup logic with real time clock and it supports USB2.0 standard at full speed, (12 Mbps) with on-chip PHY.

STA8088FG is software compatible with the ARM processor family. The device is power supplied with 1.8V and uses three on-chip voltage regulators to internally supply the RF front-end, core logic and the backup logic. In order to reduce the power consumption the chip can be directly powered with 1.2 V bypassing the embedded voltage regulators which will be put in power down mode.

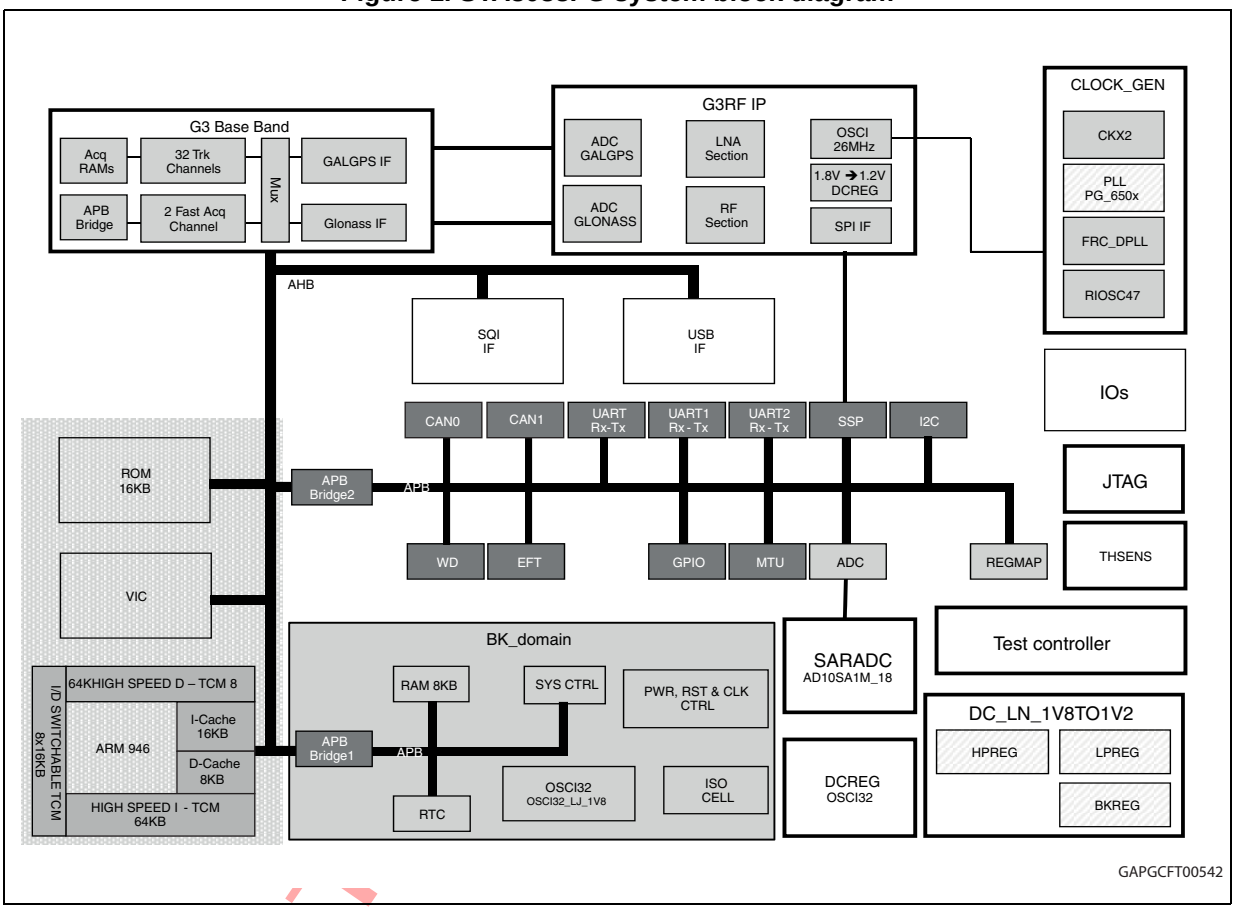
I/O lines are compatible with 1.8 V and 3.3 V.

The chip, using STMicroelectronics CMOSRF Technology, is housed in a VFQFPN-56 (7 x 7 x 0.85 mm) package with stacked 16 Mbit Flash memory.

2 Pin description

2.1 Block diagram

Figure 1. STA8088FG system block diagram



2.2 VFQFPN56 pin configuration

Figure 2. VFQFPN56 connection diagram - with CAN (bottom view)

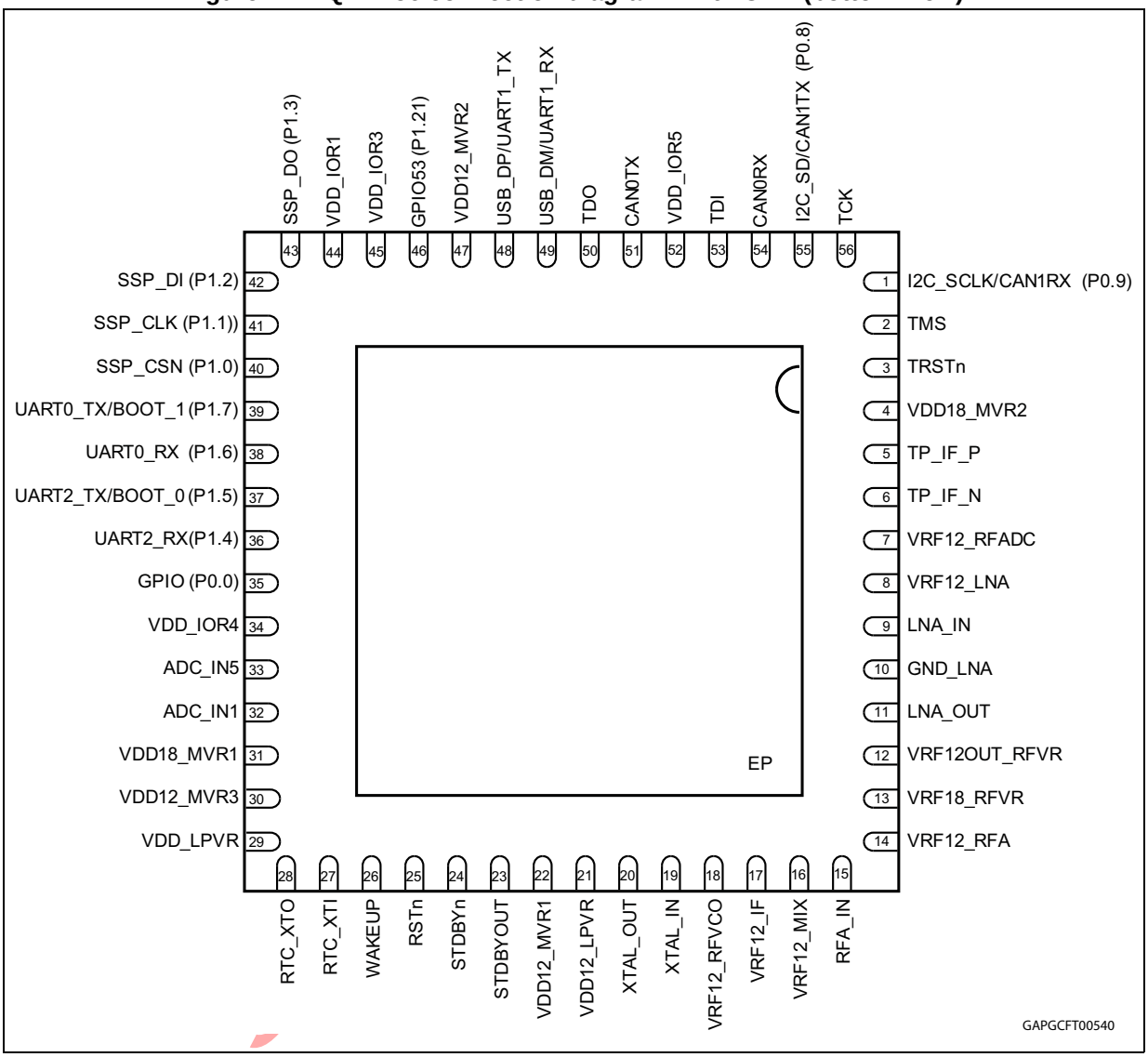
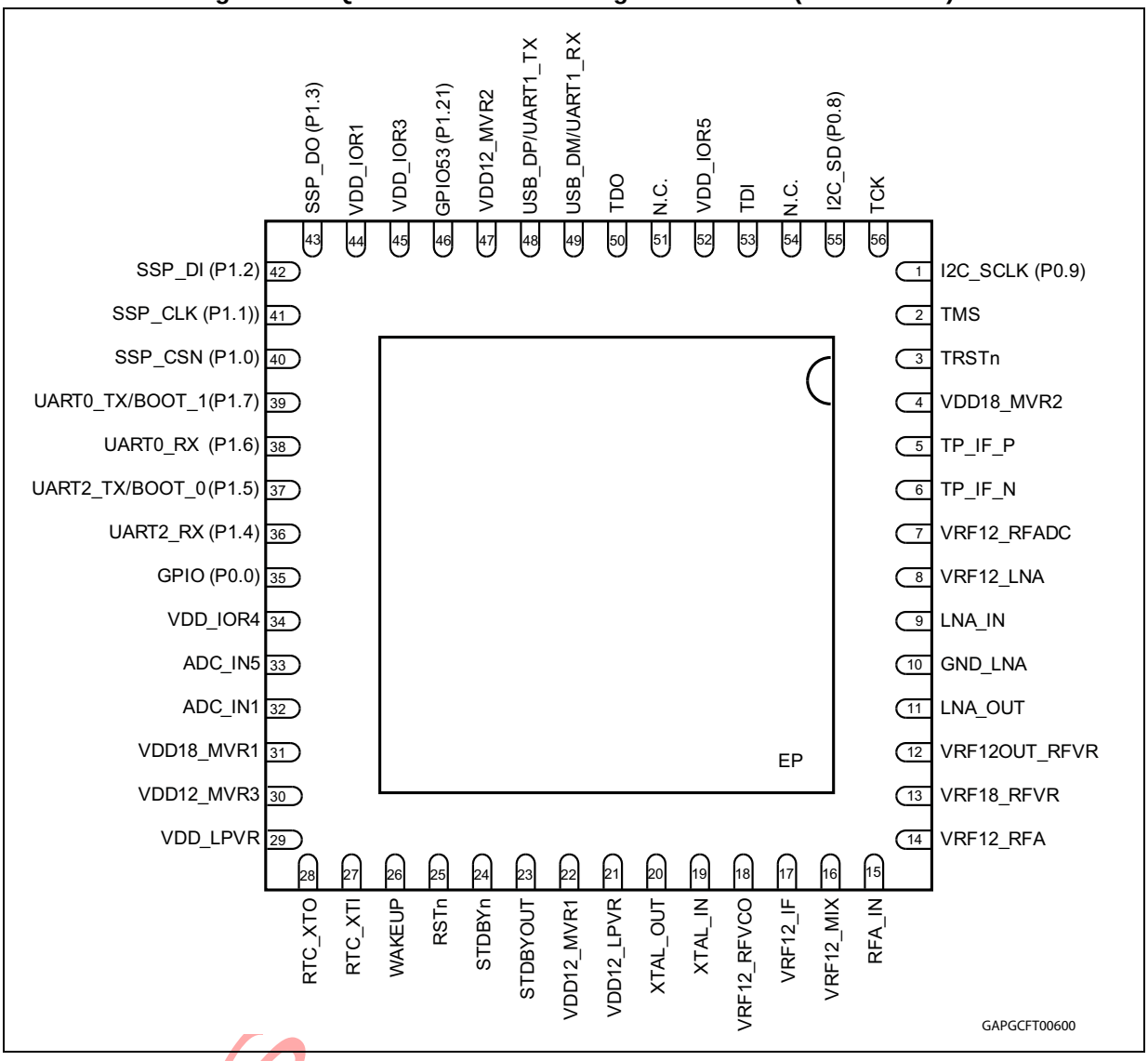


Figure 3. VFQFPN56 connection diagram - no CAN (bottom view)



2.3 Power supply pins

Table 1. Power supply pins

Symbol	I/O	Functions	VFQFPN56
VDD18_MVR[1,2]	Pwr	Digital supply voltage for main voltage regulator (1.8 V)	31,4
VDD12_MVR[1,2,3]	Pwr	Digital supply voltage for core circuitry (1.2 V). When using the MVR, this pin shall not be driven by an external voltage supply, but a capacitance shall be connected between these pins and GND to guarantee on-chip voltage stability.	22,47,30
VDD_LPVR	Pwr	Digital supply voltage for low power voltage regulator (1.62 - 3.6 V)	29

Table 1. Power supply pins (continued)

Symbol	I/O	Functions	VFQFN56
VDD12_LPVR	Pwr	Digital supply voltage for backup logic (1.2 V). When using the LPVR, this pin shall not be driven by an external voltage supply, but a capacitance shall be connected between these pins and GND to guarantee on-chip voltage stability.	21
VDD_IOR1	Pwr	Digital supply voltage for I/O ring 1 (1.8 or 3.3 V)	44
VDD_IOR3	Pwr	Digital supply voltage for I/O ring 3 (1.8 V)	45
VDD_IOR4	Pwr	Digital supply voltage for I/O ring 4 (1.8 V)	34
VDD_IOR5	Pwr	Digital supply voltage for I/O ring 5 (3.3 V)	52
VRF18_RFVR	Pwr	Analog supply voltage for RF voltage regulator (1.8 V)	13
VRF12OUT_RFVR	Pwr	RF voltage regulator 1.2 V output	12
VRF12_LNA	Pwr	Analog supply voltage for LNA (1.2 V)	8
VRF12_RFA	Pwr	Analog supply voltage for RFA (1.2 V)	14
VRF12_MIX	Pwr	Analog supply voltage for Mixer (1.2 V)	16
VRF12_IF	Pwr	Analog supply voltage for IF (1.2 V)	17
VRF12_RFVCO	Pwr	Analog supply voltage for VCO (1.2 V)	18
VRF12_RFADC	Pwr	Analog supply voltage for RF ADC (1.2 V)	7
GND_LNA	GND	Analog supply ground for LNA	10
GND	GND	Analog and digital supply ground	EP

2.4 Main function pins

Table 2. Main function pins

Symbol	I/O voltage	I/O	Functions	VFQFPN56
STDBYn	1.2V	I	When low, the chip is forced in Standby Mode - All pins in high impedance except the ones powered by Backup supply	24
STDBYOUT	1.2V	O	When low, indicates the chip is in Standby Mode.	23
RSTn(1)	1.2V	I	Reset Input with Schmitt-Trigger characteristics and noise filter.	25
WAKEUP(2)	1.2V	I	WAKEUP from STANDBY mode	26
RTC_XTI	1.5V (Max)	I	Input of the 32 KHz oscillator amplifier circuit and input of the internal real time clock circuit.	27
RTC_XTO	1.5V (Max)	O	Output of the oscillator amplifier circuit.	28
ADC_IN[1,5]	1.4V – 0 Typ Range	I	ADC Analog input [1,5]	32,33
USB_DP/UART1_TX	VDD_IOR5	USB/O	USB D+ signal / UART 1 Tx data	48
USB_DM/UART1_RX	VDD_IOR5	USB/I	USB D- signal / UART 1 Rx data	49

Table 2. Main function pins (continued)

Symbol	I/O voltage	I/O	Functions	VFQFPN56
CAN0TX(3)	VDD_IOR5	O	CAN0 - transmit data output	51
CAN0RX(3)	VDD_IOR5	I	CAN0 - receive data input	54

1. When RSTn is de-asserted, pin WAKEUP must be low.
2. The WAKEUP pulse must be longer than 500 µs.
3. Only for STA8088FGB (see *Figure 9: Ordering information scheme*).

2.5 Test/emulated dedicated pins

Table 3. Test/emulated dedicated pins

Symbol	I/O voltage	I/O	Functions	VFQFPN56
TDO	VDD_IOR5	O	JTAG test data out	50
TDI	VDD_IOR5	I	JTAG test data in	53
TCK	VDD_IOR5	I	JTAG test clock	56
TMS	VDD_IOR5	I	JTAG test mode select	2
TRSTn(1)	VDD_IOR5	I	JTAG test circuit reset	3
TP_IF_P	VRF12_IF	O	Diff. test point for IF – positive	5
TP_IF_N	VRF12_IF	O	Diff. test point for IF – negative	6

1. If JTAG interface is not used, pin TRSTn must be asserted low.

2.6 RF front-end pins

Table 4. RF front-end pins

Symbol	I/O voltage	I/O	Functions	VFQFPN56
LNA_IN	VRF12_LNA	I	Low noise amplifier input	9
LNA_OUT	VRF12_LNA	O	Low noise amplifier output	11
RFA_IN	VRF12_RFA	I	RF amplifier input	15
XTAL_In	VRF12_RFDig	I	Input side of crystal oscillator or TCXO input	19
XTAL_Out	VRF12_RFDig	O	Output side of crystal oscillator	20

2.7 Port 0 pins

Port 0 consists of a 32-bit bidirectional I/O port (only 3-bit are used in STA8088FG).

It can be either used as general purpose Input or Output port, or configured according to the associated alternate functions.

Table 5. Port 0 pins

Symbol	I/O voltage	I/O	Mode	Functions	VFQFPN56
P0.0	VDD_IOR1	IO	Default	GPIO.0: General Purpose IO	35
		I	A	PPS_IN: Pulse Per Second Input	
		O	B	PPS_OUT: Pulse Per Second Output	
		O	C	SSP_CSN: SSP Chip Select Active Low	
P0.8	VDD_IOR5	O	Default	CAN1TX(1): CAN1 Transmit Data Output	55
		IO	A	GPIO.8: General Purpose IO	
		IO	B	I2C_SD: I2C Serial Data	
P0.9	VDD_IOR5	I	Default	CAN1RX(1): CAN 1 Receive Data Input	1
		IO	A	GPIO.9: General Purpose IO	
		O	B	I2C_SCLK: I2C Clock	

1. Only for STA8088FGB (see *Figure 9: Ordering information scheme*).

2.8 Port 1 pins

Port 1 consists of a 32-bit bidirectional I/O port (only9-bit are used in STA8088FG).

It can be either used as general purpose Input or Output port, or configured according to the associated alternate functions.

Table 6. Port 1 pins

Symbol	I/O Voltage	I/O	Mode	Functions	VFQFPN56
P1.0	VDD_IOR1	O	Default	SSP_CSN/IOPWRSEL_R1: SSP chip select active low / I/O Ring 1 power selection	40
		I/O	A	GPIO32: general purpose I/O	
		I/O	B	SIGNGGPS: GGPS 3-bit coding output (sign)	
		O	C	SQI_CEN: SQI Flash chip enable	
P1.1	VDD_IOR1	I/O	Default	SSP_CLK: SSP clock	41
		I/O	A	GPIO33: general purpose I/O	
		I/O	B	CLOCK_GGPS: GGPS clock out	
		O	C	SQI_CLK: SQI Flash clock	
P1.2	VDD_IOR1	I	Default	SSP_DI: SSP serial data input	42
		I/O	A	GPIO34: general purpose I/O	
		I/O	B	SIGNGNS: GNS 3-bit coding output (sign)	
		IO	C	SQI_SIO0/SI: SQI Flash data I/O 0 / serial I	

Table 6. Port 1 pins (continued)

Symbol	I/O Voltage	I/O	Mode	Functions	VFQFPN56
P1.3	VDD_IOR1	O	Default	SSP_DO: SSP serial data output	43
		I/O	A	GPIO35: general purpose I/O	
		I/O	B	CLOCK_GNS: GNS clock out	
		IO	C	SQI_SIO1/SO: SQI Flash data I/O 1 / serial O	
P1.4	VDD_IOR1	I	Default	UART2_RX: UART 2 Rx data	36
		I/O	A	GPIO36: general purpose I/O	
P1.5	VDD_IOR1	I/O	Default	UART2_TX / BOOT_0: UART 2 Tx data / ARM Boot 0	37
		I/O	A	GPIO37: general purpose I/O	
P1.6	VDD_IOR1	I	Default	UART0_RX: UART 0 Rx data	38
		I/O	A	GPIO38: general purpose I/O	
		I/O	C	SQI_SIO2: SQI Flash data I/O 2	
P1.7	VDD_IOR1	I/O	Default	UART0_TX / BOOT_1: UART 0 Tx data / ARM Boot 1	39
		I/O	A	GPIO39: general purpose I/O	
		I/O	C	SQI_SIO3: SQI Flash data I/O 3	
P1.21	VDD_IOR3	I/O	A	GPIO53: general purpose I/O	46

2.9 Pin terminal characteristics

Table 7. Pin terminal characteristics

Name	Type(1)	Ring	Pull Up/ Pull Down	Behavior under reset (RSTn is low)	Comment
Power, reset and clock					
RSTn	IN	R0	NO	Low	Input only
STDBYn	IN	R0	NO	High	Input only
WAKEUP	IN	R0	NO	Low(2)	Input only
STDBY_OUT	OUT(3)	R0	HW controlled	Pull-up	Output buffer is disabled and pull-up is enabled until internal filtered reset is high
PPS_OUT	OUT(3)	R1	HW controlled	Pull-down	Output buffer is disabled and pull-down is enabled until internal filtered reset is high
RTC_XTI	ANA	VDD_LPVR			
RTC_XTO	ANA	VDD_LPVR			
RF Front End					
LNA_IN	ANA				

Table 7. Pin terminal characteristics (continued)

Name	Type(1)	Ring	Pull Up/ Pull Down	Behavior under reset (RSTn is low)	Comment
LNA_OUT	ANA				
RFA_IN	ANA				
XTAL_In	ANA				
XTAL_Out	ANA				
ADC					
ADC_IN1	ANA	VDD18_MVR			
ADC_IN5	ANA	VDD18_MVR			
USB/UART1					
USB_DM/ UART1_TX	USB	R5	NO		Refer to USB specifications
USB_DP/ UART1_RX	USB		NO		
UART0					
UART0_TX/ BOOT_1	INOUT	R1	HW/SW controlled	Pull-down	Output buffer is disabled and pull-down is enabled until internal filtered reset is high. When port is configured as GPIO the pull-up / pull-down feature is controlled by GPIO register. Default register map is controlled by the value latched on this pin at rising edge of RSTn. Application may pull-up this pin with external resistance
UART0_RX	INOUT	R1	HW/SW controlled	Pull-down	Output buffer is disabled and pull-down is enabled until internal filtered reset is high. When port is configured as GPIO the pull-up / pull-down feature is controlled by GPIO register
UART2					
UART2_TX/ BOOT_0	INOUT	R1	HW/SW controlled	Pull-down	Output buffer is disabled and pull-down is enabled until internal filtered reset is high. When port is configured as GPIO the pull-up / pull-down feature is controlled by GPIO register. Default register map is controlled by the value latched on this pin by wakeup edge. Application may pull-up this pin with external resistance
UART2_RX	INOUT	R1	HW/SW controlled	Pull-down	Output buffer is disabled and pull-down is enabled until internal filtered reset is high. When port is configured as GPIO the pull-up / pull-down feature is controlled by GPIO register.

Table 7. Pin terminal characteristics (continued)

Name	Type(1)	Ring	Pull Up/ Pull Down	Behavior under reset (RSTn is low)	Comment
SSP					
SSP_CSN/ IOPWRSEL_R1	INOUT	R1	HW/SW controlled	Pull-down	Output buffer is disabled and pull-down is enabled until internal filtered reset is high. When port is configured as GPIO the pull-up / pull-down feature is controlled by GPIO register. If VDD_IOR1 is 3.3V this pin should be pulled-up by external resistance so that it is latched high by wakeup edge
SSP_CLK	INOUT	R1	HW/SW controlled	Pull-down	Output buffer is disabled and pull-down is enabled until internal filtered reset is high. When port is configured as GPIO the pull-up / pull-down feature is controlled by GPIO register
SSP_DI	INOUT	R1			
SSP_DO	INOUT	R1			
CAN0					
CAN0TX	OUT(3)	R5	HW controlled	Pull-down	Output buffer is disabled and pull-down is enabled until internal filtered reset is high
CAN0RX	IN				
CAN1					
CAN1TX	INOUT	R5	HW/SW controlled	Pull-down	Output buffer is disabled and pull-down is enabled until internal filtered reset is high. When port is configured as GPIO the pull-up / pull-down feature is controlled by GPIO register
CAN1RX	INOUT				
GPIO					
GPIO0	INOUT	R1	HW/SW controlled	Pull-down	Output buffer is disabled and pull-down is enabled until internal filtered reset is high. When port is configured as GPIO the pull-up / pull-down feature is controlled by GPIO register
GPIO53	INOUT	R3			
Test					
TCK	IN	R5	NO		
TDI	IN	R5	NO		
TDO	OUT(3)	R5	HW controlled	Pull-down	Output buffer is disabled and pull-down is enabled until internal filtered reset is high
TMS	IN	R5	NO		
TRSTn	IN	R5	NO		
TP_IF_P	ANA				
TP_IF_N	ANA				

1. OUT buffers driving capability is 8 mA.

2. WAKEUP pin must be low when RSTn pin is deasserted (WAKEUP pin high and RSTn pin deasserted is allowed as reserved configuration).
3. Output buffer is disabled when RSTn pin is low.

3 General description

3.1 RF front end

The RF front-end is able to down-convert both the GPS-GALILEO signal from 1575.42 MHz to 4.092 MHz (4 Fo, being F0 = 1.023 MHz) and GLONASS signal from 1601.718 MHz to 8.57 MHz.

It embeds high performance LNA minimizing external component count and two LDOs to supply the internal core facilitating requirements for external power supply. A three bits ADC converts the IF signals to sign (SIGN) and magnitude (MAG0 and MAG1). They can be sampled or not by SPI. The magnitude bits are internally integrated in order to control the variable gain amplifiers. The VGA gain can be also set by the SPI interface.

The RF tuner accepts a wide range of reference clocks (10 to 52 MHz) and can generate 16 Fo, 32 Fo, 48 Fo and 64 Fo sampling clock (GALGPS_CLK and GNS_CLK) for the baseband.

3.2 GPS/Galileo/Glonass Base Band (G3BB) processor

TeseoII integrates G3BB proprietary IP, which is the ST last generation high-sensitivity Baseband processor fully compliant with GPS, Galileo and Glonass systems. Please refer to GPS solution specification and release notes for more details.

The Base Band receives, from the embedded RF Front-End, two separate IF signals coded in sign-magnitude digital format on 3 bits and the related clocks. The Galileo/GPS (GALGPS) and Glonass (GNS) signals at the base band inputs are centered on 4.092 MHz and 8.57 MHz respectively.

The baseband processes the two IF signals performing data codification, sample rate conversion and final frequency conversion to zero IF before acquisition and tracking correlations.

The base band processor has the capability of acquire and track the Galileo, GPS and Glonass signals in a simultaneous or single way, or a combination of the three. The number of tracking channels to be used is programmable; the not used tracking channels can be powered down.

A complete multi-OS software library is provided by ST to handle GPS processing, managing satellite acquisition, tracking, pseudo-range calculation and positioning, generating the output in the standard NMEA message format. The library includes support of ST self-trained assisted GPS (ST-AGPS), a complete and scalable solution for assisting GPS start-up with autonomous and server-based ephemeris prediction and extension.

3.3 MCU Subsystem

The implemented sub-system includes an AHB Lite bus matrix.

An ARM946 core is embedded in the sub-system and masters the AHB bus. The totally available TCM SRAM is 256 KB. The amount of memory on ITCM and DTCM can be configured by the ARM946 (see TCM Configuration Table below). ITCM can be configured as 64 + Ni x 16 KB; DTCM can be configured as 64 + Nd x 16 KB, where Ni + Nd = 8, Ni ≥ 1.

Figure 4. TCM Configuration

TCMcfg [2]	TCMcfg [1]	TCMcfg [0]	ITCM	DTCM
0	0	0	80KB	176KB
0	0	1	96KB	160KB
0	1	0	112KB	144KB
0	1	1	128KB	128KB
1	0	0	144KB	112KB
1	0	1	160KB	96KB
1	1	0	176KB	80KB
1	1	1	190KB	64KB

3.3.1 AHB slaves

- G3 APB port that allows to interface with the G3BB acquisition memory and control registers.
- 16 Kbytes ROM
- Vectored Interrupt Controller (VIC).
- SQI flash memory controller
- 2 x ARM946 APB peripheral bus (APB1, APB2).

Vectored Interrupt Controller (VIC)

This Vectored Interrupt Controller (VIC) allows the operative system interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts. It provides a software interface to the interrupt system. There are up to 32 interrupt lines. The VIC uses a bit position for each different interrupt source.

The software can control each request line to generate software interrupts. Each interrupt line can be independently enabled and configured to trigger a non-vectored Normal Interrupt Request (IRQ) or Fast Interrupt Request (FIQ) to the ARM946 CPU. Sixteen interrupt lines can also be selected to trigger a vectored IRQ.

The VIC has two operation modes: the user mode and the privilege mode, in order to have the possibility to set (or not) one level of protection during execution.

FS USB dual role controller

Full speed USB dual role with transceiver. It can work as a FS USB device if connected to a USB HOST or it can work as a USB HOST when connected to a USB device. It is an AHB slave. When active requires a 48MHz clock USB_CLK.

3.4 APB peripherals

3.4.1 CAN

The 2 CAN[(a)] cores perform communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1 MBit/s. For the connection to the physical layer, additional transceiver hardware is required.

CAN consists of the CAN core, message RAM, message handler, control registers and module. For communication on a CAN network, individual message objects are configured. The message objects and identifier masks for acceptance filtering of received messages are stored in the message RAM. All functions concerning the handling of messages are implemented in the message handler. These functions include acceptance filtering, the transfer of messages between the CAN core and the message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the CAN can be accessed directly by the CPU through the module interface. These registers are used to control/configure the CAN core and the message handler and to access the message RAM.

CAN features

- Supports CAN protocol version 2.0 part A and B
- Bit rates up to 1 MBit/s
- Each message object has its own identifier mask
- Programmable FIFO mode (concatenation of message objects)
- Maskable interrupt
- Disabled automatic re-transmission mode for time triggered CAN applications
- Programmable loop-back mode for self-test operation
- 8-bit non-multiplex Motorola HC08 compatible module interface
- Two 16-bit module interfaces to the AMBA APB bus from ARM

3.4.2 SSP

The SSP is a master or slave interface for synchronous serial communication with peripheral devices that have either Motorola SPI, National Semiconductor MicroWire or Texas Instruments Synchronous Serial Interfaces.

The SSP performs serial-to-parallel conversion on data received from a peripheral device on SSPRXD pin, and parallel-to-serial conversion on data written by CPU for transmission on SSPTXD pin. The transmit and receive paths are buffered with internal FIFO memories allowing up to 32 x 32-bit values to be stored independently in both transmit and receive modes. FIFOs may be burst-loaded or emptied by the system processor or DMA, from one to eight words per transfer. Each 32-bit word from the system fills one entry in FIFO.

The SSP includes a programmable bit rate clock divider and prescaler to generate the serial output clock SSPCLK from the on-chip clock, SSPCLKI. One combined interrupt is delivered, which is asserted from several internal maskable events.

a. Only for STA8088FGB (see *Figure 9: Ordering information scheme*).

SSP features

In both master and slave configurations, the SSP has the following features:

- Parallel-to-serial conversion on data written to an internal 32-bit wide, 32-location deep
- transmit FIFO
- Serial-to-parallel conversion on received data, buffering it in a 32-bit wide, 32-location
- deep receive FIFO
- Programmable data frame size from 4 to 32 bits,
- Programmable clock bit rate and prescaler
- Programmable clock phase and polarity in SPI mode

3.4.3 UART

The UARTx (x = 0|1|1) performs serial-to-parallel conversion on data asynchronously received from a peripheral device on URXDx pin, and parallel-to-serial conversion on data written by CPU for transmission on UTXDx pin. The transmit and receive paths are buffered with internal FIFO memories allowing up to 64 data byte for transmission, and 64 data byte with 4-bit status (break, frame, parity, and overrun) for receive.

UART features

The UARTx (x = 0|1|2) are Universal Asynchronous Receiver/Transmitter that support much of the functionality of the industry-standard 16C650 UART. The main features are:

- Programmable baud rates up to UARTCLK / 16 (3.0 Mbps with UARTCLK at 48 MHz), or up to UARTCLK / 8 (6.0 Mbps with UARTCLK at 48 MHz), with fractional baud-rate generator
- 5, 6, 7 or 8 bits of data
- Even, odd, stick or no-parity bit generation and detection
- 1 or 2 stop bit generation
- Automatic extraction of UART setting for baud rate, character size (7 or 8-bit), parity configuration and number of stop bits
- Support of the modem control functions CTS, RTS (UART0 and UART1), plus DCD, DSR, RTS, DTS and RI (UART0 only)
- Support of software flow control using programmable Xon/Xoff characters
- False start bit detection
- Line break generation and detection
- Separate 8-bit wide, 64-deep transmit FIFO and 12-bit wide, 64-deep receive FIFO
- Programmable FIFO disabling for 1-byte depth data path

These UARTs vary from industry-standard 16C650 on some minor points which are:

- Receive FIFO trigger levels
- The internal register map address space, and the bit function of each register differ
- The deltas of the modem status signals are not available
- 1.5 stop bits is not supported
- Independent receive clock feature is not supported

3.4.4 Flash

The STA8088FG integrates 16Mbits of Flash Memory. This eliminates the need external Flash simplifying the routing associated to integrate a GPS receiver into a customer board.

3.4.5 MTU

The Multi Timer Unit provides access to four interrupt generating programmable 32-bit Free-Running decrementing Counters (FRCs). The FRCs have their own clock input, allowing the counters to run from a much slower clock than the system clock.

The FRC is the part of the timer that performs the counting. There are four instantiations of the FRC block in the MTU, allowing four counts to be performed in parallel. The 32-bit counter in the FRC is split up into two 16-bit counters.

3.4.6 WDT

Watchdog Timer (WDT) provides a way of recovering from software crashes. The watchdog clock is used to generate a regular interrupt (WDOGINT), depending on a programmed value.

The watchdog monitors the interrupt and asserts a reset signal (WDOGRES) if the interrupt remains unserviced for the entire programmed period. You can enable or disable the watchdog unit as required.

The WDT is counting down at a fixed frequency of 32.768 kHz, in NORMAL, SLOW and DOZE modes, but is stopped in SLEEP modes.

Note: Watchdog is stalled when the ARM processor is in Debug mode.

3.4.7 GPIO

The GPIO block provides sixteen (16) programmable inputs or outputs. Each input or output can be controlled in two modes:

- software mode through an APB bus interface
- alternate mode, where GPIO becomes a peripheral input or output line

Any GPIO input can be independently enabled or disabled (masked) for interrupt generation. User can select for each GPIO which edge (rising, falling, both) will trigger an interrupt.

3.4.8 ADC

10 bit SAR ADC operating at1.8V analog supply. It can convert up to 2 single ended channels with analog input multiplexer at 500KSPS

3.4.9 RTC

This is an always-on power domain dedicated to RTC logic (backup system) with 8Kbyte SRAM and supplied with a dedicated voltage regulator.

The RTC provides a high resolution clock which can be used for GPS. It keeps the time when the system is inactive and can be used to wake the system up when a programmed alarm time is reached. It has a clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

RTC features

- 48-bit counter clocked by 32768 kHz clock
- 32-bit for the integer part (seconds) and 16-bit for the fractional part
- The integer part and the fractional part are readable independently
- The counter, once enabled, can be stopped
- Integer part load register (32-bit)
- Fractional part load register (16-bit)
- Load bit to transfer the content of the entire load register (integer+fractional part) to the 48-bit counter. Once set by the MCU this bits is cleared by the hardware to signal to the MCU that the RTC has been updated.

4 Electrical characteristics

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to GND.

4.2 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25°C.

4.3 Typical values

Unless otherwise specified, typical data are based on T_A = 25°C, V_{ddio} = 1.8 V, V_{dd} = 1.20 V. They are given only as design guidelines and are not tested.

4.4 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.5 Absolute maximum ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advisable to take normal precautions to avoid application of any voltage higher than the specified maximum rated voltages.

Table 8 lists the absolute maximum rating for STA8088FG.

Table 8. Voltage characteristics

Symbol	Parameter	Min.	Max.	Unit
V_{DD12_LPVR}	Power supply filter pins for the core logic and buffers of the always on section	V_{GND} - 0.3	V_{GND} + 1.32	V
V_{DDIO_r1}	Power supply pins for the IO buffers	V_{GNDIO} - 0.3	V_{GNDIO} + 3.63	V
V_{DDIO_r2}		V_{GNDIO} - 0.3	V_{GNDIO} + 3.63	V
V_{DDIO_r3}		V_{GNDIO} - 0.3	V_{GNDIO} + 3.63	V
V_{DDIO_r4}		V_{GNDIO} - 0.3	V_{GNDIO} + 3.63	V
V_{DDIO_r5}		V_{GNDIO} - 0.3	V_{GNDIO} + 3.63	V
V_{DD12_MVR}	Power supply filtering pins for the core logic in the switchable section	V_{GND} - 0.3	V_{GND} + 1.32	V
V_{RF12_LNA}	Analog supply voltage for LNA.	V_{GND_LNA} - 0.3	V_{GND_LNA} + 1.32	V
V_{RF12_RFA}	Analog supply voltage for RFA.	V_{GND_RF} - 0.3	V_{GND_RF} + 1.32	V
V_{RF12_MIX}	Analog supply voltage for mixer	V_{GND_RF} - 0.3	V_{GND_RF} + 1.32	V
V_{RF12_IF}	Analog supply voltage for IF section	V_{GND_RF} - 0.3	V_{GND_RF} + 1.32	V
V_{RF12_RFDIG}	Analog supply voltage for RF digital	V_{GND_RF} - 0.3	V_{GND_RF} + 1.32	V
V_{RF12_RFVCO}	Analog supply voltage for VCO	V_{GND_RF} - 0.3	V_{GND_RF} + 1.32	V
V_{RF12_RFADC}	Analog supply voltage for RF ADC	V_{GND_RF} - 0.3	V_{GND_RF} + 1.32	V
V_{DD18_MVR}	Main voltage regulator input supply	V_{GND} - 0.3	V_{GND} + 1.98	V
V_{DD_LPVR}	Low power voltage regulator input supply	V_{GND} - 0.3	V_{GND} + 3.60	V
V_{RF18_RFVR}	RF voltage regulator input supply	V_{GND_RF} - 0.3	V_{GND_RF} + 2.75	V
$V_{ESD\text{-}HBM}$	Electrostatic discharge, human body model	2000		V
$V_{ESD\text{-}CDM}$	Electrostatic discharge, charge device model	75		V

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 9. Thermal characteristics

Symbol	Parameter	Min.	Max.	Unit
T_{oper}	Operative ambient temperature	-40	+85	°C
T_j	Operative junction temperature	-40	+125	°C
T_{st}	Storage temperature	-55	150	°C
$R_{j\text{-}amb}$	Thermal resistance junction to ambient(1)		41	°C/W

1. According to JEDEC specification on a 2 layers board

Table 10. Frequency limits

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
F_{CLK}	Operating ARM9 CPU frequency	V_{dd} = 1.2 V; T_C = 85 °C(1)	—	—	208	MHz
F_{AHB}	AHB frequency		—	—	52	MHz

1. Not tested in production.

Table 11. Power consumption

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
P_{RF}	RFIP power (total $V_{RF18RFVR}$)	GPS + GLONASS T_{amb} = 25°C $V_{RF18RFVR}$ = 1.8 V; LNA ON	—	51	—	mW
		GPS T_{amb} = 25°C $V_{RF18RFVR}$ = 1.8 V; LNA ON	—	32	—	mW
P_{MVR}	Switchable area power (total $V_{DD18MVR}$)	f = 52 MHz (no PLL, FSMC and UART active, other peripherals inactive) T_{amb} = 25°C $V_{DD18MVR}$ = 1.8 V	—	56	—	mW
P_{LPVR}	Always ON area power (total V_{DDLPVR})	f = 52 MHz, T_{amb} = 25°C V_{DDLPVR} = 1.8 V	—	2	—	mW
P_{IO}	IO rings power (total V_{DDIO_rx})	f = 52 MHz (FSMC and UART active, other peripherals inactive), T_{amb} = 25°C V_{DDIO_rx} = 3.3 V	—	17	—	mW
I_{DSLEEP}	STAND-BY mode supply current	RTC running = 32.768 kHz, T_{amb} = 25°C, V_{DDLPVR} = 1.8 V	—	60	—	µA
I_{CC1}	Flash read current consumption	f = 52 MHz, T_{amb} = 25°C, V_{DDIO_r4} = 1.8 V			25	mA
I_{CC2}	Flash programming current consumption	f = 52 MHz, T_{amb} = 25°C, V_{DDIO_r4} = 1.8 V			20	mA
I_{CC3}	Flash sector/block erase current consumption	f = 52 MHz, T_{amb} = 25°C, V_{DDIO_r4} = 1.8 V			20	mA
I_{CC4}	Flash current consumption at power on	f = 52 MHz, T_{amb} = 25°C, V_{DDIO_r4} = 1.8 V			2.5	mA

4.6 Recommended DC operating conditions

Table 12 lists the functional recommended operating DC parameters for STA8088FG.

Table 12. Recommended DC operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DDIO}(1)	1.8V I/O supply voltage	1.71	1.8	1.89	V
	3.3V I/O supply voltage	3.00	3.30	3.60	V
V_{DDIO_r5}	I/O supply voltage for ring 5	3.00	3.30	3.60	V
V_{DD18_MVR}	Main voltage regulator input supply	1.71	1.8	1.89	V
V_{RF18_RFVR}	RF voltage regulator input supply	1.71	1.8	1.89	V
V_{DD_LPVR}	Low power voltage regulator input supply	1.62		3.60	V
T_C	Operating case temperature	-40		85	°C

1. Applicable to V_{DDIO_r1}, V_{DDIO_r2}, V_{DDIO_r3}, V_{DDIO_r4}

4.7 DC characteristics

Table 13 specifies the low voltage detection thresholds

Table 13. Low voltage detection thresholds

Parameter		Min.	Typ.	Max.	Unit
Input LVD main VR	Upper voltage threshold	1.55	1.62	1.67	V
	Lower voltage threshold	1.50	1.57	1.62	V
	Hysteresis	40	51	56	mV
Output LVD Main VR	Upper voltage threshold	1.18(1)	-	1.21(1)	V
	Lower voltage threshold	1.05	1.11	1.15	V
Input LVD LowPower VR	Upper voltage threshold	1.55	1.59	1.67	V
	Lower voltage threshold	1.50	1.57	1.62	V
	Hysteresis	18	22	25	mV
Output LVD LowPower VR	Upper voltage threshold	1.18(1)	-	1.21(1)	V
	Lower voltage threshold	1.10(1)	-	1.13(1)	V

1. Not tested in production.

Table 14 lists the DC characteristics for all the IO digital buffers expect for the following input buffers: STBYn (24), STDBY_OUT (23), WAKEUP (26) and RSTn (25).

Table 14. I/O buffers DC characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}(1)	Logical input low level voltage	V_{ddio} = 1.8 V	-0.3	—	0.3 * V_{ddio}	V
		V_{ddio} = 3.3V	-0.3	—	0.8	V

Table 14. I/O buffers DC characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IH}(1)	Logical input high level voltage	V_{ddio} = 1.8 V	0.7 * V_{ddio}	—	V_{ddio} + 0.3	V
		V_{ddio} = 3.3V	2.0	—	V_{ddio} + 0.3	V
V_{HYST}(2)	Schmitt-trigger hysteresis	–	50	—		mV
V_{OL}	Low level output voltage	V_{ddio} = 1.8 V		—	0.4	V
		V_{ddio} = 3.3V		—	0.4	V
V_{OH}	High level output voltage	V_{ddio} = 1.8 V	V_{ddio} - 0.4	—		V
		V_{ddio} = 3.3V	V_{ddio} - 0.4	—		V

1. Excludes oscillator inputs RTC_XTI and XTAL_IN. Refer to oscillator electrical specifications.
2. Apply to all digital inputs unless specified otherwise.

Table 15 lists the DC characteristics for the 1.2V IO digital buffers input buffers: STBYn (24), STDBY_OUT (23), WAKEUP (26) and RSTn (25).

Table 15. 1.2V I/O buffers DC characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Logical input low level voltage	V_{DD12_LPVR} = 1.2 V	-0.3	—	0.4 * V_{DD12_LPVR}	V
V_{IH}	Logical input high level voltage	V_{DD12_LPVR} = 1.2 V	0.7 * V_{ddio}	—	V_{DD12_LPVR} + 0.3	V
V_{OL}	Low level output voltage	V_{DD12_LPVR} = 1.2 V		—	0.2	V
V_{OH}	High level output voltage	V_{DD12_LPVR} = 1.2 V	V_{DD12_LPVR} - 0.2	—		V

4.8 AC characteristics

4.8.1 RF electrical specifications

Table 16. LNA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
S_{21}	Power gain		15	17	21	dB
NF	Noise Figure @ 25°C			1.3(1)		dB
IP_{1dB}	Input compression point	In G3 band	-26	-23		dBm

1. Not tested in production.

Table 17. RFA – MIXER G3 – GALGPS FILTER & VGA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
RFA_{GV}	RFA voltage gain	Max gain (not testable)		20		dB
		Min gain (not testable)		10		dB
		Delta gain	7	10	12	dB
f_{IF}	IF frequency			4.092		MHz
NF	RF-IF-VGA noise figure	For max gain		4.5(1)		dB
G_C	Conversion gain (from RFAin to ADC input)	VGA and RFA at max gain	89	100	104	dB
		VGA and RFA at min gain	38	50	54	
VGA	VGA dynamic range		45	50	55	dB
IP_{1dB}	RF-IF-VGA input compression point	In G3 band; RFA max; VGA min	-70	-65		dBm
IRR	Image rejection ratio		15	20		dB
BW_{GPS}	-3dB IF bandwidth	GPS mode	1.8	2.4		MHz
BW_{GAL}		Galileo mode		4.8		MHz
ATT	Alias frequency rejection	F=12 MHz	20			dB
		F = 28 MHz (Galileo)		28		dB
T_{gGPS}	IF filter group delay variation	GPS mode, fc ±1023 kHz			200(1)	ns
T_{gGAL}		Galileo mode, fc ±2046 kHz			60(1)	ns

1. Not tested in production.

Table 18. RFA – MIXER G3 – GLONASS FILTER & VGA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
RFA_{GV}	RFA voltage gain	Max gain (not testable)		20		dB
		Min gain (not testable)		10		dB
		Delta gain	7.3	10	12.6	dB
f_{IFGNS}	IF frequency			8.5		MHz
NF	RF-IF-VGA noise figure	For max gain		5(1)		dB
G_C	Conversion gain (from RFAin to ADC input)	VGA and RFA at max gain	84	95	107	dB
		VGA and RFA at min gain	33	45	54	
VGA	VGA dynamic range		38	50	64	dB
IP_{1dB}	RF-IF-VGA input compression point	In G3 band; RFA max; VGA min	-74	-69		dBm
IRR	Image rejection ratio		15	20		dB
$BW_{GLONASS}$	-1dB IF bandwidth		9	10		MHz

Table 18. RFA – MIXER G3 – GLONASS FILTER & VGA (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ATT	Alias frequency rejection	F = 24 MHz	20	29		dB
T_{gGPS}	IF filter group delay variation	fc ± 4000 kHz			20(1)	ns

1. Not tested in production.

Table 19. Synthesizer

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{TCXO_XTAL}	Input frequency for xtal amplifier (1)	10		52	MHz
R_{DIV}	Reference divider range	1		63	
N_{DIV}	Loop divider range	56		2047	
F_{LO}	LO operating frequency		3142.656		MHz

1. That amplifier can be used also like TCXO input buffer

4.8.2 Oscillator electrical specifications

This device contains two oscillators:

- a 32.768 kHz oscillator/buffer for RTC circuit.
- a 26 MHz oscillator/buffer in the RF Front-End

When used in oscillator mode, each oscillator requires a specific crystal, with parameters that must be as close as possible to the following recommended values. When used in input buffer mode, an external clock source must be applied.

32.768 kHz OSCI32 oscillator specifications

The 32.768 kHz OSCI32 oscillator is connected between RTC_XTI (oscillator amplifier input) and RTC_XTO (oscillator amplifier output). It also requires two external capacitors (CL), as shown on *Figure 5*. The CL value is linked to XTAL suppliers.

OSCI32 is power supplied by an internal dedicated DC regulators (DCREG_OSCI) that outputs a regulated 1.4V (+/- 100mV) from the unregulated VDD_LPVR input. DCREG_OSCI is enabled by default and it can be powered down by setting bit20-DCREG_OSCI_PD of CLK_CTRL_BCK_REG0.

OSCI32 is disabled by default and must be enabled by setting bit21-OSCI_EN of CLK_CTRL_BCK_REG0 to have 32.768KHz oscillation when an XTAL pi-network is connected to RTC_XTI/RTC_XTO pins.

The oscillator amplifier specifications are shown in following table:

Table 20. Oscillator amplifier specifications

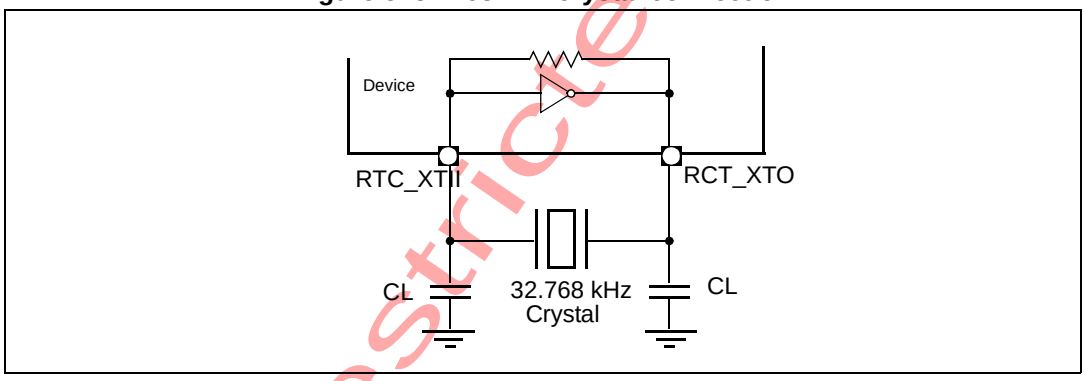
Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{ILOSCI32}$	Low level input voltage(1)	—	—	0.3	V
$V_{IHOSCI32}$	High level input voltage(1)	1.04	—	—	V

Table 20. Oscillator amplifier specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{HYSTO}	Input hysteresis(1)	35	—	—	mV
T_S	Startup time(1)	0.5	15 x L_m/R_m	5	s
T_{RISE}	Rise time(2)	0.6	—	—	ns
T_{FALL}	Fall time(2)	0.6	—	—	ns
GM	Transconductance	10	—	—	µA/V

1. Not tested in production.
2. Oscillator in bypass mode.

Figure 5. 32.768 kHz crystal connection



To drive the 32.768 kHz crystal pins from an external clock source:

- Disable the oscillator (bit21-OSCI_EN = 0b in CLK_CTRL_BCK_REG0 register). This disables the internal inverter, thus reducing the power consumption to minimum. This also allows to drive RTC_XTI input even when a crystal is connected between RTC_XTI and RTC_XTO pins.
- Drive the RTC_XTI pin with a square signal that has low level $V_{ILOSCI32}$ and a high level $V_{IHOSCI32}$, or a sine wave (maximum amplitude: $V_{IHOSCI32}$ / 2, offset: $V_{IHOSCI32}$ / 2).

Table 21. Characteristics of external slow clock input

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{JIT} (cc)	Cycle-to-cycle jitter	-70	—	70	ps
T_{JIT} (per)	Period jitter	-70	—	70	ps
	Variation	-500	—	500	ppm
T_{DUTY}	Duty cycle	45	—	55	%

4.8.3 26 MHz oscillator specifications

Refer to RF Front-End section for details.

4.8.4 System PLL specifications

This section gives the AC specification of System PLL embedded in STA8088FG device. As depicted in *Figure 6*, it receives, from the G3RF Front End, a buffered version of the external 26MHz clock source and generates a 624MHz clock used as clock reference for the clock generation block. Analog/digital power supplies connections are implemented inside the device without any needs of dedicated external pins. The SYSPLL is managed by the ARM MCU through APB Bridge 1.

Figure 6. System PLL block diagram

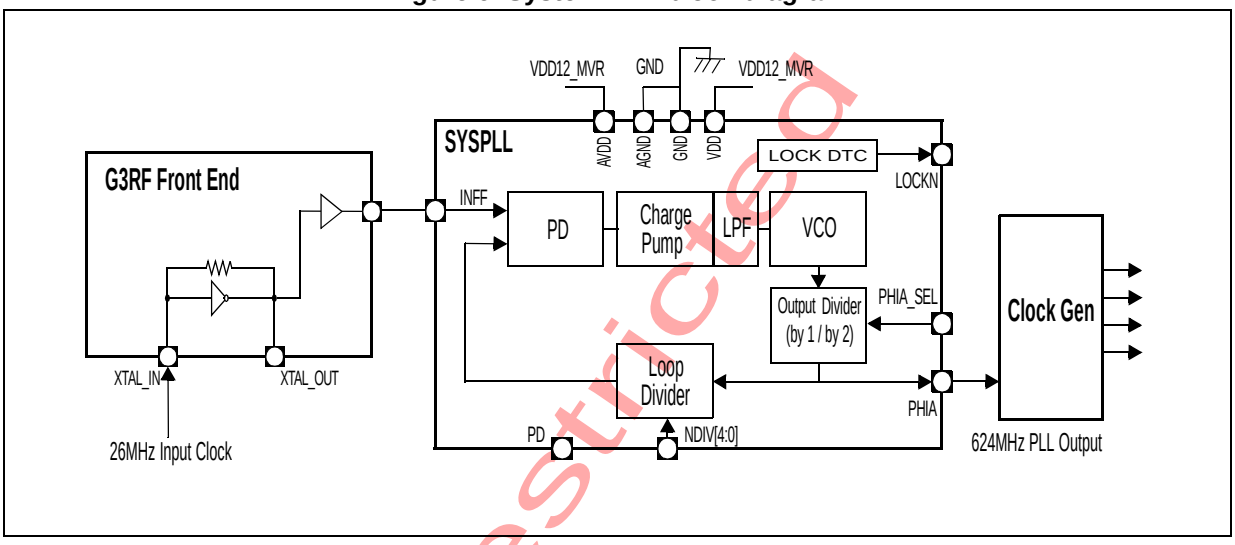


Table 22. SYSPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{IN_RANGE}	INFF input clock frequency range(1)	4	—	65	MHz
δ_{INFF}	INFF input clock duty cycle(1)	40	—	60	%
$T_{R/F}$	INFF input clock rise/fall time(1)	—	—	0.1	ns
F_{VCO}	VCO frequency range(1)	240	—	650	MHz
F_{PLL}	PLL output PHIA frequency range(1)	120	—	650	MHz
T_{LOCK}	Lock time(1)	—	—	100	µs

1. Not tested in production.

4.8.5 ADC specifications

This section gives the AC specification of the 10 bit Successive Approximation Register ADC embedded in STA8088FG device. It is controlled by the ARM9 MCU through a wrapper and an APB bridge as depicted in *Figure 7* and it has a maximum conversion rate of 1MSPS with 8 muxed analog input channels capability. An internal voltage reference is used and analog/digital power supplies connections are implemented inside the device without any needs of dedicated external pins.

Figure 7. SARADC connections

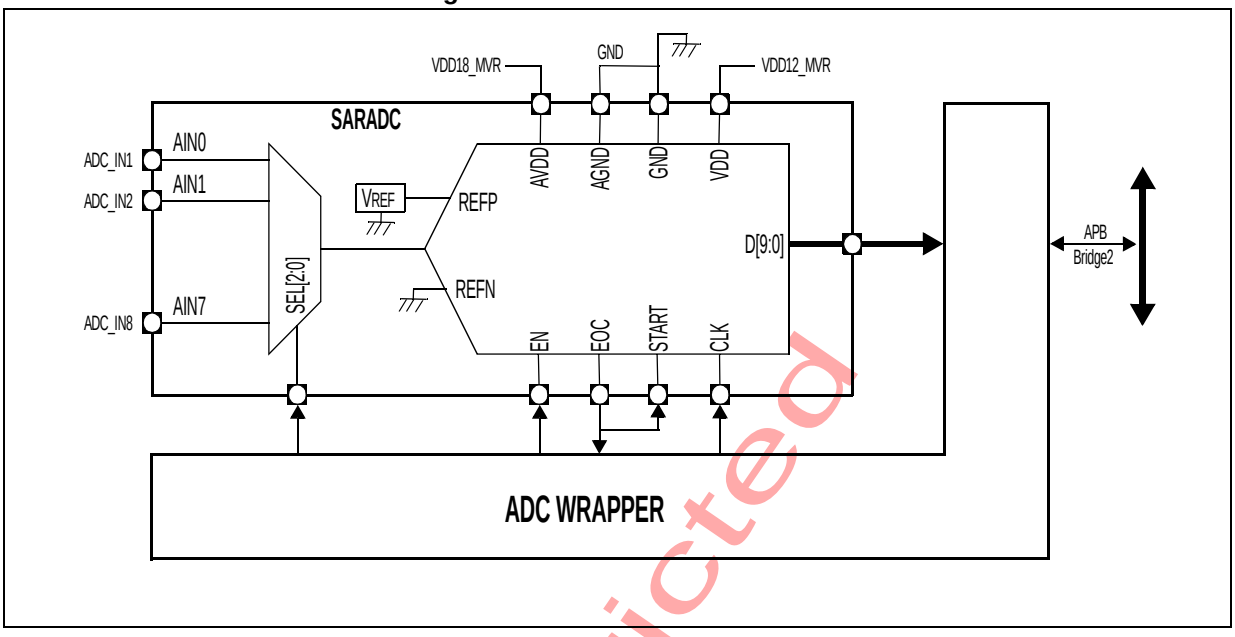


Table 23. SARADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ADCIN}	ADC_IN input range(1)	V_{GND}-0.3	—	V_{DD18_MVR}+0.3	V
V_{ADCCR}	Conversion range(1)	V_{GND}	—	V_{REF}	V
V_{REF}	Voltage reference(1)	1.35	1.4	1.45	V
C_{IN}	Input capacitance(1)	5.5	7.0	8.5	pF
R_{IN}	Input mux resistance (total equivalent sampling resistance)(1)(2)	1.5	2.0	2.5	kΩ
F_{CLK}	Clock frequency(1)	2.5		15	MHz
δ_{CLK}	Clock duty cycle(1)	45	50	55	%
T_{SUP}	Start up time(1)(3)	—	—	20	µs
T_C	Conversion time(1)	—	14		cycles
T_S	Sampling time(1)	—	3		cycles
INL	Performance			< +/- 2	LSB
DNL				< +/- 2	LSB

1. Not tested in production.
2. Pad input capacitance included.
3. From EN=1.

4.8.6 Flash specifications

This section gives the AC specification of the embedded Flash in STA8088FG device.

Table 24. Flash specifications

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f_C	Serial clock frequency	QPI mode - 4 read instructions	—		78	MHz
t_{SE}	Sector erase cycle time		—	30	200	ms
t_{BE}	Block erase cycle time		—	500	2000	ms
t_{CE}	Chip erase time	Size = 16 Mb	—	8	20	s
t_{PP}	Page program cycle time		—	0.9	3	ms

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

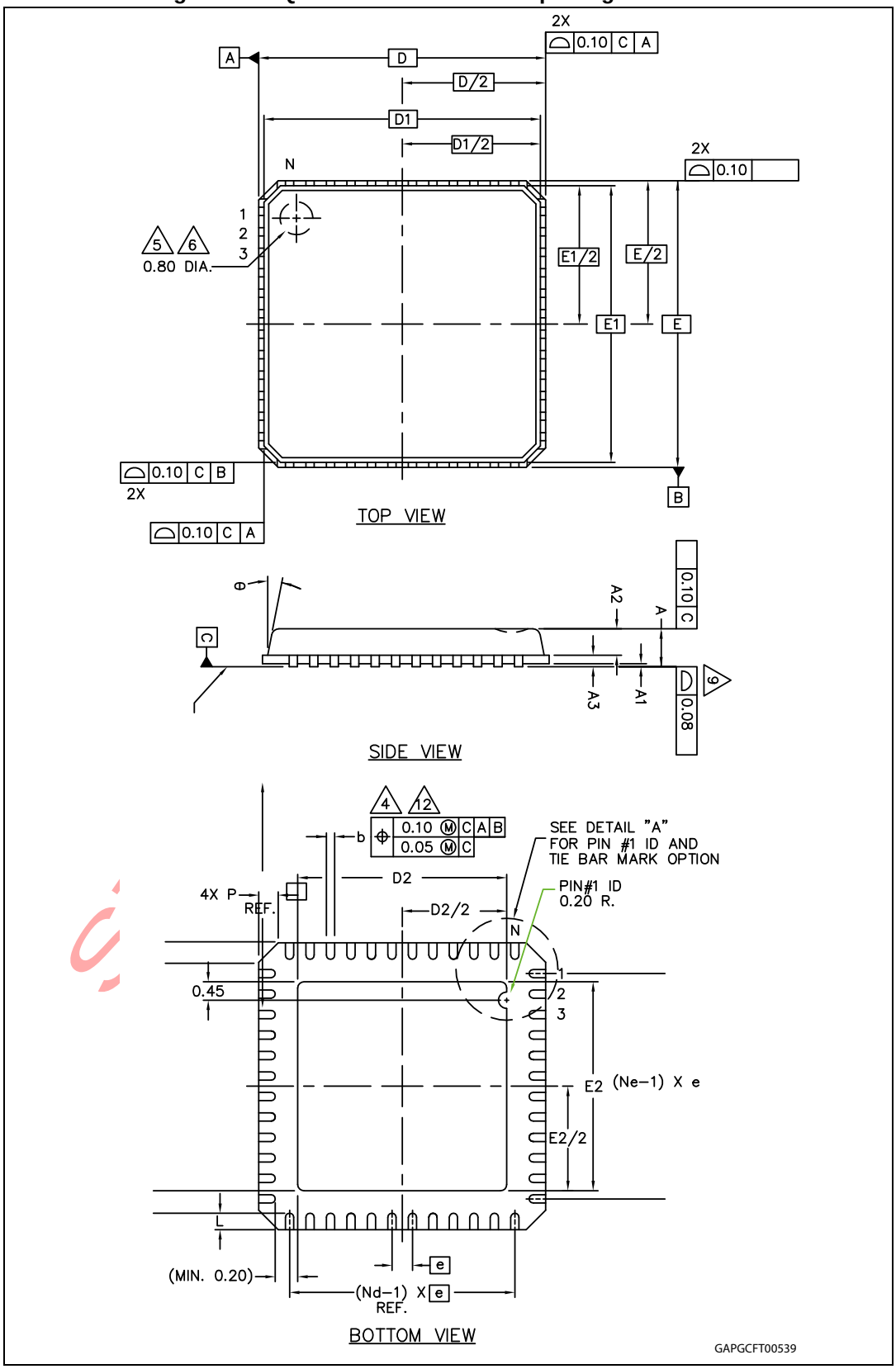
ECOPACK® is an ST trademark.

5.2 VFQFPN56 7 x 7 x 0.85 mm package information

Table 25. VFQFPN56 package dimensions

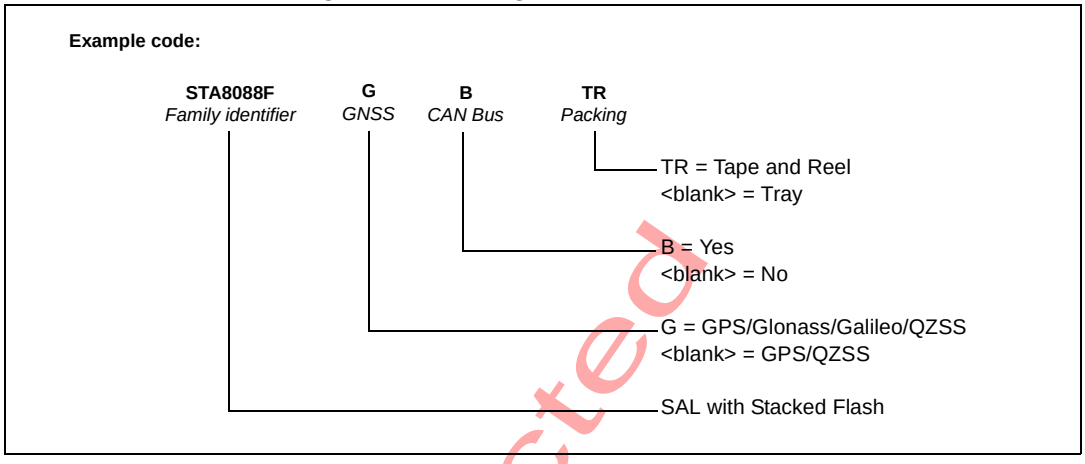
Symbol	Min.	Typ.	Max
Common dimensions			
A	0.80	0.85	0.90
A1	0	0.01	0.05
A2	0.60	0.65	0.70
A3		0.20 REF	
b	0.15	0.20	0.25
D		7.00 BSC	
D1		6.75 BSC	
D2	5.0	5.1	5.2
E		7.00 BSC	
E1		6.75 BSC	
E2	5.0	5.1	5.2
e		0.40 BSC	
θ	0°		12°
L	0.30	0.40	0.50
N		56	
Nd		14	
Ne		14	
P	0.24	0.42	0.60
Q	0.30	0.40	0.65
R	0.13	0.17	0.23

Figure 8. VFQFPN56 7 x 7 x 0.85 mm package dimension



6 Ordering information

Figure 9. Ordering information scheme



7 Revision history

Table 26. Document revision history

Date	Revision	Changes
26-Jan-2012	1	Initial release.
07-Mar-2012	2	Updated *Features* list Updated following figures: – *Figure 2: VFQFPN56 connection diagram - with CAN (bottom view)* – *Figure 3: VFQFPN56 connection diagram - no CAN (bottom view)* *Table 2: Main function pins*: – USB_DP/UART1_TX, USB_DM/UART1_RX: updated I/O
27-Jun-2012	3	Updated *Section 4.2: Minimum and maximum values* Updated following tables: – *Table 8: Voltage characteristics* – *Table 10: Frequency limits*: – *Table 11: Power consumption*: – *Table 16: LNA* – *Table 17: RFA – MIXER G3 – GALGPS FILTER & VGA* – *Table 18: RFA – MIXER G3 – GLONASS FILTER & VGA*
17-Sep-2014	4	*Table 2: Main function pins*: – RSTn: added note – WAKEUP: added note *Table 3: Test/emulated dedicated pins*: – TRSTn: added note *Table 11: Power consumption*: – I_{CC4}: added parameter Added *Section 2.9: Pin terminal characteristics* Updated *Section 4.8.2: Oscillator electrical specifications*