

**PROTECTION PRODUCTS**
**Absolute Maximum Rating**

Rating	Symbol	Value	Units
Peak Pulse Current ( $t_p = 8/20\mu s$ )	$I_{PP}$	24	A
Rectifier Repetitive Peak Reverse Voltage	$V_{RRM}$	70	V
Thermal Resistance, Junction to Ambient	$\theta_{JA}$	163	$^{\circ}C/W$
Thermal Resistance, Junction to Case	$\theta_{JC}$	38.8	$^{\circ}C/W$
Lead Soldering Temperature	$T_L$	260 (10 sec.)	$^{\circ}C$
Operating Temperature	$T_J$	-55 to +125	$^{\circ}C$
Storage Temperature	$T_{STG}$	-55 to +150	$^{\circ}C$

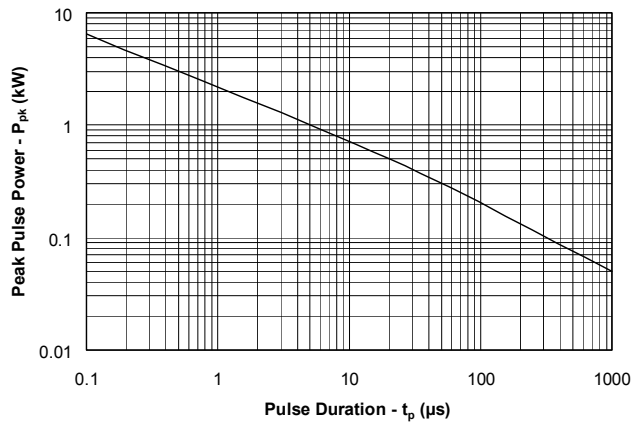
**Electrical Characteristics**

SRDA70-4						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Rectifier Repetitive Peak reverse Voltage	$V_{RRM}$				70	V
Reverse Breakdown Voltage	$V_{BR}$	$I_t = 50\mu A$	85			V
Reverse Leakage Current	$I_R$	$V_{RWM} = 70V, T=25^{\circ}C$			5	$\mu A$
Forward Voltage	$V_F$	$I_{PP} = 1A, t_p = 8/20\mu s$			1.3	V
Forward Voltage	$V_F$	$I_{PP} = 10A, t_p = 8/20\mu s$			3.3	V
Junction Capacitance	$C_J$	Between I/O pins and Ground $V_R = 0V, f = 1MHz$			15	pF
		Between I/O pins $V_R = 0V, f = 1MHz$		4		pF

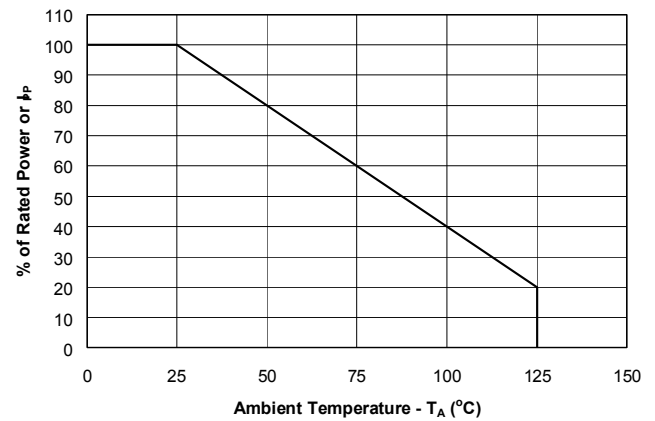
# PROTECTION PRODUCTS

## Typical Characteristics

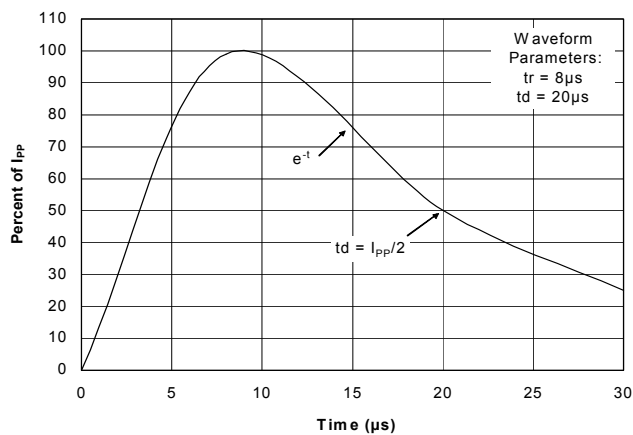
### Non-Repetitive Peak Pulse Power vs. Pulse Time



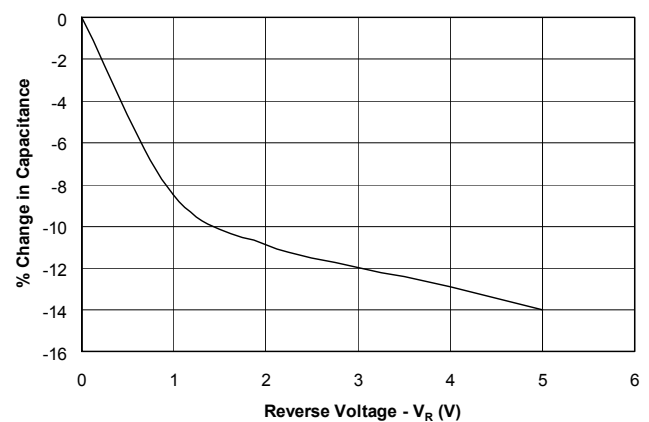
### Power Derating Curve



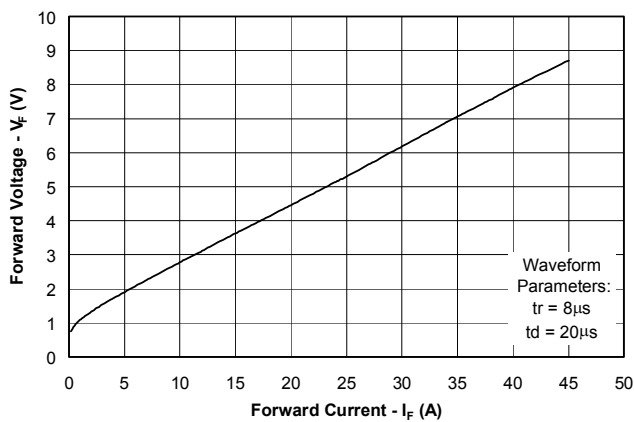
### Pulse Waveform



### Variation of Capacitance vs. Reverse Voltage



### Foward Voltage vs. Forward Current



## PROTECTION PRODUCTS

### Applications Information

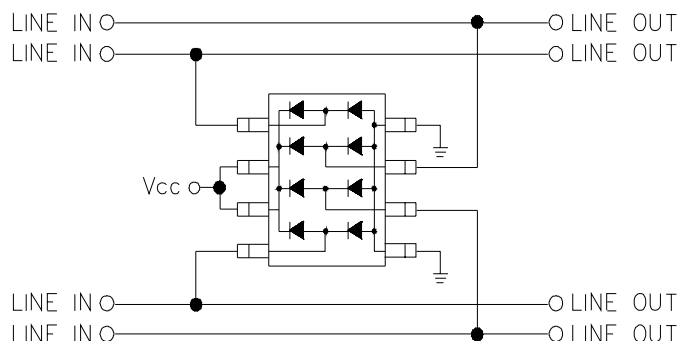
#### Device Connection Options for Protection of Four High-Speed Data Lines

The SRDA70-4 TVS is designed to protect four data lines from transient over-voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode  $V_F$ ) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 4, 6 and 7. The negative reference (REF2) is connected at pins 5 and 8. These pins should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance.

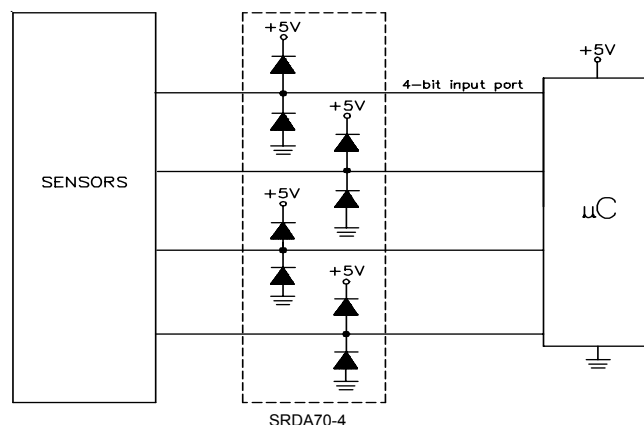
The positive reference (REF1) is connected at pins 2 and 3. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pins 2 and 3 directly to the positive supply rail ( $V_{CC}$ ). In this configuration the data lines are referenced to the supply voltage. An external TVS diode may be added between the supply rail and ground in order to prevent over-voltage on the supply rail.
2. The SRDA70-4 can be isolated from the power supply by adding a series resistor between pins 2 and 3 and  $V_{CC}$ . A value of  $10k\Omega$  is recommended. The internal steering diodes remain biased, providing the advantage of lower capacitance.
3. In applications where no positive supply reference is available, or complete supply isolation is desired, an external TVS diode may be used as the reference. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).

#### I/O Protection

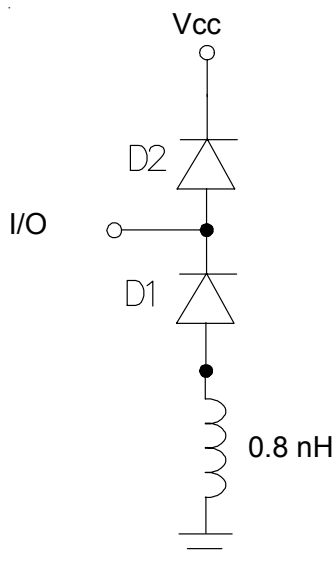


#### Microcontroller Protection

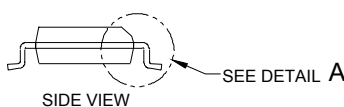
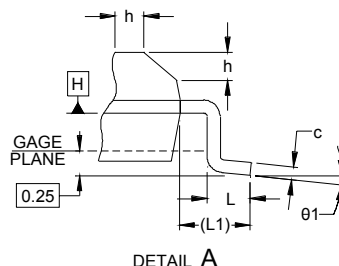
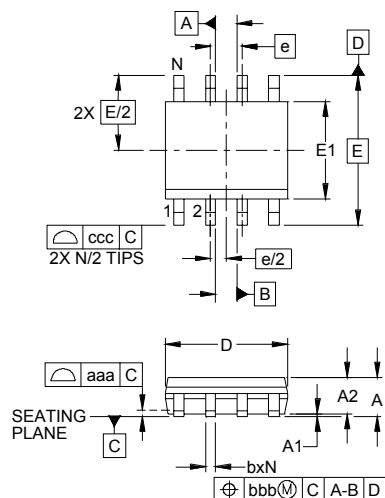


#### Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

**PROTECTION PRODUCTS**
**Applications Information - Spice Model**

**SRDA70-4 Spice Model**

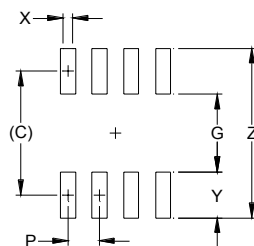
<b>SRDA70-4 Spice Parameters</b>			
<b>Parameter</b>	<b>Unit</b>	<b>D1 (LCRD)</b>	<b>D2 (LCRD)</b>
IS	Amp	3.54E-14	1.46E-14
BV	Volt	680	240
VJ	Volt	0.62	0.64
RS	Ohm	0.330	0.124
IBV	Amp	1E-3	1E-3
CJO	Farad	5.2E-12	6.2E-12
TT	sec	2.56E-9	2.56E-9
M	--	0.058	0.058
N	--	1.1	1.1
EG	eV	1.11	1.11

**PROTECTION PRODUCTS**
**Outline Drawing - S0-8**


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

**NOTES:**

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AA.

**Land Pattern - S0-8**


DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

**NOTES:**

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.

**PROTECTION PRODUCTS****Ordering Information**

Part Number	Lead Finish	Qty per Reel	Reel Size
SRDA70-4.TB	SnPb	500	7 Inch
SRDA70-4.TBT	Pb Free	500	7 Inch
SRDA70-4	SnPb	95/Tube	N/A
SRDA70-4.T	Pb Free	95/Tube	N/A

Note: Lead-free devices are RoHS/WEEE Compliant

**Contact Information**

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