ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

PV_{IN},V_{IN} 6V
All other pins ..... -0.3V to VIN+0.3V
PV_{IN}, P_{GND}, LX current 2A
Storage Temperature ..... -65°C to 150°C

OPERATING RATINGS

Input Voltage Range V_{IN}..... UVLO to 5.5V
Ambient Temperature Range ..... -40°C to +85°C
Thermal Resistance θ_{JA} .....40.5°C/W

ELECTRICAL SPECIFICATIONS

Specifications with standard type are for an Operating Ambient Temperature of T_A = 27°C only; limits applying over the full Operating Ambient Temperature range are denoted by a "•". Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_A = 27°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN} = UV_{IN} = V_{SDN} = 3.6V, V_{OUT} = V_{FB}, I_{OUT} = 0mA, T_A= –40°C to 85°C.

Parameter	Min.	Typ.	Max.	Units		Conditions
Input Voltage Operating Range	UVLO		5.5	V	•	Result of I_Q measurement at V_{IN}=PV_{IN}=5.5V
Minimum Output Voltage	1.0			V	•	
FB Set Voltage, Vr	0.784	0.800	0.816	V		25°C, I_O=200mA Close Loop. L_I = 10µH, C_{OUT} = 22µF
Overall Accuracy			±5	%	•	Measured at V_{IN}=5.5V, no load and V_{IN}=3.6V, 200mA load, Close Loop T_A= –40°C to 85°C
			±4			Measured at V_{IN}=5.5V, no load and V_{IN}=3.6V, 200mA load, Close Loop T_A= 0°C to 70°C
On-Time Constant – K_{ON} Min, T_{ON}=K_{ON}/(V_{IN}-V_{OUT})	1.5	2.25	3.0	V*µs	•	Close Loop, L_I = 10µH,C_{OUT} = 22µF
Off-Time Constant – K_{OFF} Min, T_{OFF}=K_{OFF}/V_{OUT}	1.6	2.4	3.2	V*µs	•	Inductor current limit tripped, VFB=0.5V Measured at V_{OUT}=1V
Off-Time Blanking		100		ns	•	
Turn On Time		200	400	µs	•	400mA Load
PMOS Switch Resistance		0.3	0.6	Ω	•	I_{PMOS}= 200mA
NMOS Switch Resistance		0.3	0.6	Ω	•	I_{NMOS}= 200mA
Inductor Current Limit	500	625	750	mA	•	VFB=0.5V
Power Efficiency		96		%	•	V_{OUT}=2.5V, I_O=200mA
		92				V_{OUT}=3.3V, I_O=400mA
Minimum Guaranteed Load Current	400	500		mA	•	
V_{IN} Quiescent Current		20	30	µA	•	V_{OUT}=3.3V, V_{IN}=3.6V and V_{IN}= 5.5V
V_{IN} Shutdown Current		1	500	nA	•	D1=D0=0V
V_{OUT} Quiescent Current		2	5	µA	•	V_{OUT}= 3.3V
V_{OUT} Shutdown Current		1	500	nA	•	D1=D0=0V
UVLO Undervoltage Lockout Threshold, V_{IN} falling	2.55	2.70	2.85	V	•	D1=0V, D0=V_{IN}
	2.70	2.85	3.00			D1=V_{IN}, D0=0V
	2.85	3.00	3.15			D1=V_{IN}, D0=V_{IN}
UVLO hysteresis		40		mV	•	
Battlo Trip Voltage, V_{IN}falling	265	300	335	mV	•	Measured as V_{IN}-V_{OUT}
Battlo Trip Voltage Hysteresis		9		mV	•	

Parameter	Min.	Typ.	Max.	Units		Conditions
BLON Low Output Voltage			0.4	V	•	V_{IN}=3.3V, I_{SINK}=1mA
BLON Leakage Current			1	µA	•	V_{BLON}=3.6V
Over-Temperature Rising Trip Point		140		°C	•	
Over-Temperature Hysteresis		14		°C	•	
D1,D0 Leakage Current		1	500	nA	•	
D1,D0 Input Threshold Voltage	0.60	0.90		V	•	High to Low Transition
		1.25	1.8			Low to High Transition
FB Leakage Current		1	100	nA	•	FB=1V
LX Leakage		3	5	µA	•	D1,D0=0V, V_{IN}=3.6V LX=0V,LX=V_{IN}+0.2V

BLOCK DIAGRAM

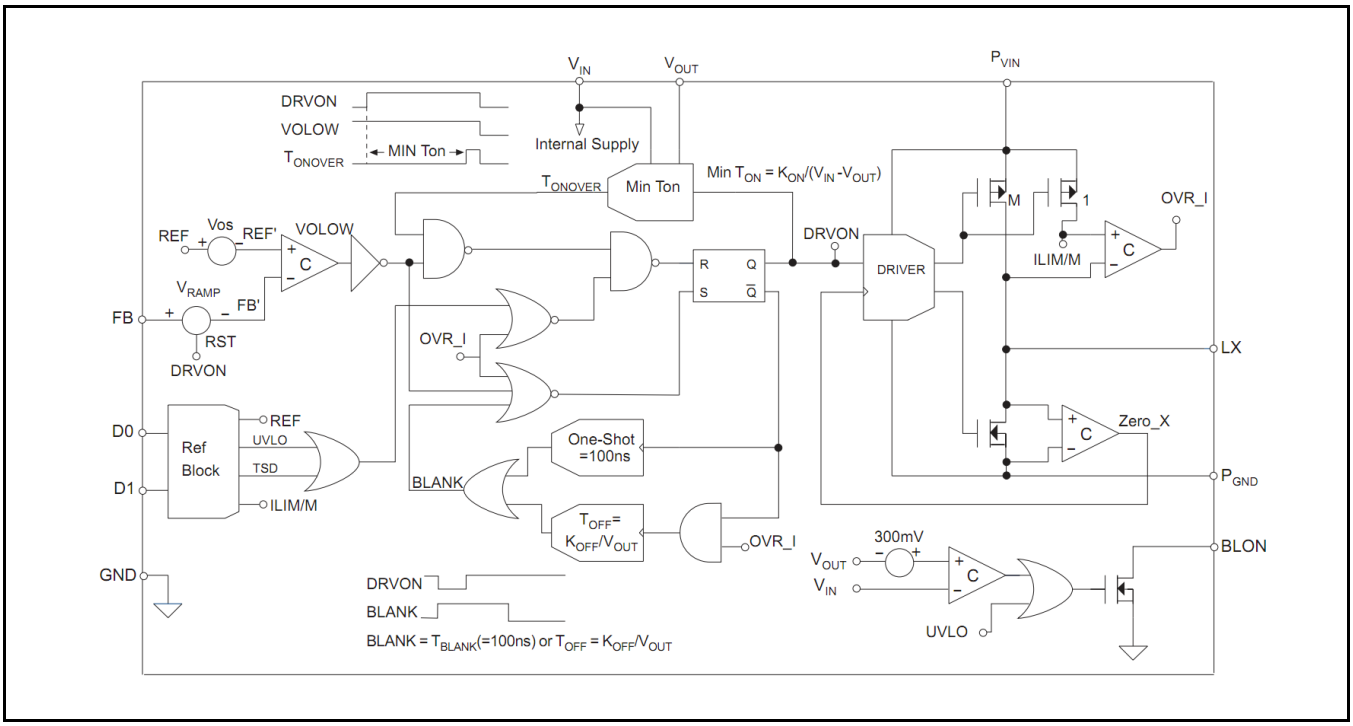


Fig. 2:SP6655 Block Diagram

PIN ASSIGNMENT

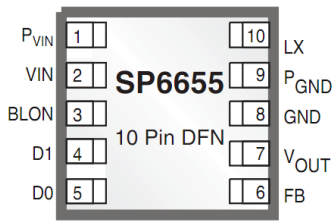


Fig. 3: SP6655 Pin Assignment

PIN DESCRIPTION

Name	Pin Number	Description
P_{VIN}	1	Input voltage power pin. Inductor charging current passes through this pin.
V_{IN}	2	Internal supply voltage. Control circuitry powered from this pin.
BLON	3	Open drain battery low output. (V_{IN}-V_O) less than 300mV pulls this node to ground. (V_{IN}-V_O) above threshold, this node is open.
D1	4	Digital mode control input. See table 1 for definition.
D0	5	Digital mode control input. See table 1 for definition.
FB	6	External feedback network input connection. Connect a resistor from FB to ground and FB to V_{OUT} to set the output voltage. This pin regulates to the internal bandgap reference voltage of 0.8V.
V_{OUT}	7	Output voltage sense pin. Used by the timing circuit to set minimum on and off times.
GND	8	Internal ground pin. Control circuitry returns current to this pin.
P_{GND}	9	Power ground pin. Synchronous rectifier current returns through this pin.
LX	10	Inductor switching node. Inductor tied between this pin and the output capacitor to create regulated output voltage.

D0	D1	Operating Mode
0	0	Shutdown. All internal circuitry is disabled and the power switches are opened.
0	1	Device enabled, falling UVLO threshold =2.70V
1	0	Device enabled, falling UVLO threshold =2.85V
1	1	Device enabled, falling UVLO threshold =3.00V

Table 1: Operating Mode Definition

ORDERING INFORMATION

Part Number	Temperature Range	Marking	Package	Packing Quantity	Note 1	Note 2
SP6655ER-L	-40°C≤T_A≤+85°C	SP66 55ER WWXX	DFN10	Bulk		
SP6655ER-L/TR				3K/Tape & Reel		
SP6655EB	Evaluation Board					

"YY" = Year – "WW" = Work Week – "X" = Lot Number; when applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at T_A = 27°C, unless otherwise specified - Schematic and BOM from Application Information section of this datasheet.

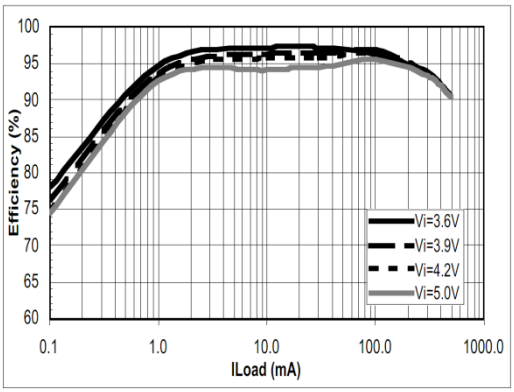


Fig. 4: Efficiency vs. Load, V_{OUT}=3.3V

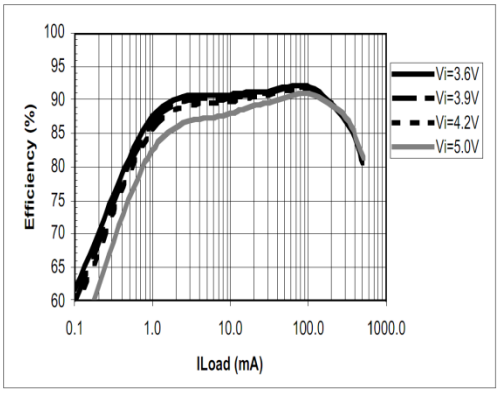


Fig. 5: Efficiency vs Load, V_{OUT}= 1.5V

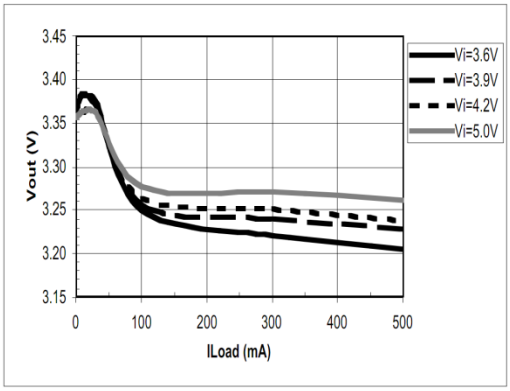


Fig. 6: Line/Load Rejection, V_{OUT}= 3.3V

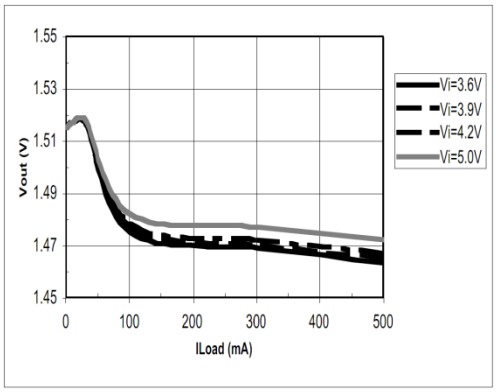


Fig. 7: Line/Load Rejection, V_{OUT}= 1.5V

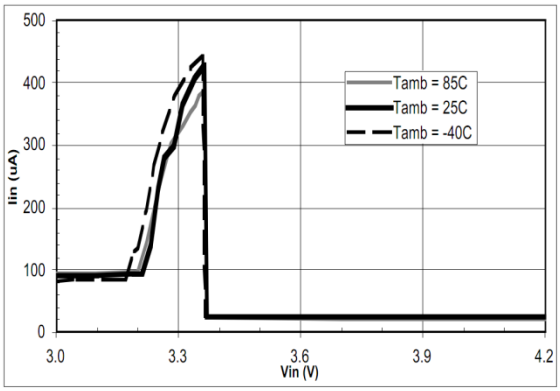


Fig. 8: No Load Battery Current, V_{OUT}=3.3V

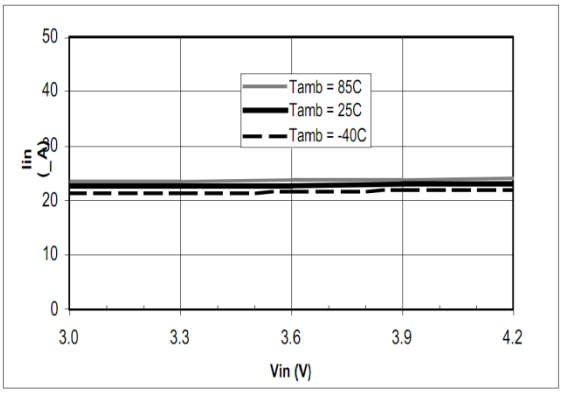


Fig. 9: No Load Battery Current, V_{OUT}=1.5V

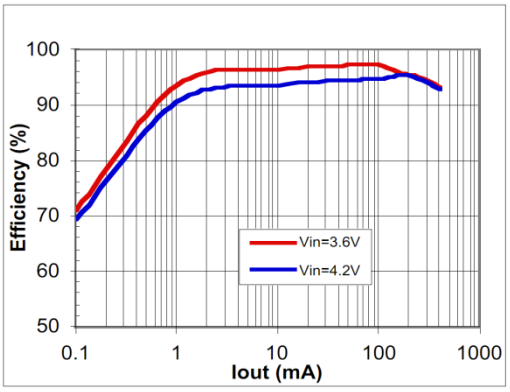


Fig. 10: 4.7µH Efficiency at $3.3V_{OUT}$
L1=LQH32CN4R7

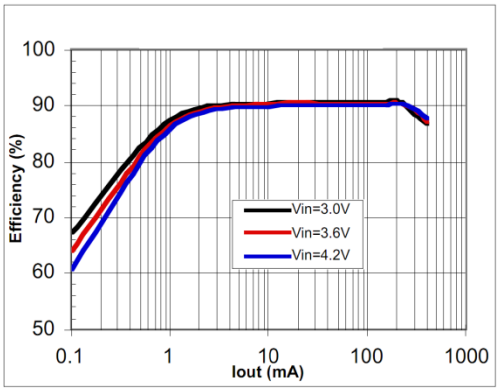


Fig. 11: 4.7µH Efficiency at $1.8V_{OUT}$
L1=LQH32CN4R7

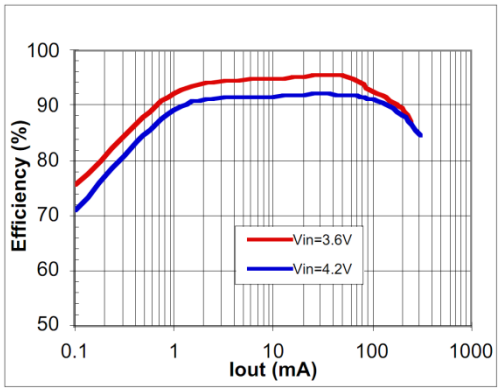


Fig. 12: 4.7µH Efficiency at $3.3V_{OUT}$
L1=LQH31CN4R7

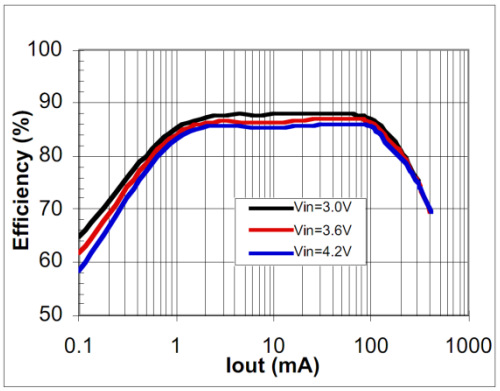


Fig. 13: 4.7µH Efficiency at $1.8V_{OUT}$
L1=LQH31CN4R7

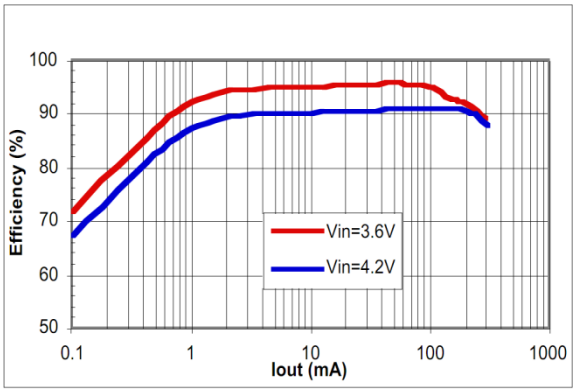


Fig. 14: 4.7µH Efficiency at $3.3V_{OUT}$
L1=LQH2MCN4R7

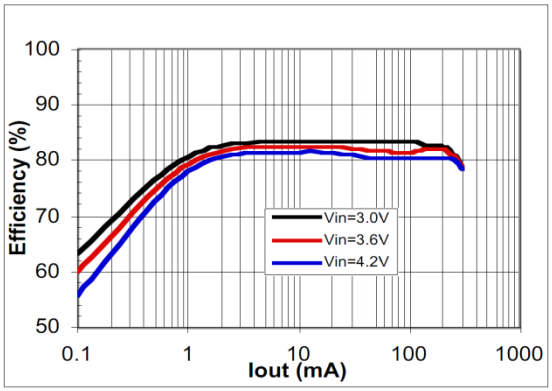


Fig. 15: 44.7µH Efficiency at $1.8V_{OUT}$
L1=LQH2MCN4R7

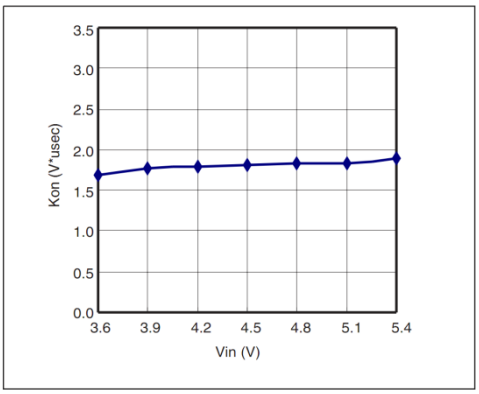


Fig. 16: K_{ON} vs V_{IN}, V_{OUT}=3.3V

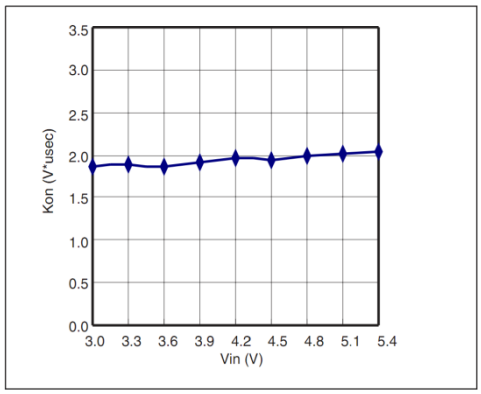


Fig. 17: K_{ON} vs V_{IN}, V_{OUT}=1.5V

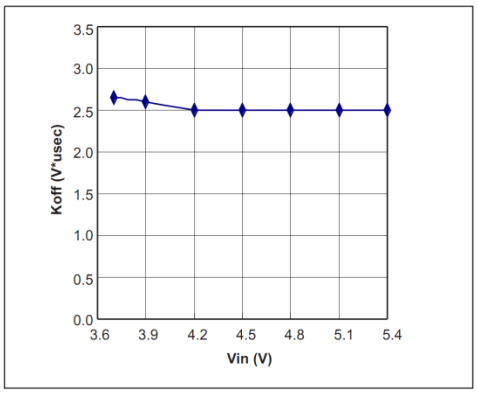


Fig. 18: K_{OFF} vs V_{IN}, V_{OUT}=3.3V

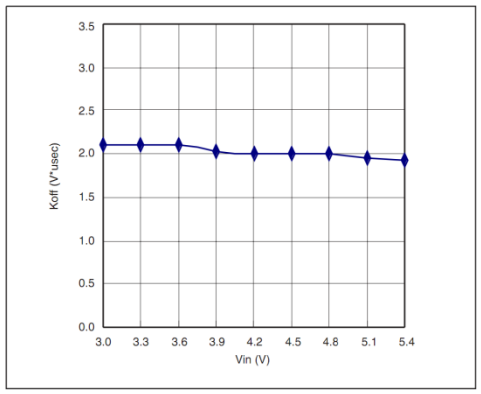


Fig. 19: K_{OFF} vs V_{IN}, V_{OUT}=1.5V

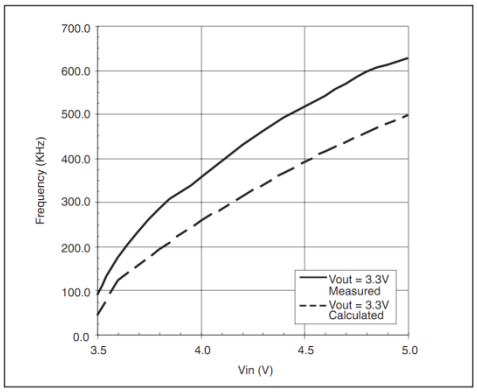


Fig. 20: Ripple Frequency vs. V_{IN}, I_{OUT}=0.4A, V_{OUT}=3.3V

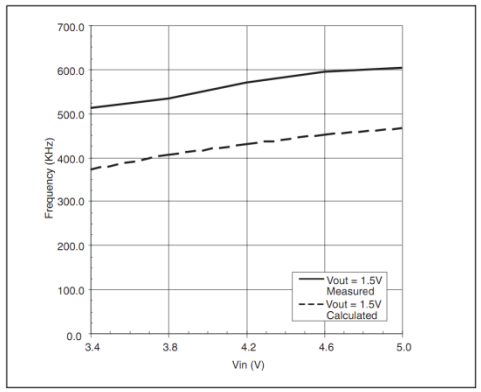


Fig. 21: Ripple Frequency vs. V_{IN}, I_{OUT}=0.4A, V_{OUT}=1.5V

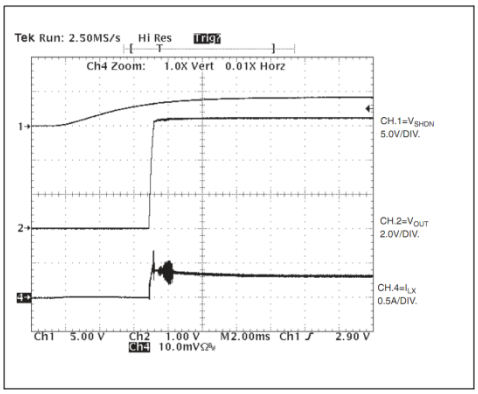


Fig.22: V_{IN} Start up, V_{IN} = 4.2V, I_{OUT}=0.4A, V_{OUT}=3.3V

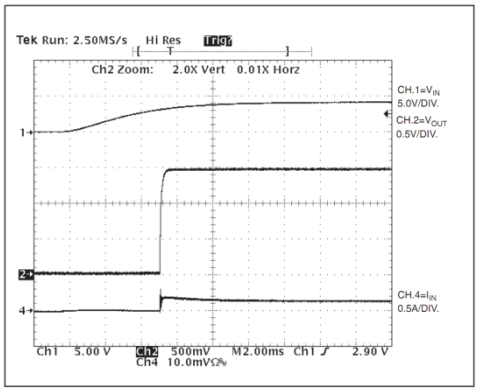


Fig.23: V_{IN} Start up, V_{IN} = 4.2V, I_{OUT}=0.4A, V_{OUT}=1.5V

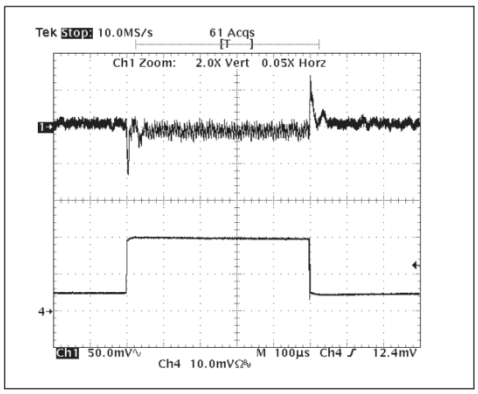


Fig. 24: Load Step, V_{IN}=4.2V, I_{OUT}=0.1A to 0.4A, V_{OUT}=3.3V

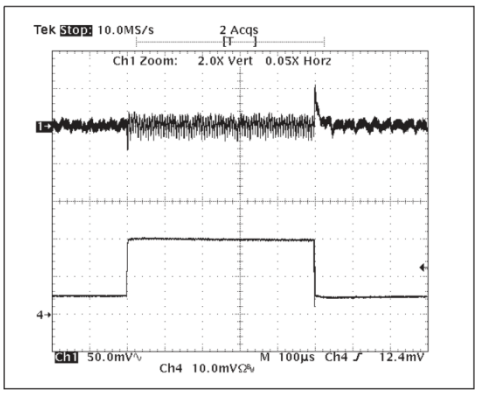


Fig.25: Load Step, V_{IN}=4.2V, I_{OUT}=0.1A to 0.4A, V_{OUT}=1.5V

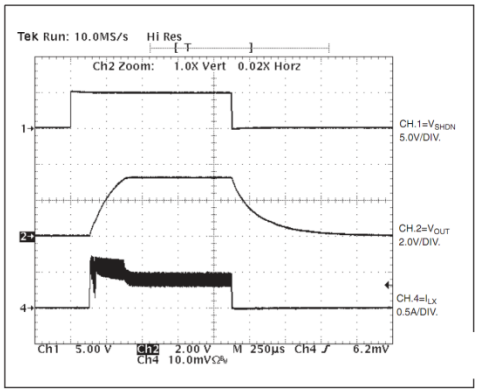


Fig.26: Start up from SHDN, V_{IN}=5V ,I_{OUT}=0.4A, V_{OUT}=3.3V

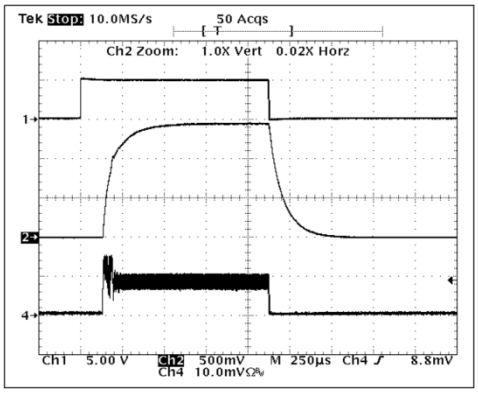


Fig.27: Start up from SHDN, V_{IN}=5V, I_{OUT}=0.4A, V_{OUT}=1.5V

THEORY OF OPERATION

The SP6655 is a high efficiency synchronous buck regulator with an input voltage range of +2.7V to +5.5Vand an output that is adjustable between +1.0V and V_{IN}. The SP6655 features a unique on-time control loop that runs in discontinuous conduction mode (DCM) or continuous conduction mode (CCM) using synchronous rectification. Other features include over-temperature shutdown, over-current protection, digitally controlled enable and under-voltage lockout, a battery low indicator, and an external feedback pin.

The SP6655 operates with a light load quiescent current of 20µA using a 0.3Ω PMOS main switch and a 0.3Ω NMOS synchronous switch. It operates with excellent efficiency across the entire load range, making it an ideal solution for battery powered applications and low current step-down conversions. The part smoothly transitions into a 100% duty cycle under heavy load/low input voltage conditions.

ON-TIME CONTROL - CHARGE PHASE

The SP6655 uses a precision comparator and a minimum on-time to regulate the output voltage and control the inductor current under normal load conditions. As the feedback pin drops below the regulation point, the loop comparator output goes high and closes the main switch. The minimum on-timer is triggered, setting a logic high for the duration defined by:

$$T_{ON} = \frac{K_{ON}}{V_{IN} - V_{OUT}}$$

where:

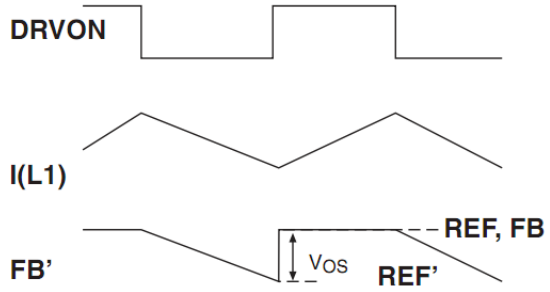
K_{ON}= 2.25V *µsec constant

V_{IN}= V_{IN} pin voltage

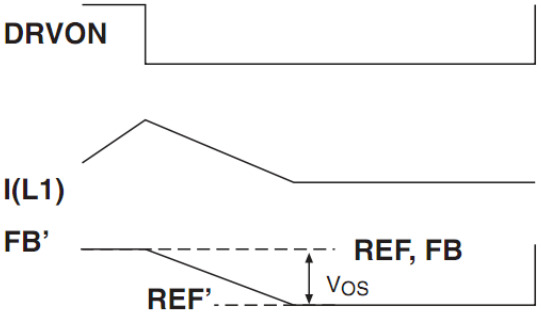
V_{OUT}= V_{OUT} pin voltage

To accommodate the use of ceramic and other low ESR capacitors, an open loop ramp is added to the feedback signal to mimic the inductor current ripple. The following waveforms describe the ideal ramp operation in both CCM and DCM operation.

RAMP: CCM OPERATION



RAMP: DCM OPERATION



In either CCM or DCM, the negative going ramp voltage (V_{RAMP} in the functional diagram) is added to FB and this creates the FB's signal. This FB signal is applied to the negative terminal of the loop comparator. The REF voltage of 0.8V is applied to the positive terminal of the loop comparator plus an offset voltage V_{os} to compensate for the DC level of V_{RAMP} applied to the negative terminal. The result is an internal ramp with enough negative going offset (approximately 50mV) to trip the loop comparator whenever FB falls below regulation.

The output of the loop comparator, a rising VOLOW, causes a SET if BLANK = 0 and OVR_I = 0. This starts inductor charging (DRVON = 1) and starts the minimum on-timer. The minimum on-timer times out and indicates DRVON can be reset if the voltage loop is satisfied. If V_{OUT} is still below the regulation point, RESET is held low until V_{OUT} is above regulation. Once RESET occurs, T_{ON} minimum is reset, and the T_{OFF} one-shot is triggered to blank the loop comparator from starting a new charge cycle for a minimum

period. This blanking period occurs during the noisy LX transition to discharge, where spurious comparator states may occur. For $T_{OFF} > T_{BLANK}$, the loop is in a discharge or wait state until the loop comparator starts the next charge cycle by DRVON going high.

If an over current condition occurs during charge, the loop is interrupted and DRVON is RESET. The off-time one-shot pulse width is widened to $T_{OFF} = K_{OFF} / V_{OUT}$, which holds the loop in discharge for that time. At the end of the off-time, the loop is released and controlled by VOLOW. In this manner maximum inductor current is controlled on a cycle-by-cycle basis. An assertion of UVLO (undervoltage lockout) or TSD (thermal shutdown) holds the loop in no-charge until the fault has ended.

ON-TIME CONTROL - DISCHARGE PHASE

The discharge phase follows with the high side PMOS switch opening and the low side NMOS switch closing to provide a discharge path for the inductor current. The decreasing inductor current and the load current cause the output voltage to drop. Under normal load conditions when the inductor current is below the programmed limit, the off-time will continue until the output voltage falls below the regulation threshold, which initiates a new charge cycle via the loop comparator.

The inductor current "floats" in continuous conduction mode. During this mode the inductor peak current is below the programmed limit and the valley current is above zero. This is to satisfy load currents that are greater than half the minimum current ripple. The current ripple, I_{LR}, is defined by the equation:

$$I_{LR} \approx \frac{K_{ON}}{L} \times \frac{V_{IN} - V_{OUT} - I_{OUT} - R_{CH}}{V_{IN} - V_{OUT}}$$

where:

L = Inductor value

I_{OUT}= Load current

R_{CH}= PMOS on resistance, 0.3 Ωtyp.

If the $I_{OUT} * R_{CH}$ term is negligible compared with (V_{IN} - V_{OUT}), the above equation simplifies to:

$$I_{LR} \approx \frac{K_{ON}}{L}$$

For most applications, the inductor current ripple controlled by the SP6655 is constant regardless of input and output voltage.

The maximum loop frequency in CCM is defined by the equation:

$$F_{LP} \approx \frac{(V_{IN} - V_{OUT}) \times (V_{OUT} + I_{OUT} \times R_{DC})}{K_{ON} \times (V_{IN} + I_{OUT} \times (R_{DC} - R_{CH}))}$$

where:

F_{LP}= CCM loop frequency

R_{DC}= NMOS on resistance, 0.3 Ωtyp.

Ignoring conduction losses simplifies the loop frequency to:

$$F_{LP} \approx \frac{1}{K_{ON}} \times \frac{V_{OUT}}{V_{IN}} \times$$

AND'ing the loop comparator and the on-timer reduces the switching frequency for load currents below half the inductor ripple current. This increases light load efficiency. The minimum on-time insures that the inductor current ripple is a minimum of K_{ON}/L, more than the load current demands. The converter goes in to a standard pulse frequency modulation (PFM) mode where the switching frequency is proportional to the load current.

LOW DROPOUT AND LOAD TRANSIENT OPERATION

AND'ing the loop comparator also increases the duty ratio past the ideal D= V_{OUT} /V_{IN} up to and including 100%. Under a light to heavy load transient, the loop comparator will hold the main switch on longer than the minimum on timer until the output is brought back into regulation.

Also, as the input voltage supply drops down close to the output voltage, the main MOSFET resistance loss will dictate a much higher duty ratio to regulate the output. Eventually as the input voltage drops low enough, the output voltage will follow, causing the loop

comparator to hold the converter at 100% duty cycle.

This mode is critical in extending battery life when the output voltage is at or above the minimum usable input voltage. The dropout voltage is the minimum (V_{IN} -V_{OUT}) below which the output regulation cannot be maintained. The dropout voltage of SP6655 is equal to I_L* (0.3Ω+ R_{L1}) where 0.3Ω is the typical $R_{DS(ON)}$ of the P-Channel MOSFET and R_L is the DC resistance of the inductor.

The SP6655 has been designed to operate in dropout with a light load I_q of only 80µA. The on-time control circuit seamlessly operates the converter between CCM, DCM, and low dropout modes without the need for compensation. The converter's transient response is quick since there is no compensated error amplifier in the loop.

INDUCTOR OVER-CURRENT PROTECTION

To reduce the light load dropout I_q, the SP6655 over-current system is only enabled when I_{L1} > 400mA. The inductor overcurrent protection circuitry is programmed to limit the peak inductor current to 0.625A. This is done during the on-time by comparing the source to drain voltage drop of the PMOS passing the inductor current with a second voltage drop representing the maximum allowable inductor current. As the two voltages become equal, the over-current comparator triggers a minimum off-time one shot. The off-time one shot forces the loop into the discharge phase for a minimum T_{OFF} time causing the inductor current to decrease. At the end of the off-time, loop control is handed back to the AND'd on-time signal. If the output voltage is still low, charging begins until the output is in regulation or the current limit has been reached again. During startup and over-load conditions, the converter behaves like a current source at the programmed limit minus half the current ripple. The minimum T_{OFF} is controlled by the equation:

$$T_{OFF}(MIN) = \frac{K_{OFF}}{V_{OUT}}$$

UNDER-VOLTAGE LOCKOUT

The SP6655 is equipped with a programmable under-voltage lockout to protect the input battery source from excessive currents when substantially discharged. When the input supply is below the UVLO threshold, both power switches are open to prevent inductor current from flowing. The three levels of falling input voltage UVLO threshold have a typical hysteresis of 120mV to prevent chattering due to the impedance of the input source. During UVLO, BLON is forced low.

UNDER-CURRENT DETECTION

The synchronous rectifier is comprised of an inductor discharge switch, a voltage comparator, and a driver latch. During the offtime, positive inductor current flows into the PGND pin 9 through the low side NMOS switch to LX pin 10, through the inductor and the output capacitor, and back to pin 9. The comparator monitors the voltage drop across the discharge NMOS. As the inductor current approaches zero, the channel voltage sign goes from negative to positive, causing the comparator to trigger the driver latch and open the switch to prevent inductor current reversal. This circuit along with the on-timer puts the converter into PFM mode and improves light load efficiency when the load current is less than half the inductor ripple current defined by K_{ON}/L.

THERMAL SHUTDOWN

The converter will open both power switches if the die junction temperature rises above 140°C. The die must cool down below 126°C before the regulator is re-enabled. This feature protects the SP6655 and surrounding circuitry from excessive power dissipation due to fault conditions.

SHUTDOWN/ENABLE CONTROL

The D0, D1 pins 4, 5 of the device are logic level control pins that shut down the converter when both are a logic low, or enable the converter when either are a logic high. When the converter is shut down, the power switches are opened and all circuit biasing is extinguished leaving only junction leakage

currents on supply pins 1 and 2. After pins 4 or 5 are brought high to enable the converter, there is a turn on delay to allow the regulator circuitry to re-establish itself. Power conversion begins with the assertion of the internal reference ready signal which occurs approximately 150µs after the enable signal is received.

BATTERY LOW INDICATOR

The BLON function is a differential measurement of (V_{IN} -V_{OUT}) which causes the open drain NMOS on pin 3 to sink current to ground when (V_{IN} -V_{OUT}) < 300mV. Tying a resistor from pin 3 to V_{IN} or V_{OUT} creates a logic level battery low indicator. A low bandwidth comparator and 3% hysteresis filter the input voltage ripple to prevent noisy transitions at the threshold. BLON is forced Low when in UVLO.

EXTERNAL FEEDBACK PIN

The FB pin 6 is compared to an internal reference voltage of 0.8V to regulate the SP6655 output. The output voltage can be externally programmed within the range +1.0V to +5.0V by tying a resistor from FB to ground and FB to V_{OUT} (pin7). See the applications section for resistor selection information.

APPLICATION INFORMATION

INDUCTOR SELECTION

The SP6655 uses a specially adapted minimum on-time control of regulation utilizing a precision comparator and bandgap reference. This adaptive minimum on-time control has the advantage of setting a constant current ripple for a given inductor size. From the operations section it has been shown:

Inductor Current Ripple, $I_{LR} \approx K_{ON} / L$

For the typical SP6655 application circuit with inductor size of 10µH, and K_{ON} of 2V*µsec, the SP6655 current ripple would be about 200mA, and would be fairly constant for different input and output voltages, simplifying the selection of components for the SP6655 power circuit. Other inductor values could be selected, as shown in Table 1 Components Selection. Using a larger value than 10µH in an attempt to reduce output voltage ripple would reduce inductor current ripple and may not produce as stable an output ripple. For larger inductors with the SP6655, which has a peak inductor current of 0.625A, most 15µH or 22µH inductors would have to be of larger physical sizes, limiting their use in small portable applications. Smaller values like 10µH would more easily meet the 0.625A limit and come in small case sizes, and the increased inductor current ripple of almost 200mA would produce very stable regulation and fast load transient response at the expense of slightly reduced efficiency.

Other inductor parameters are important, such as the inductor current rating and the DC resistance. When the current through the inductor reaches the level of I_{SAT}, the inductance drops to 70% of the nominal value. This non-linear change can cause stability problems or excessive fluctuation in inductor current ripple. To avoid this, the inductor should be selected with saturation current at least equal to the maximum output current of the converter plus half the inductor current ripple. To provide the best performance in dynamic conditions such as start-up and load transients, inductors should be chosen with saturation current close to the SP6655 inductor current limit of 0.625A.

DC resistance, another important inductor characteristic, directly affects the efficiency of the converter, so inductors with minimum DC resistance should be chosen for high efficiency designs. Recommended inductors with low DC resistance are listed in Table 2. Preferred inductors for on board power supplies with the SP6655 are magnetically shielded types to minimize radiated magnetic field emissions.

INDUCTORS - SURFACE MOUNT							
Inductance (uH)	Manufacturer/Part No.	Inductor Specification: Series R (ohms)	Isat (A)	Size: Lx W (mm)	Size: Ht. (mm)	Inductor Type	Manufacturer Website
4.7	Murata LQH32CN4R7M53L	0.150	0.65	3.2x2.5	1.55	Unshielded Ferrite Core	www.murata.com
4.7	Murata LQH31CN4R7M03L	0.65	0.34	3.2x1.6	1.8	Unshielded Ferrite Core	www.murata.com
4.7	Murata LQH2MCN4R7M02L	0.80	0.30	2.0x1.6	0.9	Unshielded Ferrite Core	www.murata.com
10	**Murata LQH32CN100K53L**	**0.300**	**0.45**	**3.2x2.5**	**1.55**	**Unshielded Ferrite Core**	www.murata.com
10	TDK RLF5018T-100MR94	0.056	0.94	5.6x5.2	2.0	Shielded Ferrite Core	www.tdk.com
10	Coilcraft LPO6013-103K	0.300	0.70	6.0x5.4	1.3	Unshielded Ferrite Core	www.coilcraft.com
22	Murata LQH32CN220K21	0.710	0.25	3.2x2.5	2.0	Unshielded Ferrite Core	www.murata.com
22	TDK RLF5018T-220MR63	0.130	0.63	5.6x5.2	2.0	Shielded Ferrite Core	www.tdk.com
22	Coilcraft LPO6013-223K	0.520	0.45	6.0x5.4	1.3	Unshielded Ferrite Core	www.coilcraft.com
CAPACITORS - SURFACE MOUNT							
Capacitance (uF)	Manufacturer/Part No.	Capacitor Specification: ESR (ohms (max))	Ripple Current (A) @ 45C	Size: L x W (mm)	Size: Ht. (mm)	Voltage (V)	Capacitor Type	Manufacturer Website
10	**TDK C2012X5R0J106M**	**0.003**	**1.00**	**2.0x1.2**	**1.25**	**6.3**	**X5R Ceramic**	www.tdk.com
10	Murata GRM21BR60J106KE01	0.003	1.00	2.0x1.2	1.25	6.3	X5R Ceramic	www.murata.com
4.7	TDK C2012X5R0J475M	0.005	1.00	2.0x1.2	1.25	6.3	X5R Ceramic	www.tdk.com
4.7	Murata GRM21BR60J475KE01	0.005	1.00	2.0x1.2	1.25	6.3	X5R Ceramic	www.murata.com

Table 2: Component Selection

Note: Components highlighted in bold are those used on the SP6655 Evaluation Board

CAPACITOR SELECTION

The SP6655 has been designed to work with very low ESR output capacitors (listed in Table 1 Component Selection) which for the typical application circuit are 10µF ceramic capacitors. These capacitors combine small size, low ESR and good value. To regulate the output with low ESR capacitors of 0.01Ω or less, an internal ramp voltage V_{RAMP} has been added to the FB signal to reliably trip the loop comparator (as described in the Operations section).

The output capacitor is required to keep the output voltage ripple small and to ensure regulation loop stability. The output capacitor must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and high ripple current. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} <= \frac{V_{OUT} \cdot (VINMax - V_{OUT})}{(VINMax * L * f_{OSC})} * \left\{ESR + \frac{1}{(8 * f_{OSC} * C_{OUT})}\right\}$$

To improve stability, a small ceramic capacitor, C_F = 22pF should be paralleled with the feedback voltage divider RF, as shown on the typical application schematic on page 1. Another function of the output capacitance is to hold up the output voltage during the load transients and prevent excessive overshoot and undershoot. The typical performance characteristics curves show very good load step transient response for the SP6655 with the recommended output capacitance of 10µF ceramic.

The input capacitor will reduce the peak current drawn from the battery, improve efficiency and significantly reduce high frequency noise induced by a switching power

supply. The typical input capacitor for the SP6655 is 10µF ceramic. These capacitors will provide good high frequency bypassing and their low ESR will reduce resistive losses for higher efficiency. An RC filter is recommended for the V_{IN} pin 2 to effectively reduce the noise for the IC's analog supply rail which provides power to sensitive circuits. This time constant needs to be at least 5 times greater than the switching period, which is calculated as 1/FLP during the CCM mode. The typical application schematic uses the values of R_{VIN} = 10Ω and C_{VIN}= 1 µF to meet these requirements.

Output Voltage Program

The output voltage is programmed by the external divider, as shown in the typical application circuit on page 1. First pick a value for R_I that is no larger than 300KΩ. Too large a value of R_I will reduce the AC voltage seen by the loop comparator, since the internal FB pin capacitance can form a low pass filter with R_F in parallel with R_I. The formula for R_F with a given R_I and output voltage is:

$$R_F = \left(\frac{V_{OUT}}{0.8V} - 1 \right) \bullet R_I$$

Output Voltage Ripple Frequency

An important consideration in a power supply application is the frequency value of the output ripple. Given the control technique of the SP6655 (as described in the operations section), the frequency of the output ripple will vary when in light to moderate load in the discontinuous or PFM mode. For moderate to heavy loads greater than about 100mA inductor current ripple, (for the typical 10µH inductor application on 100mA is half the 200mA inductor current ripple), the output ripple frequency will be fairly constant. From the operations section, this maximum loop frequency in continuous conduction mode is:

$$F_{LP} \approx \frac{1}{K_{ON}} * \frac{V_{OUT}}{V_{IN}} * (V_{IN} - V_{OUT})$$

Data for loop frequency, as measured from output voltage ripple frequency, can be found in the typical performance curves.

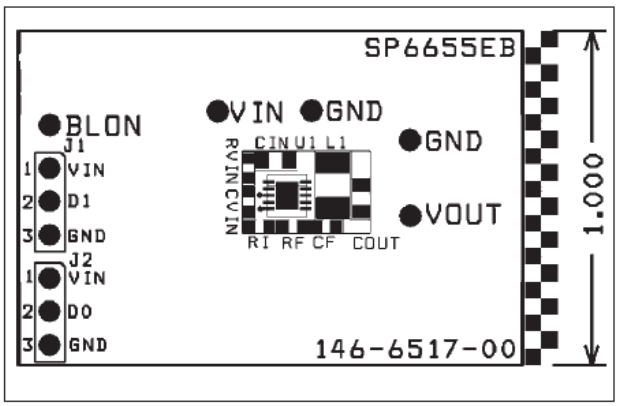
Layout Considerations

Proper layout of the power and control circuits is necessary in a switching power supply to obtain good output regulation with stability and a minimum of output noise. The SP6655 application circuit can be made very small and reside close to the IC for best performance and solution size, as long as some layout techniques are taken into consideration. To avoid excessive interference between the SP6655 high frequency converter and the other active components on the board, some rules should be followed. Refer to the typical application schematic on page 1 and the sample PCB layout shown in the following figures to illustrate how to layout a SP6655 power supply.

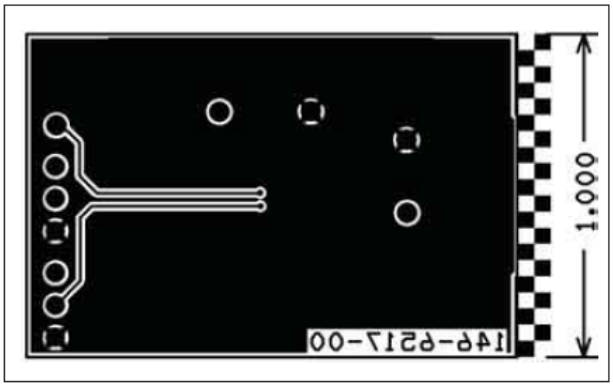
Avoid injecting noise into the sensitive part of circuit via the ground plane. Input and output capacitors conduct high frequency current through the ground plane. Separate the control and power grounds and connect them together at a single point. Power ground plane is shown in the figure titled PCB top sample layout and connects the ground of the C_{OUT} capacitor to the ground of the C_{IN} capacitor and then to the PGND pin 10. The control ground plane connects from pin 9 GND to ground of the C_{VIN} capacitor and the R_I ground return of the feedback resistor. These two separate control and power ground planes come together in the figure titled PCB top sample layout where SP6655 pin 9 GND is connected to pin 10 PGND.

Power loops on the input and output of the converter should be laid out with the shortest and widest traces possible. The longer and narrower the trace, the higher the resistance and inductance it will have. The length of traces in series with the capacitors increases their ESR and ESL and reduces their effectiveness at high frequencies. Therefore, put the 1µF bypass capacitor as close to the V_{IN} and GND pins of the converter as possible, the 10µF C_{IN} close to the P_{VIN} pin and the 10µF output capacitor as close to the inductor as possible. The external voltage feedback network R_F, R_I and feedforward capacitor C_F should be placed very close to the FB pin. Any noise traces like the LX pin should be kept

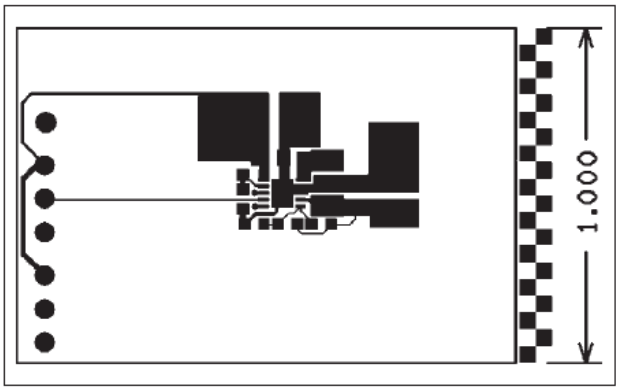
away from the voltage feedback network and separated from it by using power ground copper to minimize EMI.



SP6655 Component Sample Layout

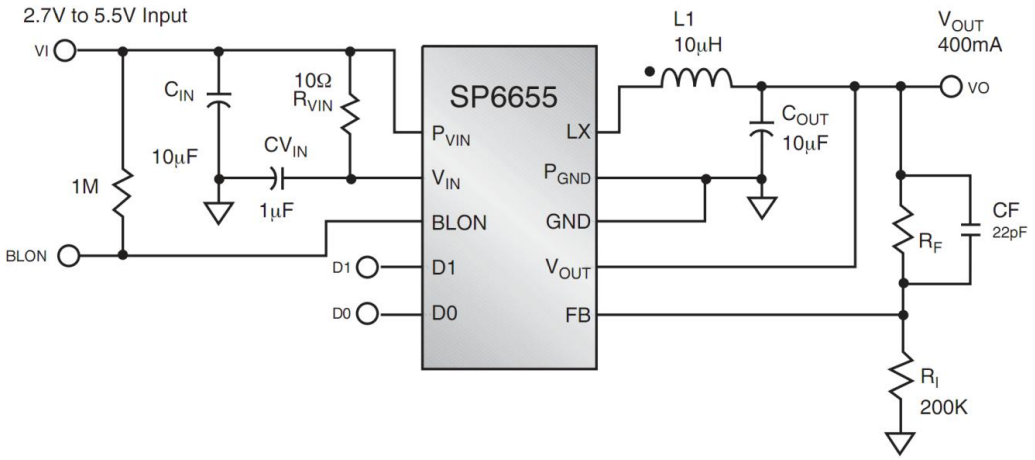


SP6655 PC Layout Bottom Side



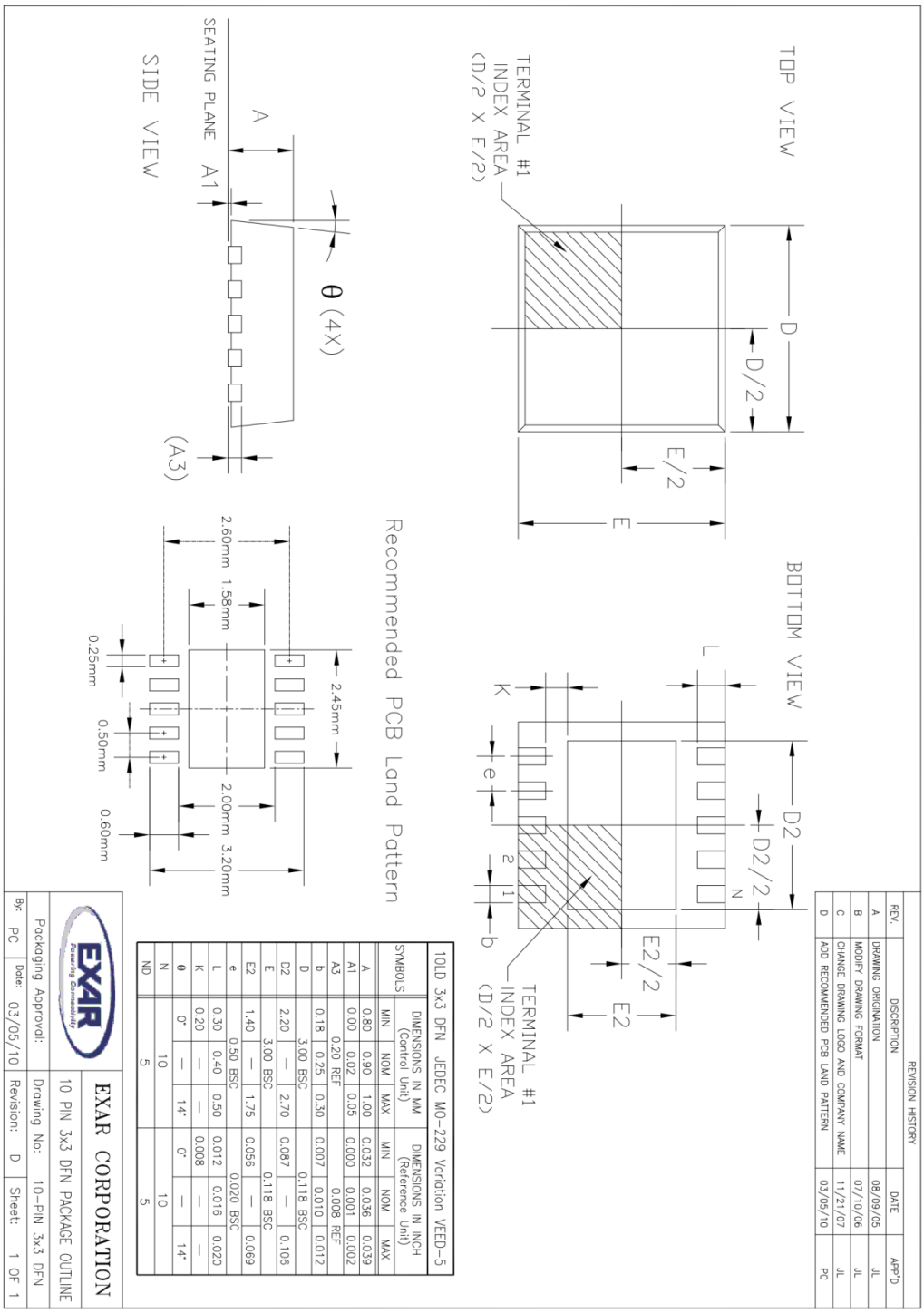
SP6655 PC Layout Top Side

TYPICAL APPLICATIONS



PACKAGE SPECIFICATION

10-PIN DFN



10LD 3x3 DFN JEDEC MO-229 Variation VEED-5								
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)				
	MIN	NOM	MAX	MIN	NOM	MAX		
A	0.80	0.90	1.00	0.032	0.036	0.039		
A1	0.00	0.02	0.05	0.000	0.001	0.002		
A3		0.20 REF			0.008 REF			
b	0.18	0.25	0.30	0.007	0.010	0.012		
D		3.00 BSC			0.118 BSC			
D2	2.20	—	2.70	0.087	—	0.106		
E		3.00 BSC			0.118 BSC			
E2	1.40	—	1.75	0.056	—	0.069		
e		0.50 BSC			0.020 BSC			
L	0.30	0.40	0.50	0.012	0.016	0.020		
K	0.20	—	—	0.008	—	—		
θ	0°	—	14°	0°	—	14°		
N		10			10			
ND		5			5			

EXAR CORPORATION

10 PIN 3x3 DFN PACKAGE OUTLINE

Packaging Approval:		Drawing No:	10-PIN 3x3 DFN	Revision:	D	Sheet:	1 OF 1
By: PC	Date: 03/05/10						

REVISION HISTORY

Revision	Date	Description
2.0.0	12/07/2012	Reformat of Datasheet

FOR FURTHER ASSISTANCE

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NOTICE