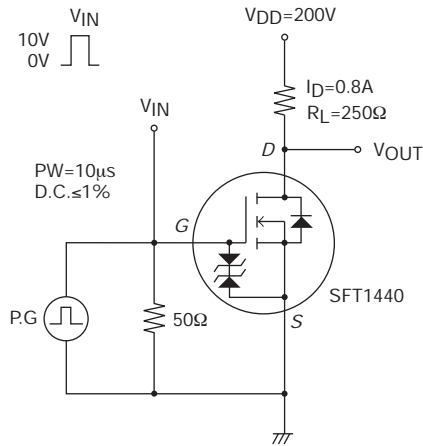


Electrical Characteristics at Ta=25°C

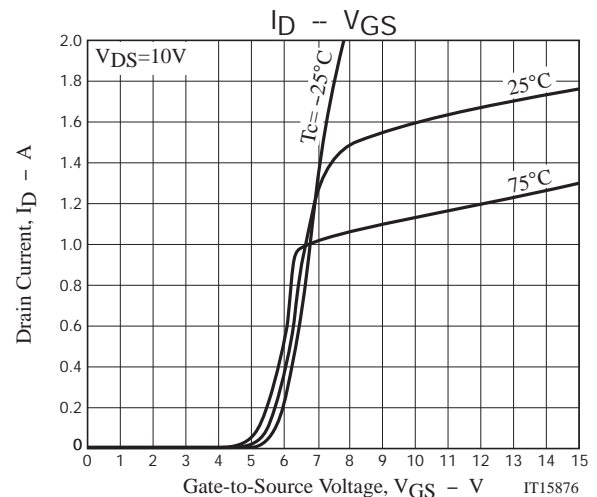
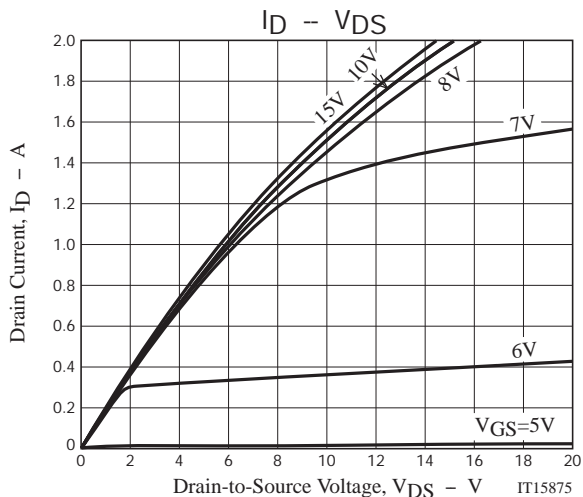
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D=10mA, V_{GS}=0V$	600			V
Zero-Gate Voltage Drain Current	I_{DSS}	$V_{DS}=480V, V_{GS}=0V$			100	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 24V, V_{DS}=0V$			± 10	μA
Cutoff Voltage	$V_{GS(off)}$	$V_{DS}=10V, I_D=1mA$	3.0		5.0	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS}=10V, I_D=0.8A$		1.0		S
Static Drain-to-Source On-State Resistance	$R_{DS(on)1}$	$I_D=0.8A, V_{GS}=10V$		6.2	8.1	Ω
Input Capacitance	C_{iss}	$V_{DS}=30V, f=1MHz$		130		pF
Output Capacitance	C_{oss}			25		pF
Reverse Transfer Capacitance	C_{rss}			4.0		pF
Turn-ON Delay Time	$t_{d(on)}$			9.1		ns
Rise Time	t_r	See specified Test Circuit.		15		ns
Turn-OFF Delay Time	$t_{d(off)}$			18		ns
Fall Time	t_f			19		ns
Total Gate Charge	Q_g	$V_{DS}=300V, V_{GS}=10V, I_D=1.5A$		6.3		nC
Gate-to-Source Charge	Q_{gs}			1.4		nC
Gate-to-Drain "Miller" Charge	Q_{gd}			3.6		nC
Diode Forward Voltage	V_{SD}	$I_S=1.5A, V_{GS}=0V$		0.85	1.2	V

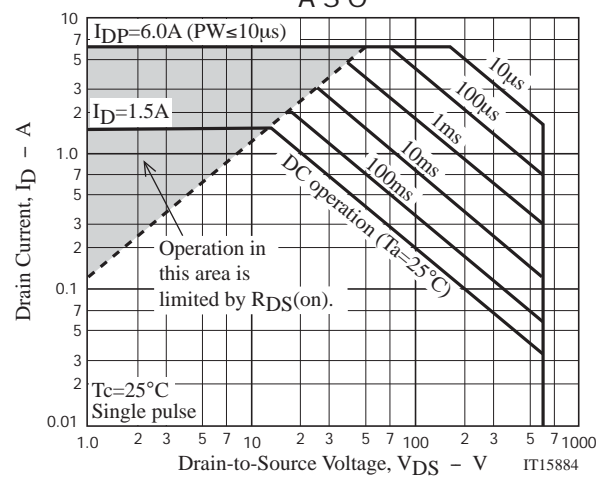
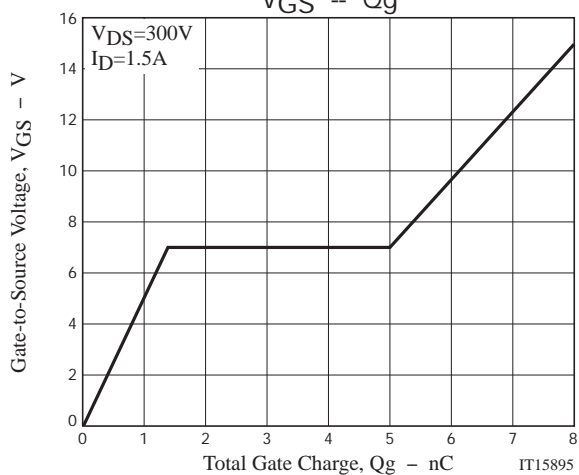
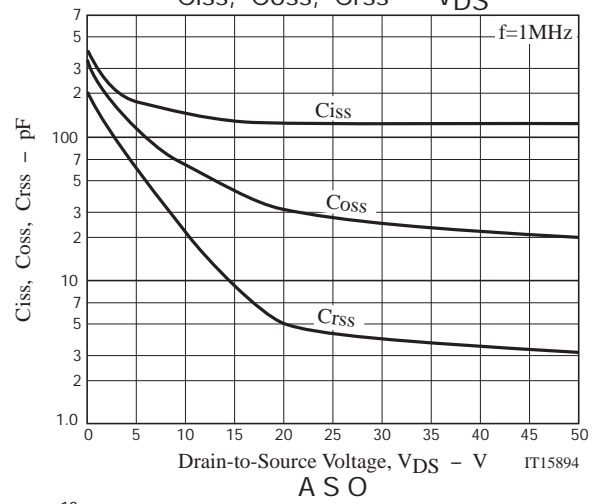
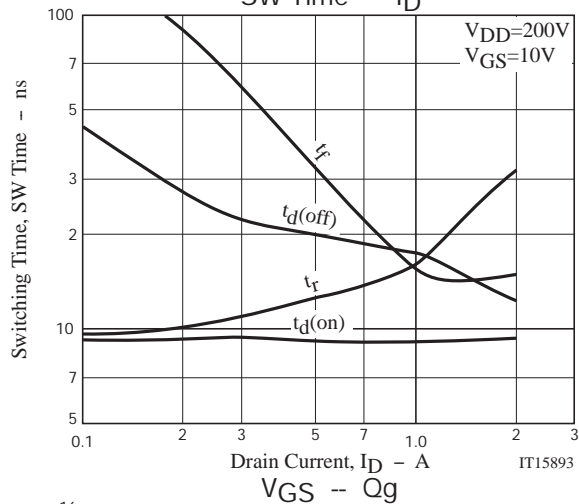
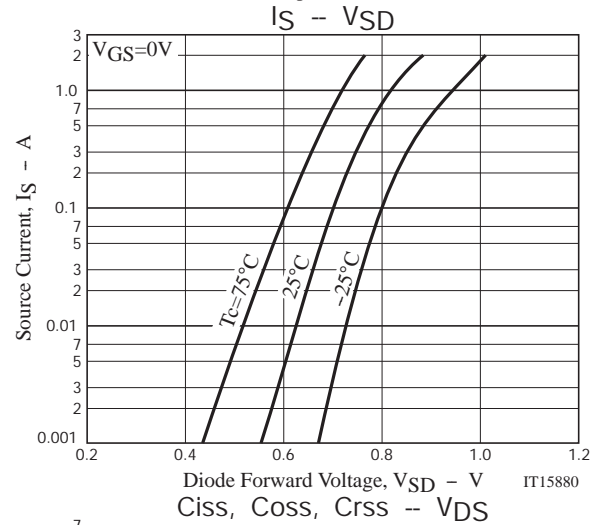
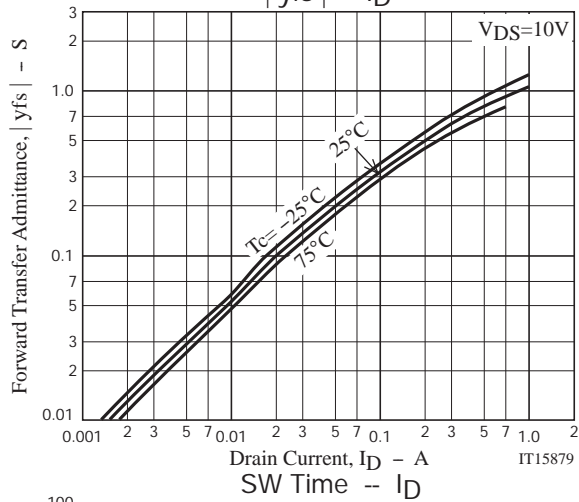
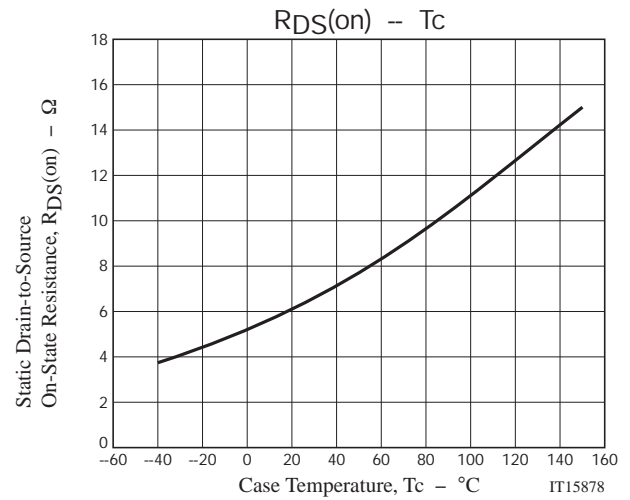
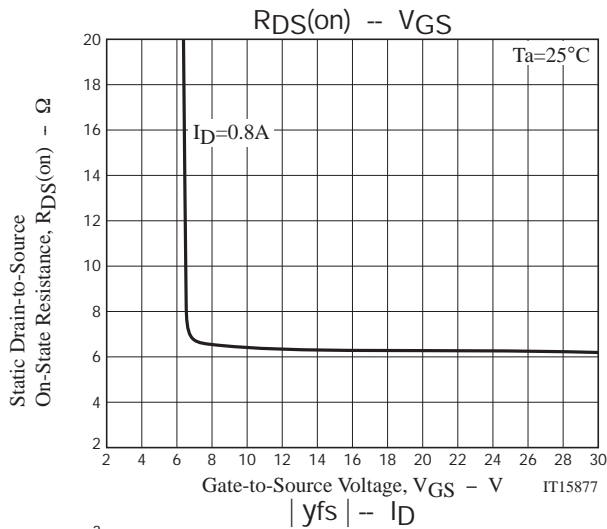
Switching Time Test Circuit

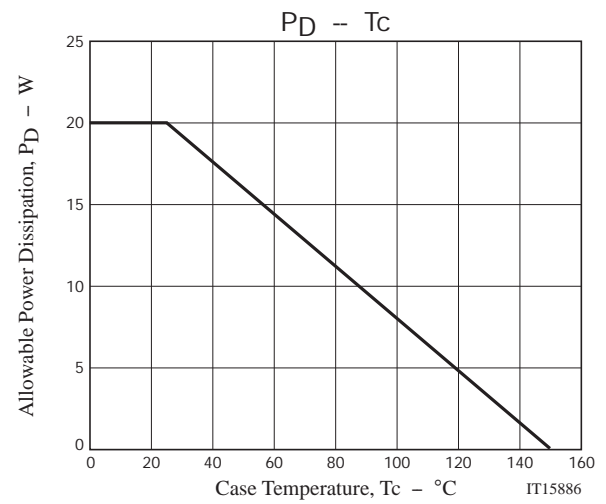
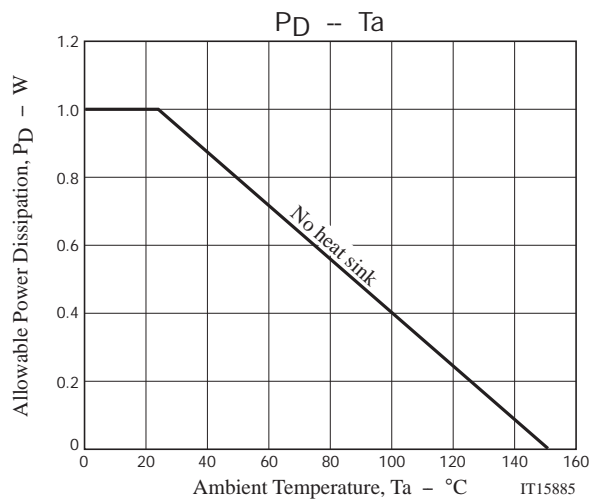


Ordering Information

Device	Package	Shipping	memo
SFT1440-E	TP	500pcs./bag	Pb Free
SFT1440-TL-E	TP-FA	700pcs./reel	







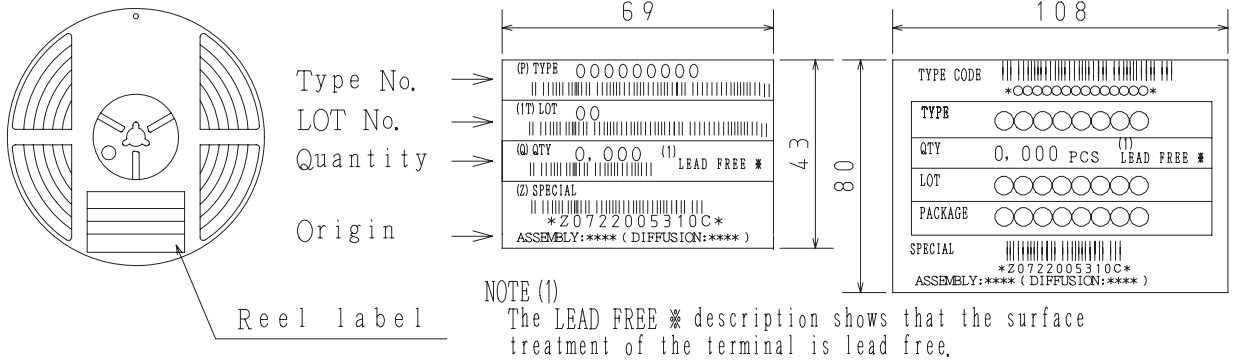
Taping Specification

SFT1440-TL-E

Packing Format

Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	Inner BOX (C-1)	Outer BOX (A-7)
TP-FA	TP	700	2,100	12,600	3 reels contained Dimensions:mm (external) 183×72×185	6 inner boxes contained Dimensions:mm (external) 440×195×210

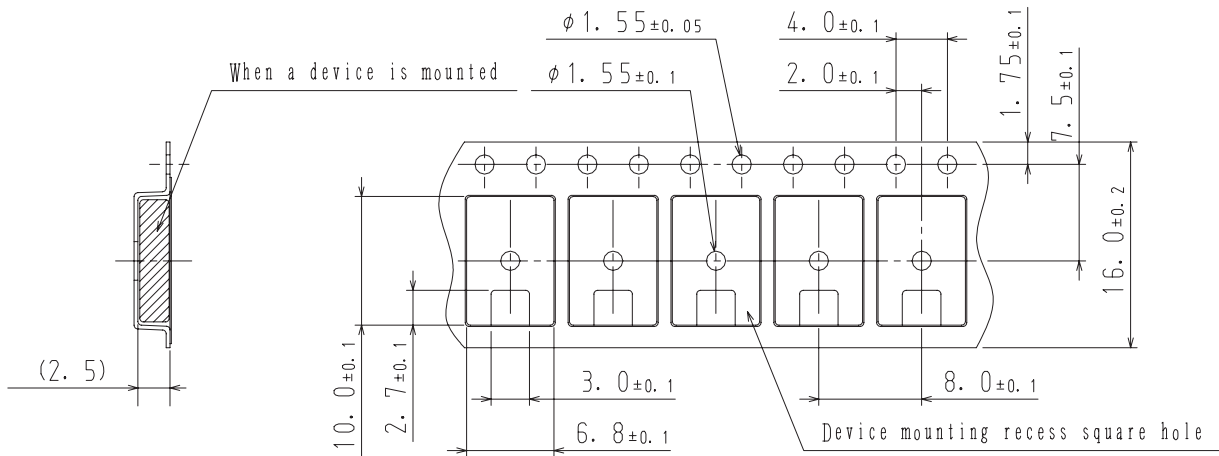
Packing method



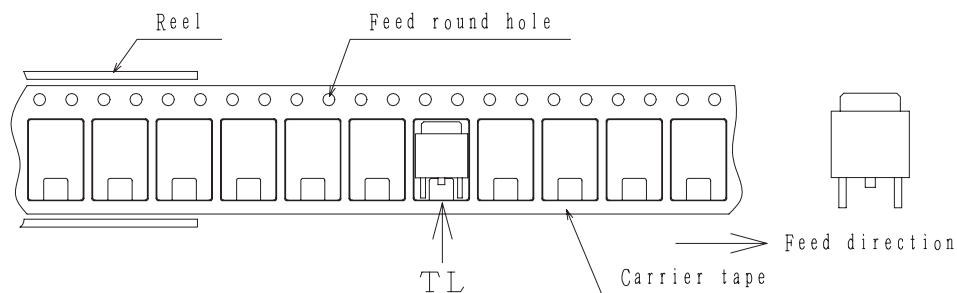
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

Taping configuration

1. Carrier tape size (unit:mm)



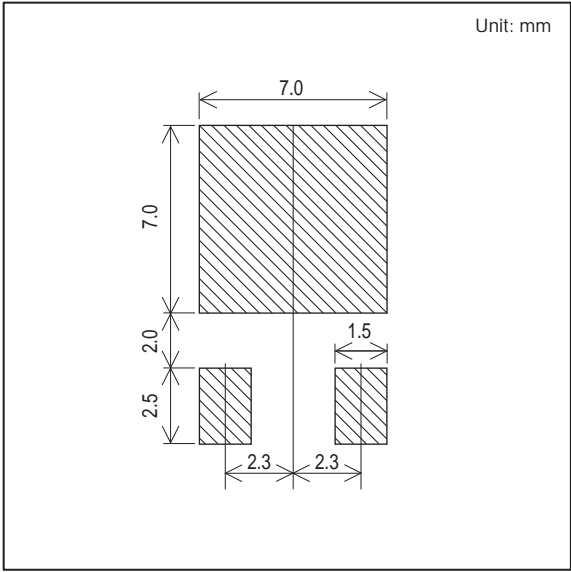
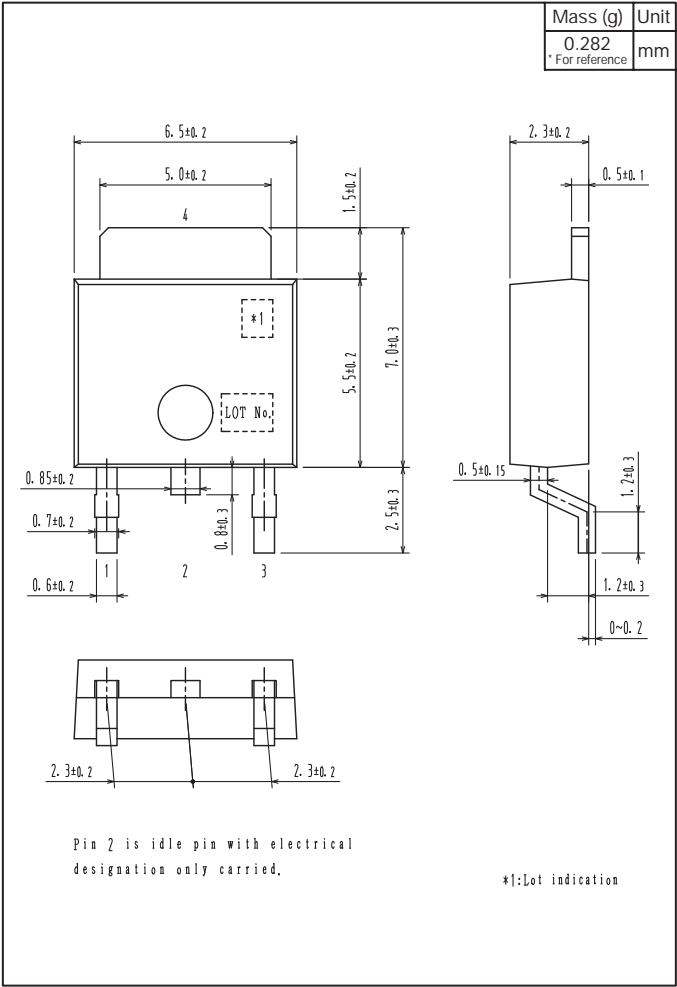
2. Device placement direction



Those with one electrode terminal on the feed hole side.....TL

Outline Drawing
SFT1440-TL-E

Land Pattern Example

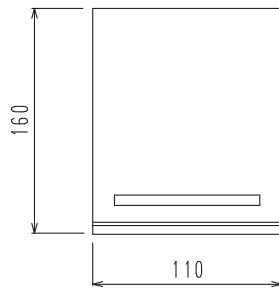


Bag Packing Specification

SFT1440-E

1. Packing Format

Package Name	Maximum Number of devices contained (pcs)			
	Bag	Inner box	Outer box	
TP	500	B-1	A-1	A-2
		10, 000	50, 000	30, 000
		Packing format (Dimensions:mm (external))		
		Inner box	Outer box	
		B-1	A-1	A-2
		445×225×55	470×250×300	470×250×190

2. Bag dimensions
(unit:mm)3. Bag label, Inner box label
(unit:mm)

Type No. →	(P) TYPE 0000000000	69	43
LOT No. →	(T) LOT 00		
Quantity →	(Q) QTY 0,000 (1) LEAD FREE *		
Origin →	(2) SPECIAL *Z0722005310C* ASSEMBLY:**** (DIFFUSION:****)		

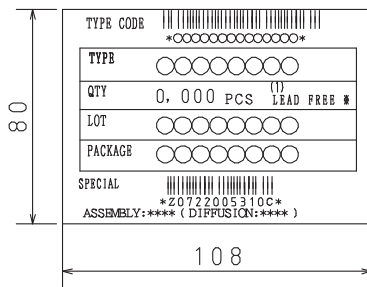
4. Outer box label
(unit:mm)

It is a label at the time of factory shipments.
The form of a label may change in physical
distribution process.

NOTE (1)

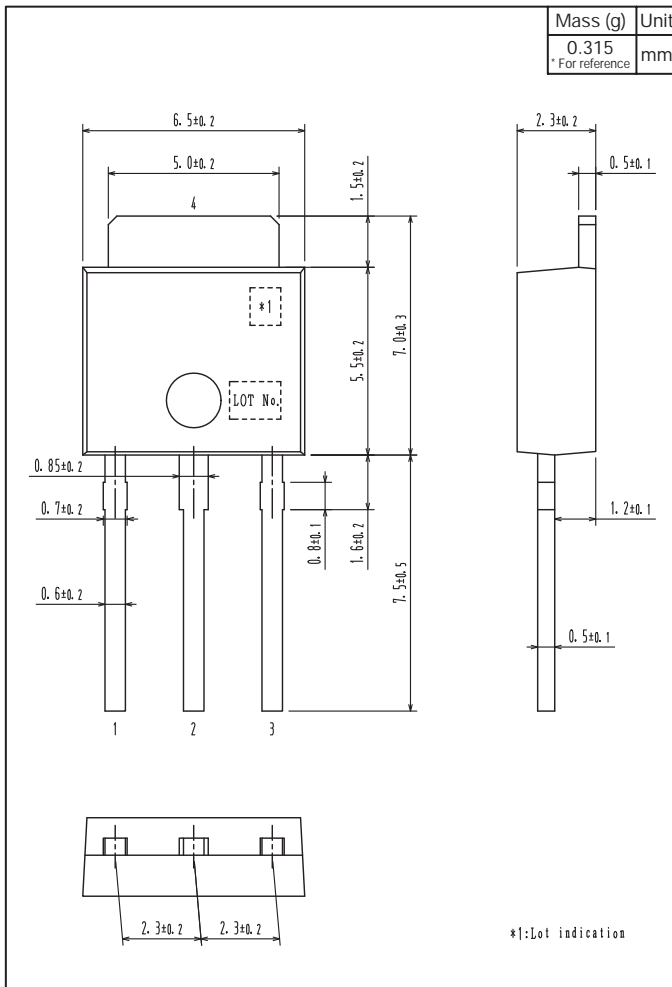
The LEAD FREE * description shows that the
surface treatment of the terminal is lead free.

Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3



Outline Drawing

SFT1440-E



Note on usage : Since the SFT1440 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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