

Pin Descriptions

Pin Name	Type	Pin #	Descriptions
SRC_DIV#	Input	1	3.3V LVTTL input for selecting input frequency divide by 2, active LOW.
SRC & SRC#	Input	4, 5	0.7V Differential SRC input from PI6C410 clock synthesizer
OE [0:7]	Input	6, 7, 14, 15, 35, 36, 43, 44	3.3V LVTTL input for enabling outputs, active HIGH.
OE_INV	Input	40	3.3V LVTTL input for inverting the OE, SRC_STOP# and PWRDWN# pins. When 0 = same stage When 1 = OE[0:7], SRC_STOP#, PWRDWN# inverted.
OUT[0:7] & OUT[0:7]#	Output	8, 9, 12, 13, 16 17, 20, 21, 29, 30, 33, 34, 37, 38, 41, 42	0.7V Differential outputs
PLL/BYPASS#	Input	22	3.3V LVTTL input for selecting fan-out of PLL operation.
SCLK	Input	23	SMBus compatible SCLOCK input
SDA	I/O	24	SMBus compatible SDATA
I _{REF}	Input	46	External resistor connection to set the differential output current
SRC_STOP#	Input	27	3.3V LVTTL input for SRC stop, active LOW
PLL_BW#	Input	28	3.3V LVTTL input for selecting the PLL bandwidth
PWRDWN#	Input	26	3.3V LVTTL input for Power Down operation, active LOW
LOCK	Output	45	3.3V LVTTL output, transition high when PLL lock is achieved (Latched output)
V _{DD}	Power	2, 11, 19, 31, 39	3.3V Power Supply for Outputs
V _{SS}	Ground	3, 10, 18, 25, 32	Ground for Outputs
V _{SS_A}	Ground	47	Ground for PLL
V _{DD_A}	Power	48	3.3V Power Supply for PLL

Serial Data Interface (SMBus)

PI6C20800 is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

Address assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	1	1	0	0/1

Data Protocol⁽¹⁾

1 bit	7 bits	1	1	8 bits	1	8 bits	1	8 bits	1	8 bits	1	1 bit
Start bit	Slave Addr	R/W	Ack	Register offset	Ack	Byte Count = N	Ack	Data Byte 0	Ack	Data Byte N - 1	Ack	Stop bit

Note:

1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

Data Byte 0: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	SRC_DIV# 0 = Divide by 2 1 = Normal	RW	1 = x1	OUT[0:7], OUT[0:7]#	NA
1	PLL/BYPASS# 0 = Fanout 1 = PLL	RW	1 = PLL	OUT[0:7], OUT[0:7]#	NA
2	PLL Bandwidth 0 = HIGH Bandwidth, 1 = LOW Bandwidth	RW	1 = Low	OUT[0:7], OUT[0:7]#	NA
3	TBD				NA
4	TBD				NA
5	TBD				NA
6	SRC_STOP# 0 = Driven when stopped 1 = Tristate	RW	0 = Driven when stopped	OUT[0:7], OUT[0:7]#	
7	PWRDWN# 0 = Driven when stopped 1 = Tristate	RW	0 = Driven when stopped	OUT[0:7], OUT[0:7]#	NA

Data Byte 1: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	OUTPUTS enable 1 = Enabled 0 = Disabled	RW	1 = Enabled	OUT0, OUT0#	NA
1		RW	1 = Enabled	OUT1, OUT1#	NA
2		RW	1 = Enabled	OUT2, OUT2#	NA
3		RW	1 = Enabled	OUT3, OUT3#	NA
4		RW	1 = Enabled	OUT4, OUT4#	NA
5		RW	1 = Enabled	OUT5, OUT5#	NA
6		RW	1 = Enabled	OUT6, OUT6#	NA
7		RW	1 = Enabled	OUT7, OUT7#	NA

Data Byte 2: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	Allow control of OUTPUTS with assertion of SRC_STOP# 0 = Free running 1 = Stopped with SRC_Stop#	RW	0 = Free running	OUT0, OUT0#	NA
1		RW	0 = Free running	OUT1, OUT1#	NA
2		RW	0 = Free running	OUT2, OUT2#	NA
3		RW	0 = Free running	OUT3, OUT3#	NA
4		RW	0 = Free running	OUT4, OUT4#	NA
5		RW	0 = Free running	OUT5, OUT5#	NA
6		RW	0 = Free running	OUT6, OUT6#	NA
7		RW	0 = Free running	OUT7, OUT7#	NA

Data Byte 3: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	TBD	RW			
1		RW			
2		RW			
3		RW			
4		RW			
5		RW			
6		RW			
7		RW			

Data Byte 4: Pericom ID Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	Pericom ID	R	0	NA	NA
1		R	0	NA	NA
2		R	0	NA	NA
3		R	0	NA	NA
4		R	0	NA	NA
5		R	1	NA	NA
6		R	0	NA	NA
7		R	0	NA	NA

Functionality

PWRDWN#	OUT	OUT#	SRC_Stop#	OUT	OUT#
1	Normal	Normal	1	Normal	Normal
0	$I_{REF} \times 2$ or Float	LOW	0	$I_{REF} \times 6$ or Float	LOW

Power Down (PWRDWN# assertion)

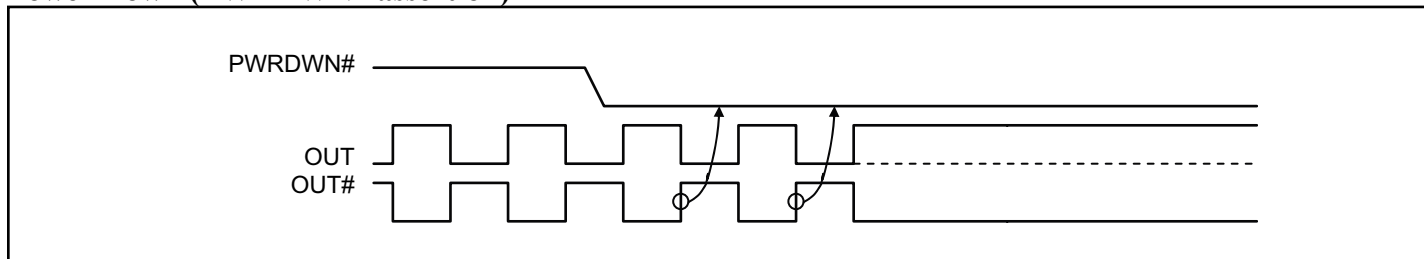


Figure 1. Power down sequence

Power Down (PWRDWN# De-assertion)

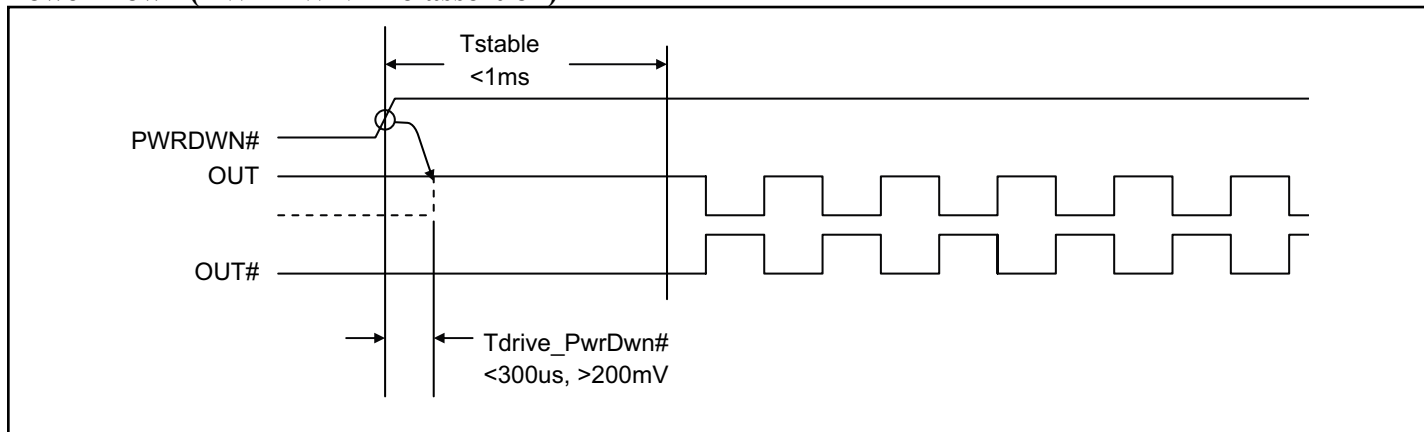


Figure 2. Power down de-assert sequence

Current-mode output buffer characteristics of OUT[0:7], OUT[0:7]#

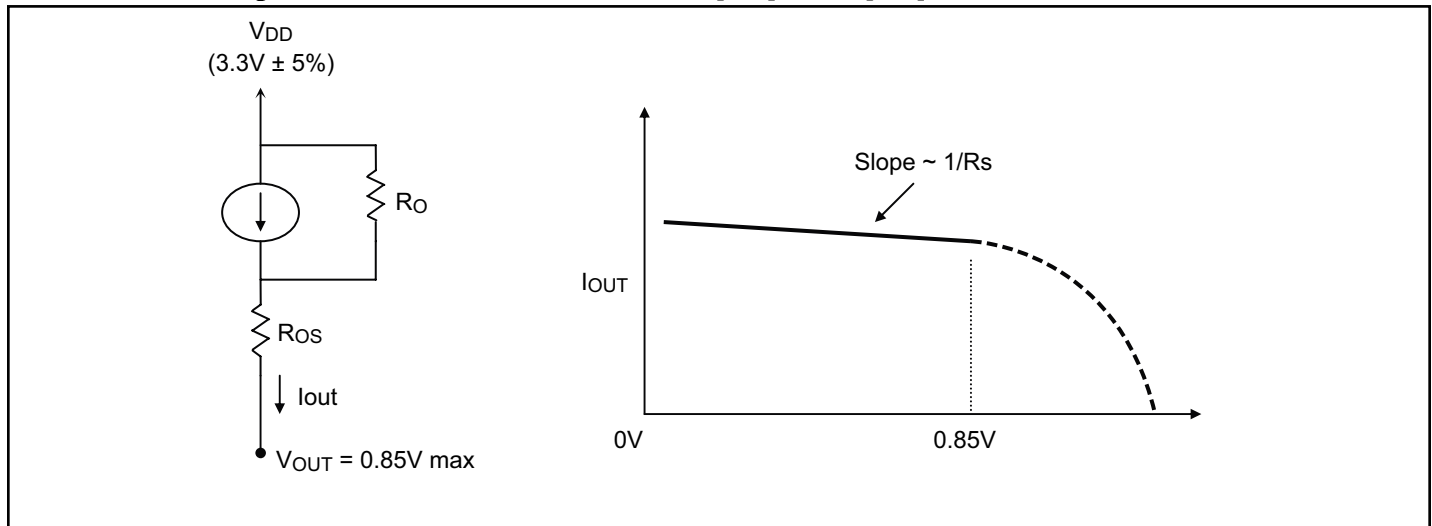


Figure 9. Simplified diagram of current-mode output buffer

Differential Clock Buffer characteristics

Symbol	Minimum	Maximum
R_O	3000 Ω	N/A
R_{OS}	unspecified	unspecified
V_{OUT}	N/A	850mV

Current Accuracy

Symbol	Conditions	Configuration	Load	Min.	Max.
I_{OUT}	$V_{DD} = 3.30 \pm 5\%$	$R_{REF} = 475\Omega$ 1% $I_{REF} = 2.32mA$	Nominal test load for given configuration	-12% $I_{NOMINAL}$	+12% $I_{NOMINAL}$

Note:

1. $I_{NOMINAL}$ refers to the expected current based on the configuration of the device.

Differential Clock Output Current

Board Target Trace/Term Z	Reference R, $I_{ref} = V_{DD}/(3 \times R_r)$	Output Current	$V_{OH} @ Z$
100 Ω (100 Ω differential \approx 15% coupling ratio)	$R_{REF} = 475\Omega$ 1%, $I_{REF} = 2.32mA$	$I_{OH} = 6 \times I_{REF}$	0.7V @ 50

Absolute Maximum Ratings⁽¹⁾ (Over operating free-air temperature range)

Symbol	Parameters	Min.	Max.	Units
V _{DD_A}	3.3V Core Supply Voltage	-0.5	4.6	V
V _{DD}	3.3V I/O Supply Voltage	-0.5	4.6	
V _{IH}	Input HIGH Voltage		4.6	
V _{IL}	Input LOW Voltage	-0.5		
T _s	Storage Temperature	-65	150	°C
V _{ESD}	ESD Protection	2000		V

Note:

- Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

DC Electrical Characteristics (V_{DD} = 3.3±5%, V_{DD_A} = 3.3±5%)

Symbol	Parameters	Condition	Min.	Max.	Units
V _{DD_A}	3.3V Core Supply Voltage		3.135	3.465	V
V _{DD}	3.3V I/O Supply Voltage		3.135	3.465	
V _{IH}	3.3V Input HIGH Voltage	V _{DD}	2.0	V _{DD} + 0.3	
V _{IL}	3.3V Input LOW Voltage		V _{SS} - 0.3	0.8	
I _{IK}	Input Leakage Current	0 < V _{IN} < V _{DD}	-5	+5	μA
V _{OH}	3.3V Output HIGH Voltage	I _{OH} = -1mA	2.4		V
V _{OL}	3.3V Output LOW Voltage	I _{OL} = 1mA		0.4	
I _{OH}	Output HIGH Current	I _{OH} = 6 x I _{REF} , I _{REF} = 2.32mA	12.2	15.6	mA
C _{IN}	Logic Input Pin Capacitance		1.5	5	
C _{OUT}	Output Pin Capacitance			6	pF
L _{PIN}	Pin Inductance			7	nH
I _{DD}	Power Supply Current	V _{DD} = 3.465V, F _{CPU} = 200MHz		250	mA
I _{SS}	Power Down Current	Driven outputs		60	
I _{SS}	Power Down Current	Tristate outputs		12	
T _A	Ambient Temperature		0	70	°C

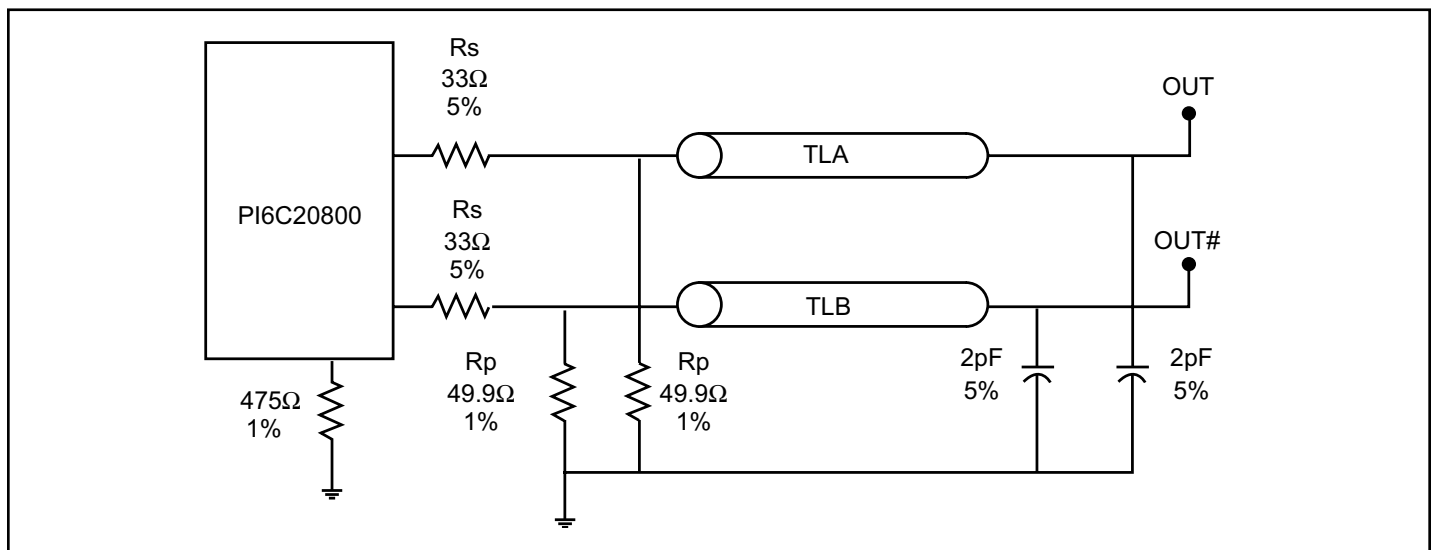
AC Switching Characteristics^(1,2,3) ($V_{DD} = 3.3 \pm 5\%$, $V_{DD_A} = 3.3 \pm 5\%$)

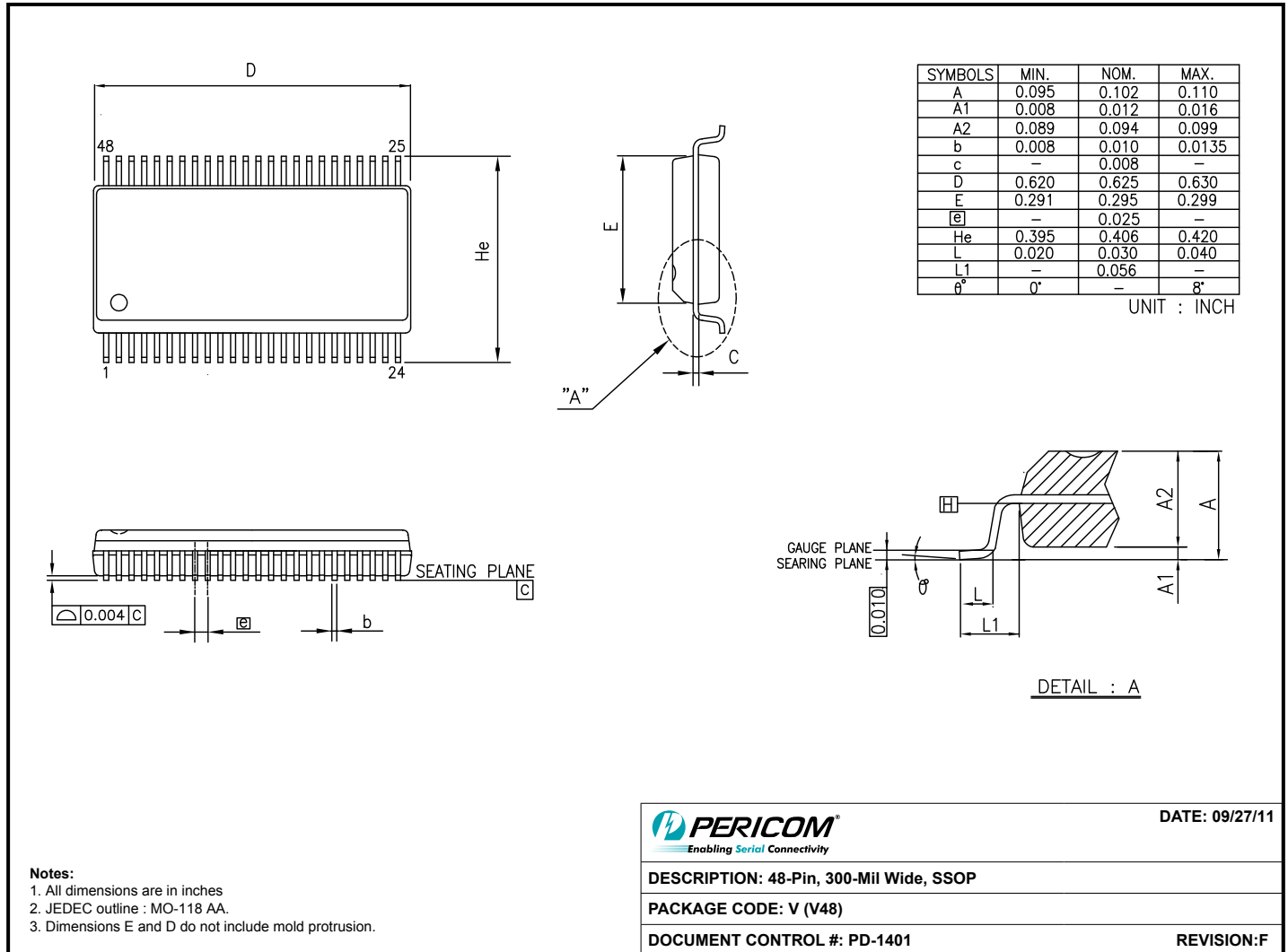
Symbol	Parameters	Min	Max.	Units	Notes
F_{IN}	PLL Mode	100	200	MHz	
	Bypass Mode	100	400	MHz	
T_{rise} / T_{fall}	Rise and Fall Time (measured between 0.175V to 0.525V)	175	700	ps	2
$\Delta T_{rise} / \Delta T_{fall}$	Rise and Fall Time Variation		125		2
T_{skew}	Output-to-Output Skew		50	ps	3
V_{HIGH}	Voltage HIGH	660	850	mV	2
V_{OVS}	Max. Voltage		1150		
V_{UDS}	Min. Voltage	-300			
V_{LOW}	Voltage LOW	-150	+150		2
V_{cross}	Absolute crossing poing voltages	250	550		2
ΔV_{cross}	Total Variation of V_{cross} over all edges		140		2
T_{DC}	Duty Cycle	45	55	%	3
$T_{jycyc-cyc}$	Jitter, Cycle-to-cycle (PLL Mode, Measurement for differential waveform)		50	ps	
	Jitter, Cycle-to-cycle (BYPASS mode as additive jitter)				

Notes:

1. Test configuration is $R_S = 33.2\Omega$, $R_P = 49.9\Omega$, and 2pF.
2. Measurement taken from Single Ended waveform.
3. Measurement taken from Differential waveform.

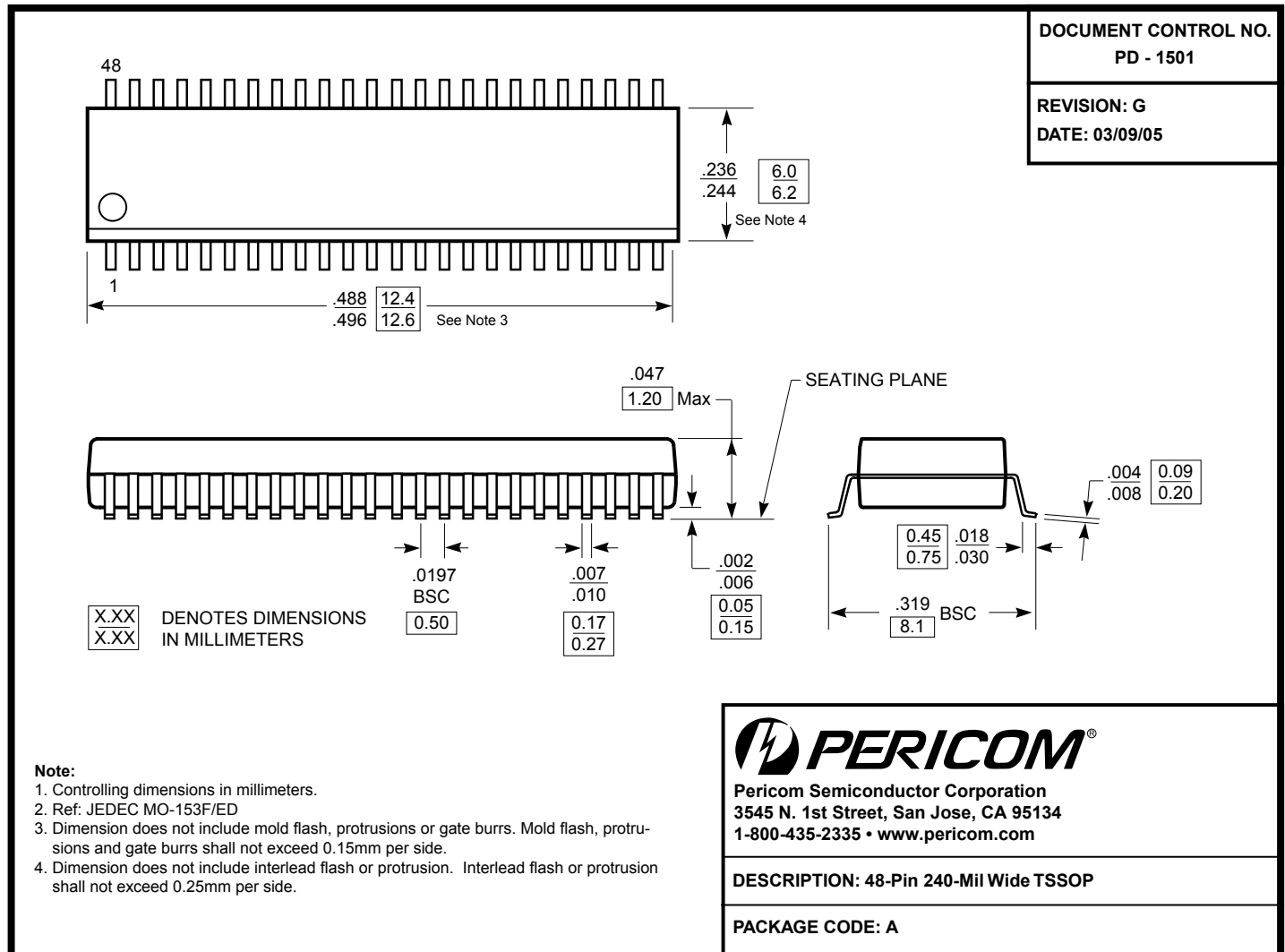
Configuration Test Load Board Termination



Packaging Mechanical: 48-Pin SSOP (V)


11-0197

Packaging Mechanical: 48-Pin TSSOP (A)



Ordering Information^(1,2)

Ordering Code	Package Code	Package Description
PI6C20800VE	V	48-pin, 300-mil wide, SSOP, Pb-Free and Green
PI6C20800AE	A	48-pin, 240-mil wide, TSSOP, Pb-Free and Green

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X suffix = Tape/Reel