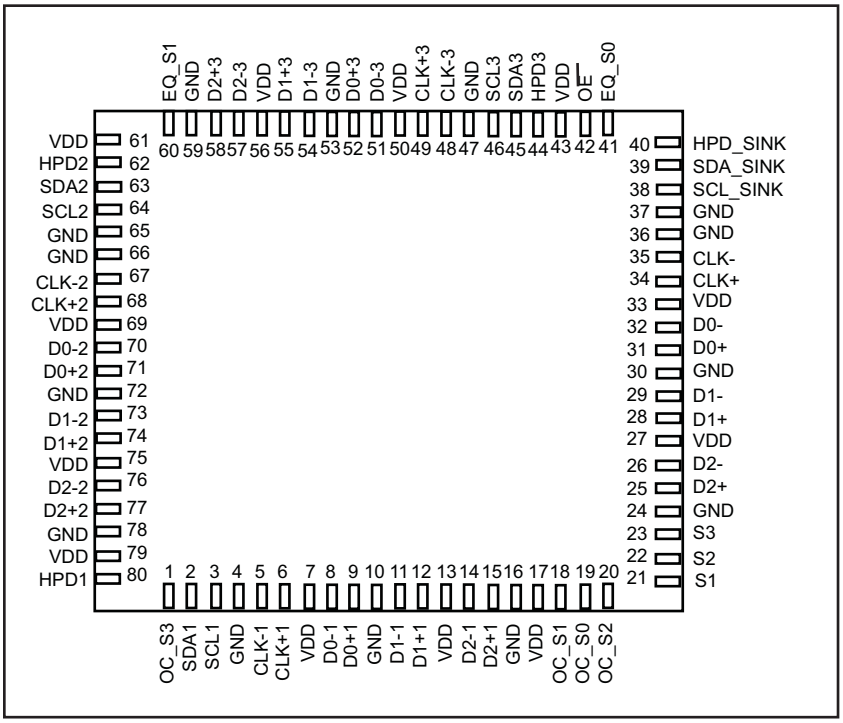
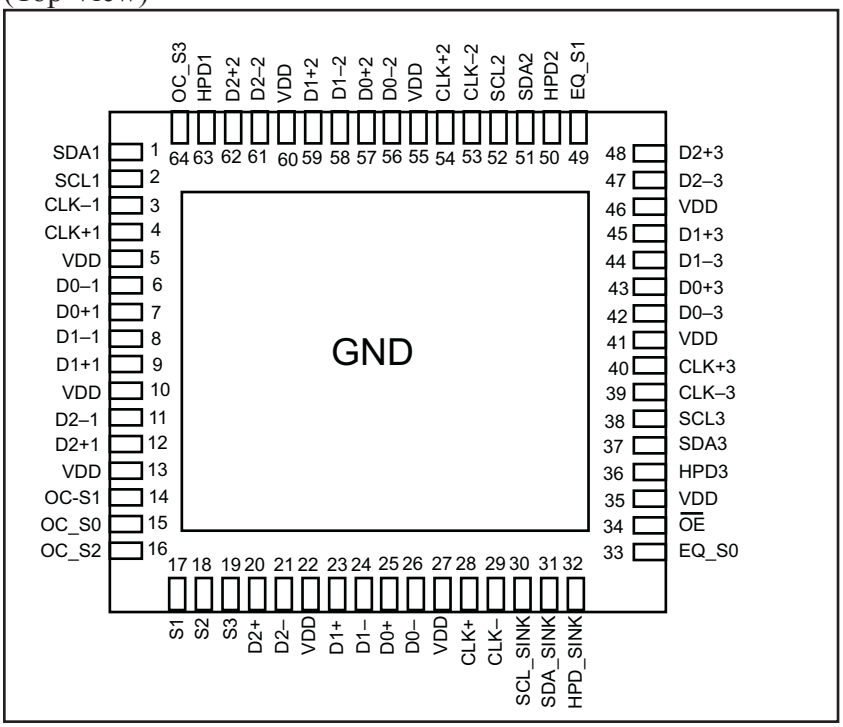
Pin Configuration (Top View)

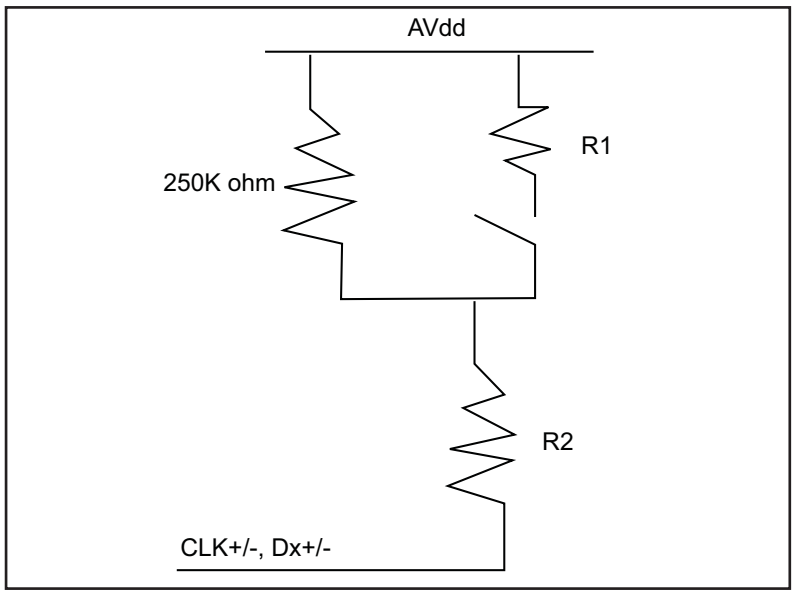


(Top View)



Receiver Block[1]

Each input has integrated equalization that can eliminate deterministic jitter caused by 25meter 24AWG cables. All activity can be configured using pin strapping. The Rx block is designed to receive all relevant signals directly from the HDMI™ connector without any additional circuitry, 3 High speed TMDS data, 1 pixel clock, 1 HPD signals, and DDC signals. TMDS Channels have following termination scheme for Rx Sense support.

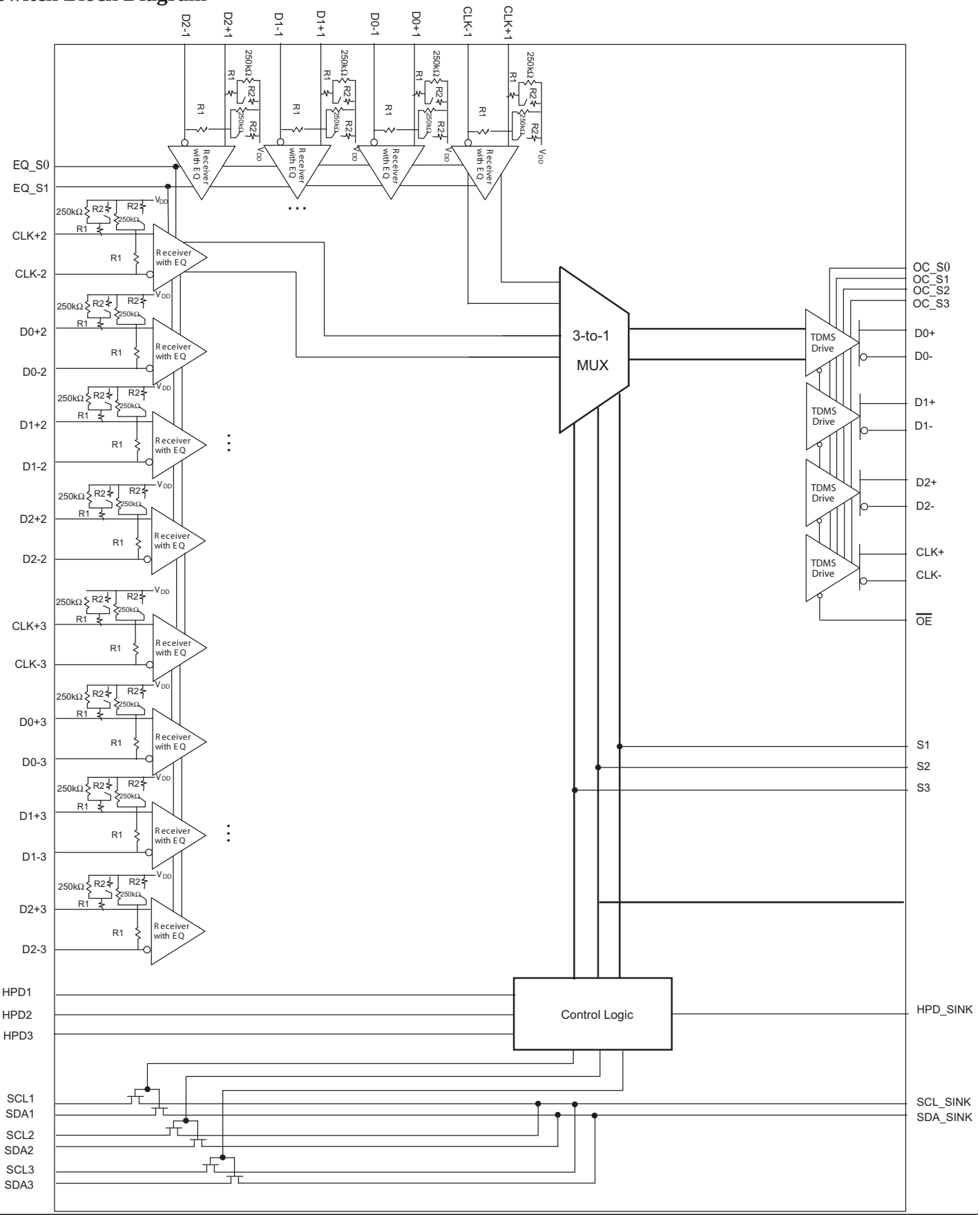


Note:
1. $R_1 + R_2 = 50\ \Omega$

Pin Description

80 LQFP Pin #	64 TQFN Pin #	Pin Name	I/O	Description
9, 12, 15, 6	7, 9,12, 4	D_0+1, D_1+1, D_2+1, CLK+1	I	Port 1 TMDS Positive inputs
71, 74, 77, 68	57, 59, 62, 54	D_0+2, D_1+2, D_2+2, CLK+2	I	Port 2 TMDS Positive inputs
52, 55, 58, 49	43, 45, 48, 40	D_0+3, D_1+3, D_2+3, CLK+3	I	Port 3 TMDS Positive inputs
8, 11, 14, 5	6, 8, 11, 3	D_0-1, D_1-1, D_2-1, CLK-1	I	Port 1 TMDS Negative inputs
70, 73, 76, 67	56, 58, 61, 53	D_0-2, D_1-2, D_2-2, CLK-2	I	Port 2 TMDS Negative inputs
51, 54, 57, 48	42, 44, 47, 39	D_0-3, D_1-3, D_2-3, CLK-3	I	Port 3 TMDS Negative inputs
4, 10, 16, 24, 30, 36, 37, 47, 53, 59, 65, 66, 72, 78		GND		Ground
80	63	HPD1	O	Port 1 HPD output
62	50	HPD2	O	Port 2 HPD output
44	36	HPD3	O	Port 3 HPD output
40	32	HPD_Sink	I	Sink side hot plug detector input. High: 5-V power signal asserted from source to sink and EDID is ready. Low: No 5-V power signal asserted from source to sink, or EDID is not ready.
42	34	$\overline{OE}$	I	Output Enable, Active LOW
3	2	SCL1	I/O	Port 1 DDC Clock
64	52	SCL2	I/O	Port 2 DDC Clock
46	38	SCL3	I/O	Port 3 DDC Clock
38	31	SCL_Sink	I/O	Sink Side DDC Clock
2	1	SDA1	I/O	Port 1 DDC Data
63	51	SDA2	I/O	Port 2 DDC Data
45	37	SDA3	I/O	Port 3 DDC Data
39	31	SDA_Sink	I/O	Sink Side DDC Data
21, 22, 23	17, 18, 19	S1, S2, S3	I	Source Input Control
7, 13, 17, 27, 33, 43, 50, 56, 61, 69, 75, 79	5, 10, 22, 27, 35, 41, 46, 55, 60	V_{DD}		3.3V Power Supply
31, 28, 25, 34	25, 23, 20, 28	D_0+, D_1+, D_2+, CLK+	O	TMDS positive outputs
32, 29, 26, 35	26, 24, 21, 29	D_0-, D_1-, D_2-, CLK-	O	TMDS negative outputs
41, 60	33, 49	EQ_S0, EQ_S1	I	Equalizer controls, both controls have internal pull-ups
19, 18, 20, 1	15, 14, 16, 64	OC_S0, OC_S1, OC_S2, OC_S3	I	Output buffer controls, all control bits have internal pull-ups

Switch Block Diagram



Truth Table

Control Pins				I/O Selected		Hot Plug Detect Status		
$\overline{OE}$	S1	S2	S3	TMDS outputs	SCL_Sink SDA_Sink	HPD1	HPD2	HPD3
L	H	x	x	Port1	SCL1 SDA1	HPD_Sink	L	L
L	L	H	x	Port2	SCL2 SDA2	L	HPD_Sink	L
L	L	L	H	Port3	SCL3 SDA3	L	L	HPD_Sink
L	L	L	L	None (Hi-Z)	None (Hi-Z)	L	L	L
H	X	X	X	None (Hi-Z)	Follow S1, S2, S3	Follow S1, S2, S3		

OC Setting Value Logic Table

0 Input Control Pins				Setting Value	
OC_S3(1)	**OC_S2(1)**	**OC_S1(1)**	**OC_S0(1)**	**Vswing (mV)**	**Pre-emphasis/De-emphasis (dB)**
0	**0**	**0**	**0**	**333**	**-9.5**
0	**0**	**0**	**1**	**500**	**-6**
0	**0**	**1**	**0**	**666**	**-3.5**
0	**0**	**1**	**1**	**1000**	**0**
0	**1**	**0**	**0**	**160**	**-9**
0	**1**	**0**	**1**	**270**	**-6**
0	**1**	**1**	**0**	**340**	**-3.5**
0	**1**	**1**	**1**	**500**	**0**
1	**0**	**0**	**0**	**500**	**6**
1	**0**	**0**	**1**	**500**	**3.5**
1	**0**	**1**	**0**	**500**	**1.5**
1	**0**	**1**	**1**	**500**	**0**
1	**1**	**0**	**0**	**600**	**0**
1	**1**	**0**	**1**	**1000**	**0**
1	**1**	**1**	**0**	**750**	**0**
1	**1**	**1**	**1**	**500**	**0**

EQ Setting Value Logic Table for high speed data bits (TMDS CLK input is left at 3dB default always)

EQ_S1(1)	EQ_S0(1)	Setting Value
0	0	15dB on all high speed data inputs
0	1	3dB on all high speed data inputs
1	0	8dB on all high speed data inputs
1	1	Optimized Equalization on all high speed data inputs (Default setting which can support all cable lengths from 1meter to 20meters)

Notes:

1) Integrated internal pull-ups

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C
Supply Voltage to Ground Potential..... –0.5V to +4.0V
DC Input Voltage ..... –0.5V to V_{DD}
DC Output Current..... 120mA
Power Dissipation 1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage	3.135	3.3	3.465	V
T_A	Operating free-air temperature	0		70	°C
TMDS Differential PinS					
V_{ID}	Receiver peak-to-peak differential input voltage	150		1560	mVp-p
V_{IC}	Input common mode voltage	2		V_{DD} + 0.01	V
V_{DD}	TMDS output termination voltage	3.135	3.3	3.465	V
R_T	Termination resistance	45	50	55	ohm
	Signaling rate	0.25		2.5	Gbps
Control Pins (OC_Sx, EQ_Sx, Sx, $\overline{OE}$)					
V_{IH}	LVTTL High-level input voltage	2		V_{DD}	V
V_{IL}	LVTTL Low-level input voltage	GND		0.8	
DDC Pins (SCLx, SCL_SINK, SDAx, SDA_SINK)					
$V_{I(DDC)}$	Input voltage	GND		5.5	V
Status Pins (HPD_SINK)					
V_{IH}	LVTTL High-level input voltage	2		5.3	V
V_{IL}	LVTTL Low-level input voltage	GND		0.8	

TMDS Compliance Test Results

Item	HDMI™ 1.3 Spec	Pericom Product Spec
Operating Conditions		
Termination Supply Voltage, V_{DD}	3.3V ≤ 5%	3.30 ± 5%
Terminal Resistance	50-ohm ± 10%	45 to 55-ohm
Source DC Characteristics at TP1		
Single-ended high level output voltage, VH	V_{DD} ± 10mV	V_{DD} ±10mV
Single-ended low level output voltage, VL	(V_{DD} - 600mV) ≤ VL ≤ (V_{DD} - 400mV)	(V_{DD} - 600mV) ≤ VL ≤ (V_{DD} - 400mV)
Single-ended output swing voltage, Vswing	400mV ≤ Vswing ≤ 600mV	400mV ≤ Vswing ≤ 600mV
Single-ended standby (off) output voltage, Voff	V_{DD} ± 10mV	V_{DD} ± 10mV
Transmitter AC Characteristics at TP1		
Risetime/Falltime (20%-80%)	75ps ≤ Risetime/Falltime ≤ 0.4 Tbit (75ps ≤ tr/tf ≤ 242ps) @ 1.65 Gbps	240ps
Intra-Pair Skew at Transmitter Connector, max	0.15 Tbit (90.9ps @ 1.65 Gbps)	60ps max
Inter-Pair Skew at Transmitter Connector, max	0.2 Tpixel (1.2ns @ 1.65 Gbps)	100ps max
Clock Jitter, max	0.25 Tbit (151.5ps @ 1.65 Gbps)	82ps max
Sink Operating DC Characteristics at TP2		
Input Differential Voltage Level, Vdiff	150 ≤ Vdiff ≤ 1200mV	150mV ≤ V_{DIFF} ≤ 1200mV
Input Common Mode Voltage Level, V_{ICM}	(V_{DD} - 300mV) ≤ Vicm ≤ (V_{DD}-37.5mV) Or V_{DD} ±10%	(V_{DD} - 300mV) ≤ Vicm ≤ (V_{DD}-37.5mV) Or V_{DD} ±10%
Sink DC Characteristics When Source Disabled or Disconnected at TP2		
Differential Voltage Level	V_{DD} ± 10mV	V_{DD} ±10mV

Electrical Characteristics (over recommended operating conditions unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
I_{CC}	Supply Current	$V_{IH} = V_{DD}$, $V_{IL} = V_{DD}$ - 0.4V, R_T = 50-ohm, V_{DD} = 3.3V Data Input = 1.65 Gbps HDMI™ data pattern CLK Input = 165 MHz clock		200		mA
P_D	Power Dissipation			660		mW
I_{CCQ}	Standby Current	$\overline{OE}$ = HIGH, S1 = S2 = S3 = LOW		8		mA
TMDS Differential Pins						
V_{OH}	Single-ended high-level output voltage	V_{DD} = 3.3V, R_T = 50-ohm Pre-emphasis/De-emphasis = 0dB	V_{DD}-10		V_{DD} + 10	mV
V_{OL}	Single-ended low-level output voltage		V_{DD} - 600		V_{DD} - 400	
V_{swing}	Single-ended output swing voltage		400		600	
$V_{OD(O)}$	Overshoot of output differential voltage			6%	15%	2x V_{swing}
$V_{OD(U)}$	Undershoot of output differential voltage			12%	25%	
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			0.5	5	mV
$\|I_{(OS)}\|$	Short circuit output current				12	mA
$V_{ODE(SS)}$	Steady state output differential voltage	OC_Sx = GND, Data Input = 250 Mbps HDMI™ data pattern CLK Input = 25 MHz clock x = 0, 1, 2, 3	560		840	mVp-p
$V_{ODE(PP)}$	Peak-to-peak output differential voltage		800		1200	
$V_{I(open)}$	Single-ended input voltage under high impedance input or open input	I_I = 10µA	V_{DD} - 10		V_{DD} + 10	mV
R_{INT}	Input termination resistance	V_{IN} = 2.9V	45	50	55	ohm
DDC I/O Pins (SCLx, SCL_SINK, SDAx, SDA_SINK)						
$\|I_{lkg}\|$	Input leakage current	V_I = 5.5V	-50		50	µA
		$V_I = V_{DD}$	-10		10	
C_{IO}	Input/output capacitance	V_I = 0V		7.5		pF
R_{ON}	Switch resistance	I_O = 3mA, V_O = 0.4V		25	50	ohm
V_{PASS}	Switch output voltage	V_I = 3.3V, I_I = 100µA	1.5(2)	2.0	2.5(3)	V
Status Pins (HPD)						
$V_{OH(TTL)}$	TTL High-level output voltage	I_{OH} = -4mA	2.4			V
$V_{OL(TTL)}$	TTL Low-level output voltage	I_{OL} = 4mA			0.4	V

(Table Continued)

Electrical Characteristics (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
Control Pins (OC_Sx, EQ_Sx, Sx, $\overline{OE}$)						
I_{IH}	High-level digital input current	V_{IH}= 2.0V or V_{DD}	-10		10	µA
I_{IL}	Low-level digital input current	V_{IL} = GND or 0.8V	-10		10	
Status Pins (HPD_SINK)						
I_{IH}	High-level digital input current	V_{IH} = 5.3V	-50		50	µA
		V_{IH} = 2.0V or V_{DD}	-10		10	
I_{IL}	Low-level digital input current	V_{IL} = GND or 0.8V	-10		10	

Notes:

1. All typical values are at 25°C and with a 3.3V supply.
2. The value is tested in full temperature range at 3.0V.
3. The value is tested in full temperature range at 3.6V.

Switching Characteristics (over recommended operating conditions unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
TMDS Differential Pins						
tpd	Propagation delay	V_{DD} = 3.3V, R_T = 50-ohm, pre-emphasis/de-emphasis = 0dB			2000	ps
t_r	Differential output signal rise time (20% - 80%)		75		140	
t_f	Differential output signal fall time (20% - 80%)		75		140	
$t_{sk(p)}$	Pulse skew			10	50	
$t_{sk(D)}$	Intra-pair differential skew			23	50	
$t_{sk(o)}$	Inter-pair differential skew(2)				100	
$TCLK_{jit(pp)}$	Peak-to-peak output jitter from TMDS CLK channel residual jitter	pre-emphasis/de-emphasis = 0dB, Data Input = 1.65 Gbps HDMI™ data pattern CLK Input = 165 MHz clock		15	30	
$TDATA_{jit(pp)}$	Peak-to-peak output jitter from TMDS data residual jitter			18	50	
t_{DE}	De-emphasis duration	de-emphasis = -3.5dB, Data Input = 250 Mbps HDMI™ data pattern, CLK Input = 25 MHz clock		240		
t_{SX}	Select to switch output				10	ns
t_{en}	Enable time				200	
t_{dis}	Disable time				10	
DDC I/O Pins (SCLx, SCL_SINK, SDAx, SDA_SINK)						
$t_{pd(DDC)}$	Propagation delay from SCLn to SCL_SINK or SDAx to SDA_SINK or SDA_SINK to SDAx	C_L = 10pF		0.4	2.5	ns
Control and Status Pins (OC_SX, EQ_SX, Sx, HPD_SINK, HPDx)						
$t_{pd(HPD)}$	Propagation delay (from HPD_SINK to the active port of HPDx)	C_L = 10pF		2	6.0	ns
$t_{sx(HPD)}$	Switch time (from port select to the latest valid status of HPDx)			3	6.5	

Notes:

1. All typical values are at 25°C and with a 3.3V supply.
2. $t_{sk(o)}$ is the magnitude of the difference in propagation delay times between any specified terminals of channel 2 to 4 of a device when inputs are tied together.

Application Information

Supply Voltage

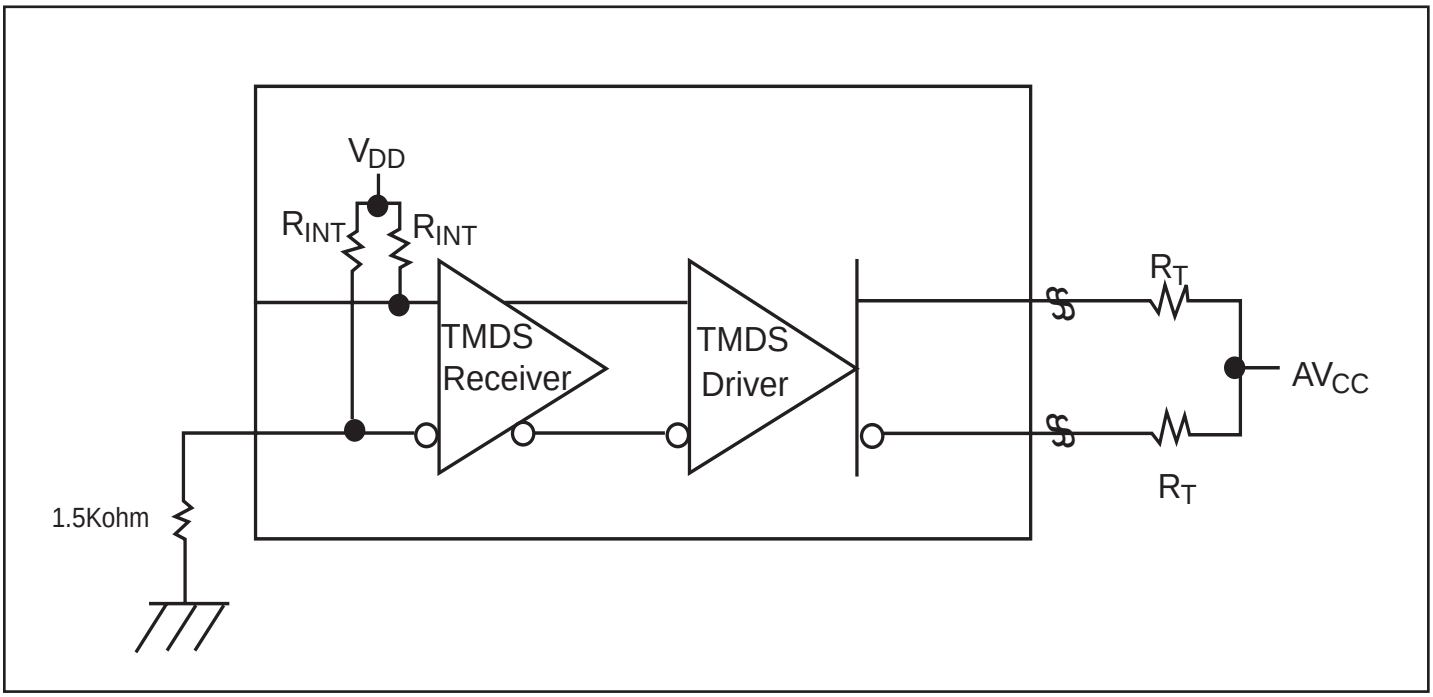
All V_{DD} pins are recommended to have a 0.01µF capacitor tied from V_{DD} to GND to filter supply noise

TMDS inputs

Standard TMDS terminations have already been integrated into Pericom's PI3HDMI301 device. Therefore, external terminations are not required. Any unused port must be left floating and not tied to GND.

TMDS output oscillation elimination

The TMDS inputs do not incorporate a squelch circuit. Therefore, we reccomend the input to be externally biased to prevent output oscillation. One pin will be pulled high to V_{DD} with the other grounded through a 1.5K-Ohm resistor as shown.



TMDS Input Fail-Safe Recommendation

Recommended Power Supply Decoupling Circuit

Figure 1 is the recommended power supply decoupling circuit configuration. It is recommended to put 0.1µF decoupling capacitors on each V_{DD} pins of our part, there are four 0.1µF decoupling capacitors are put in Figure 1 with an assumption of only four V_{DD} pins on our part, if there is more or less V_{DD} pins on our Pericom parts, the number of 0.1µF decoupling capacitors should be adjusted according to the actual number of V_{DD} pins. On top of 0.1µF decoupling capacitors on each V_{DD} pins, it is recommended to put a 10µF decoupling capacitor near our part's V_{DD}, it is for stabilizing the power supply for our part. Ferrite bead is also recommended for isolating the power supply for our part and other power supplies in other parts of the circuit. But, it is optional and depends on the power supply conditions of other circuits.

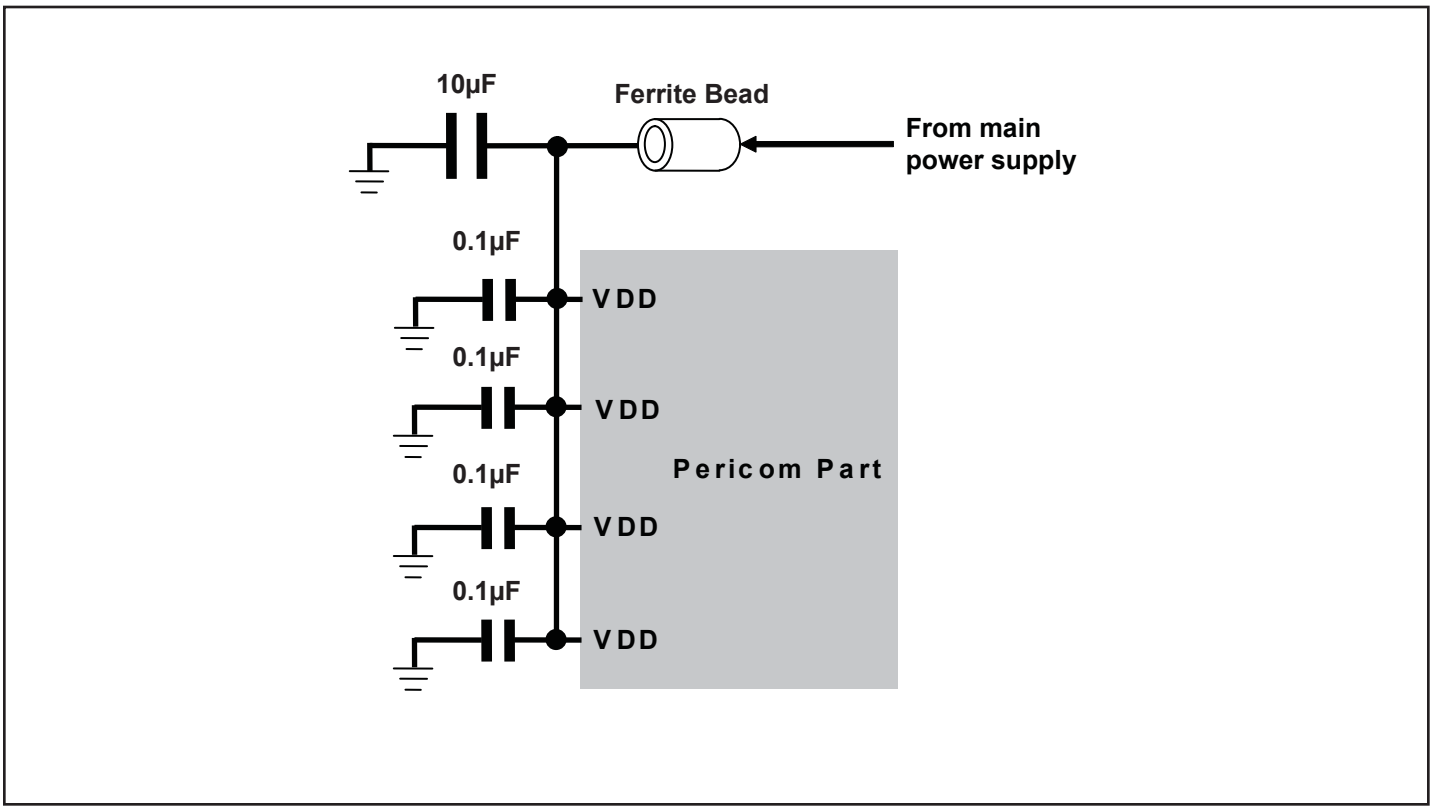


Figure 1 Recommended Power Supply Decoupling Circuit Diagram

Requirements on the Decoupling Capacitors

There is no special requirement on the material of the capacitors. Ceramic capacitors are generally being used with typically materials of X5R or X7R.

Layout and Decoupling CapacitorPlacement Consideration

i. Each 0.1µF decoupling capacitor should be placed as close as possible to each V_{DD} pin.
ii. V_{DD} and GND planes should be used to provide a low impedance path for power and ground.
iii. Via holes should be placed to connect to V_{DD} and GND planes directly.
iv. Trace should be as wide as possible
v. Trace should be as short as possible.
vi. The placement of decoupling capacitor and the way of routing trace should consider the power flowing criteria.
vii. 10µF capacitor should also be placed closed to our part and should be placed in the middle location of 0.1µF capacitors.
viii. Avoid the large current circuit placed close to our part; especially when it is shared the same V_{DD} and GND planes. Since large current flowing on our V_{DD} or GND planes will generate a potential variation on the V_{DD} or GND of our part.

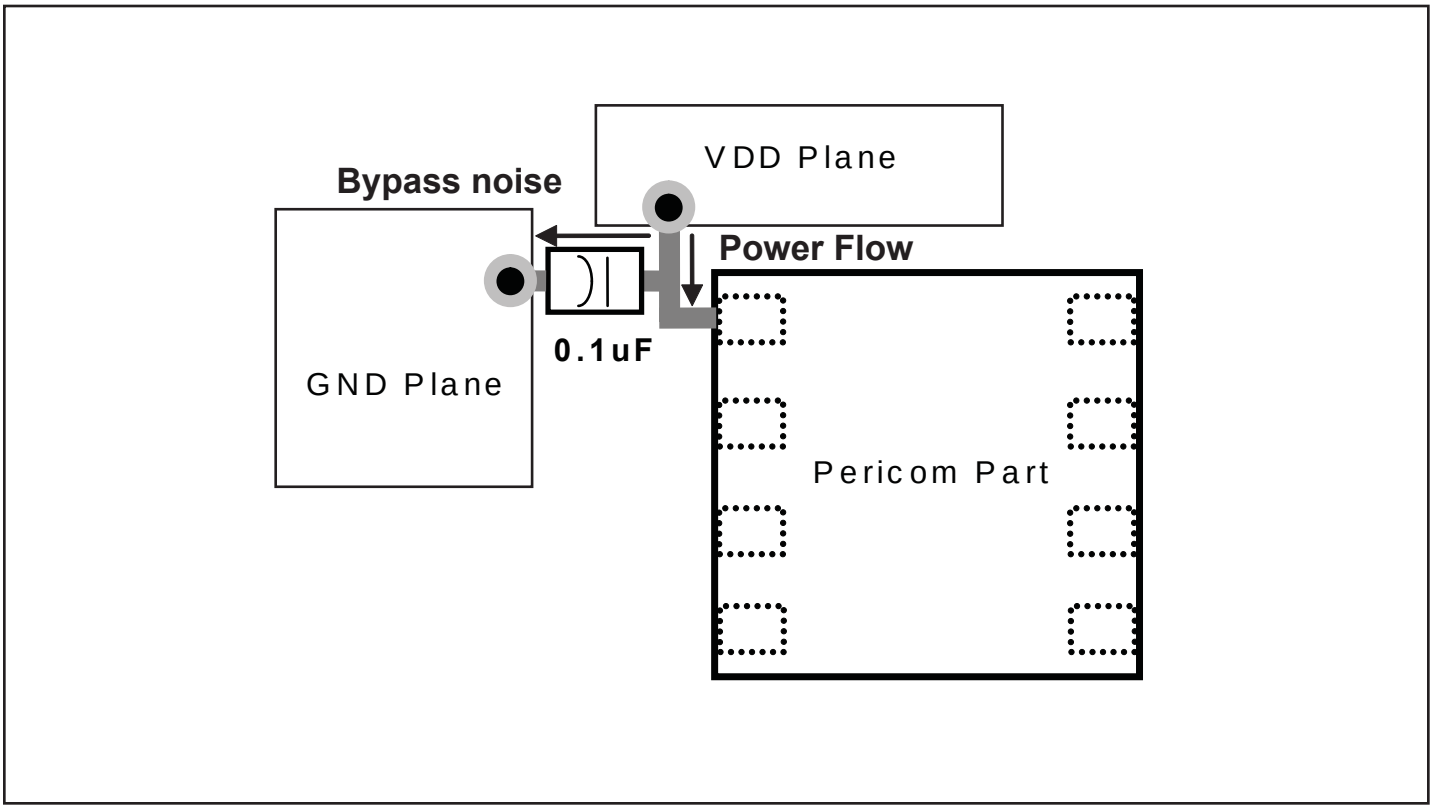
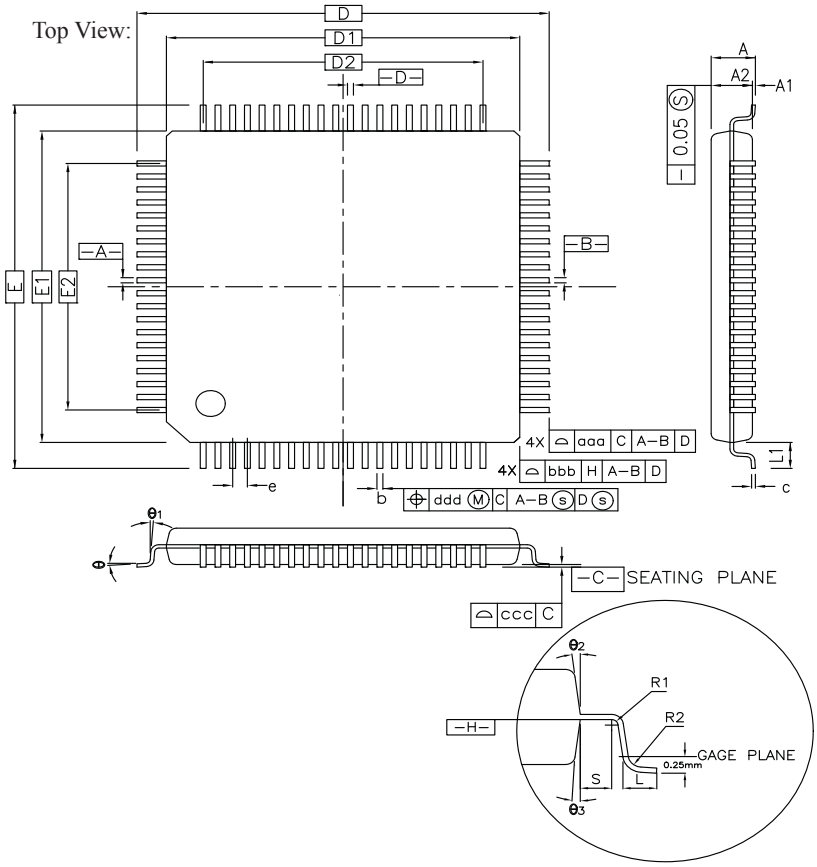


Figure 2 Layout and Decoupling Capacitor Placement Diagram

Package Mechanical: 80-pin, Low Profile Quad Flat Package (FF80)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	14.00 BSC.			0.551 BSC.		
D_1	12.00 BSC.			0.472 BSC.		
E	14.00 BSC.			0.551 BSC.		
E_1	12.00 BSC.			0.472 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	9.50			0.374		
E2	9.50			0.374		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTE :
1. ALL DIMENSION IN MM
2. Refer JEDEC MS–026/BDD
3. Package Outline Exclusive of Mold Flash and Metal Burr

PERICOM Enabling Serial Connectivity

DATE: 03/18/09

DESCRIPTION: 80-contact, Low Profile Quad Flat Package (LQFP)

PACKAGE CODE: FF (FF80)

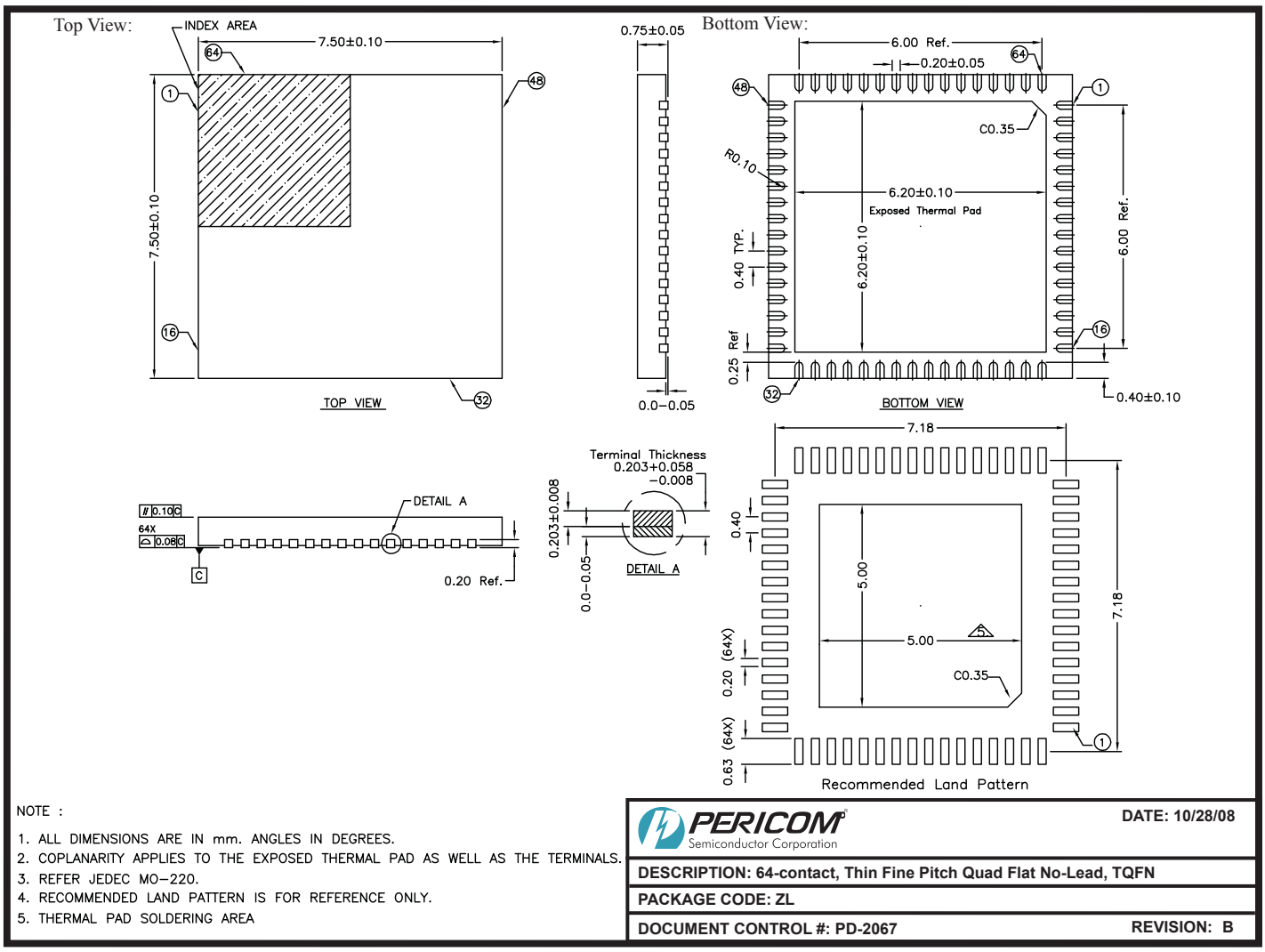
DOCUMENT CONTROL #: PD-2064 REVISION: A

07-0100

Note:

• For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Package Mechanical: 64-pin, Quad Flat Package (ZL64)



NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO–220.
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA

PERICOM Semiconductor Corporation — DATE: 10/28/08

DESCRIPTION: 64-contact, Thin Fine Pitch Quad Flat No-Lead, TQFN

PACKAGE CODE: ZL

DOCUMENT CONTROL #: PD-2067 — REVISION: B

08-0530

Note:

• For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Code	Package Code	Package Description
PI3HDMI301FFE	FF	80-pin, Pb-free & Green LQFP
PI3HDMI301ZLE	ZL	64-pin, Pb-free & Green TQFN

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X Suffix = Tape/Reel