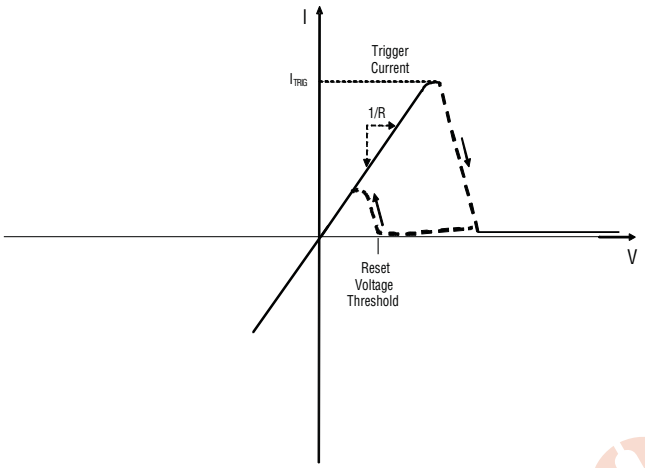
Applications

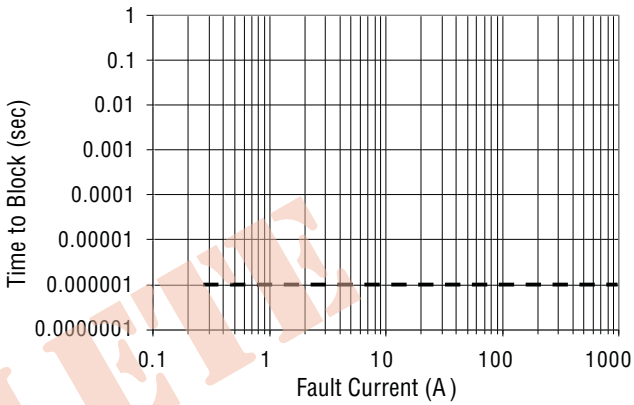
- Mb Ethernet port protection
- Gb Ethernet port protection
- Isolated and floating interfaces

Typical Performance Characteristics

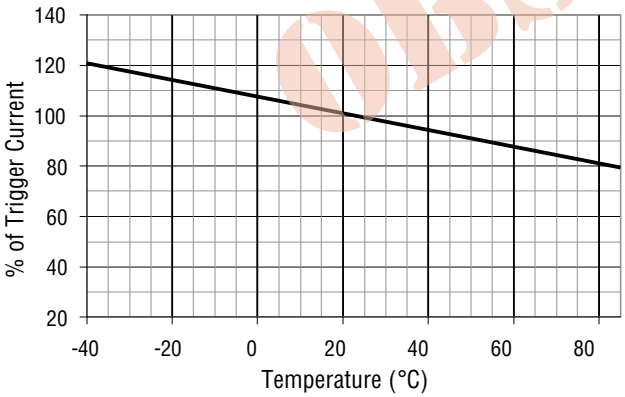
V-I Characteristics



Time to Block vs. Fault Current



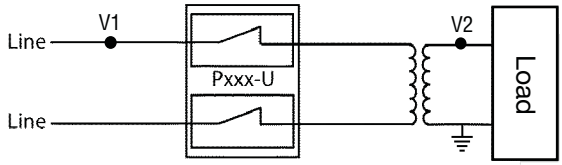
Trigger Current vs. Temperature



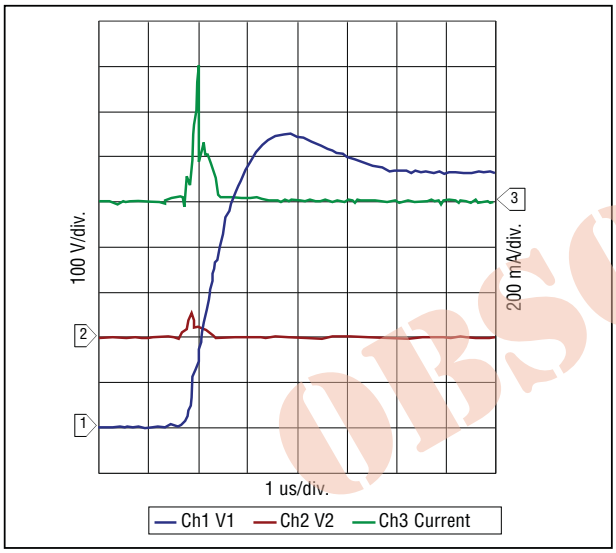
Operational Characteristics

The graphs below demonstrate the operational characteristics of the TBU® protector. For each graph the fault voltage, protected side voltage, and current is presented.

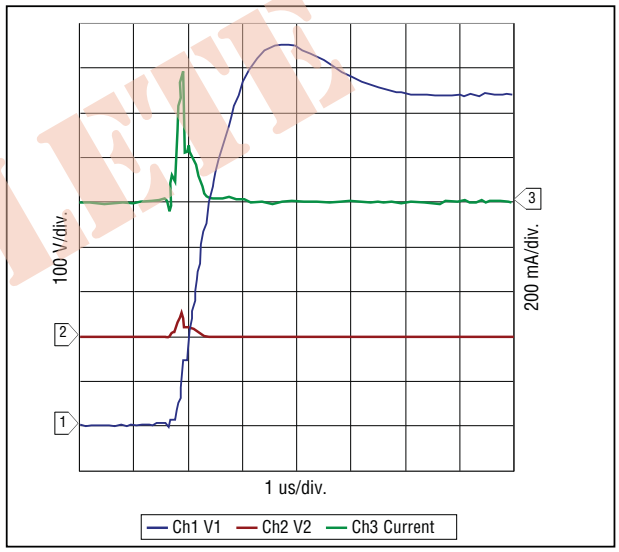
TEST CONFIGURATION DIAGRAM



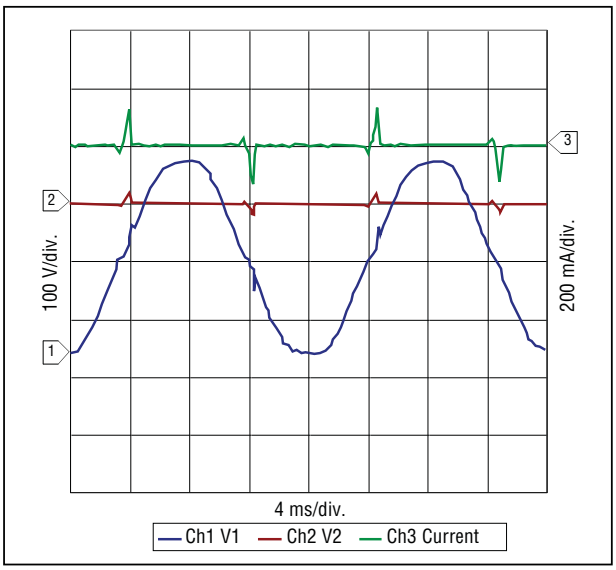
P650-U Lightning, 650 V



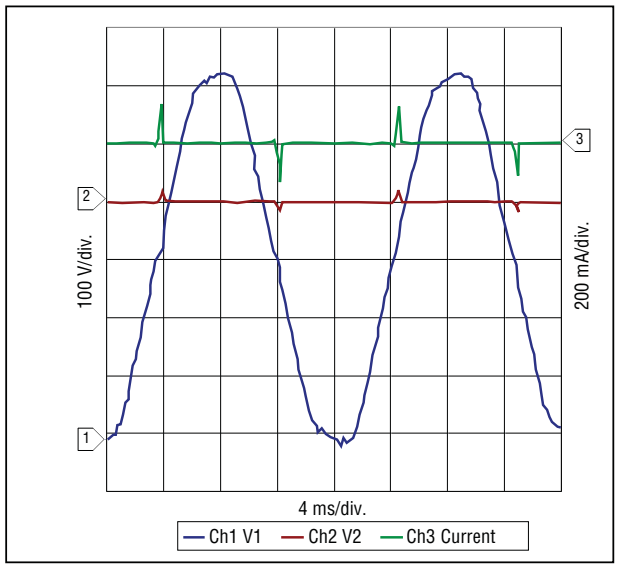
P850-U Lightning, 850 V



P650-U Power Fault, 120 Vrms, 25 A

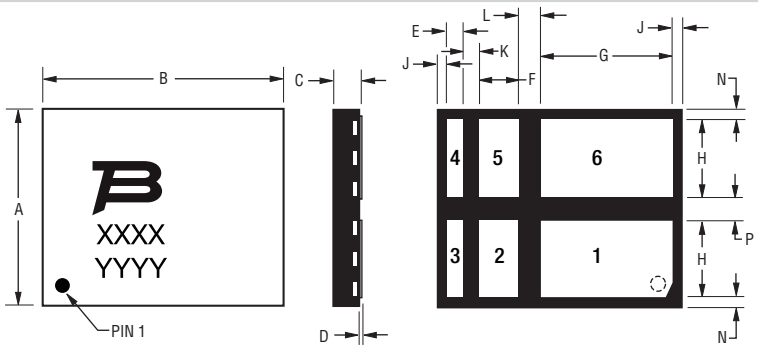


P850-U Power Fault, 230 Vrms, 25 A



Specifications are subject to change without notice.
The device characteristics and parameters in this data sheet can and do vary in different applications and actual device performance may vary over time.
Users should verify actual device performance in their specific applications.

Product Dimensions

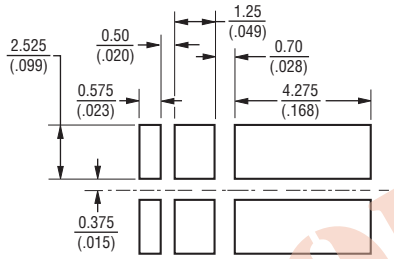


TOP VIEW SIDE VIEW BOTTOM VIEW

Dim.	Min.	Typ.	Max.
A	6.15 (.242)	6.25 (.246)	6.35 (.250)
B	7.65 (.301)	7.75 (.305)	7.85 (.309)
C	0.80 (.031)	0.85 (.033)	0.90 (.035)
D	0.000 (.000)	0.025 (.001)	0.050 (.002)
E	0.50 (.020)	0.55 (.022)	0.60 (.024)
F	1.20 (.047)	1.25 (.049)	1.30 (.051)
G	4.20 (.165)	4.25 (.167)	4.30 (.169)
H	2.45 (.096)	2.50 (.098)	2.55 (.100)
J	0.20 (.008)	0.25 (.010)	0.30 (.012)
K	0.45 (.018)	0.50 (.020)	0.55 (.022)
L	0.65 (.026)	0.70 (.028)	0.75 (.030)
N	0.20 (.008)	0.25 (.010)	0.30 (.012)
P	0.70 (.028)	0.75 (.030)	0.80 (.031)
Q	3.20 (.126)	3.25 (.128)	3.30 (.130)

DIMENSIONS: MM / (INCHES)

Recommended Pad Layout



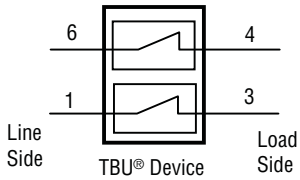
Pad Designation

Pad #	Apply
1	In1
2	NC
3	Out1
4	Out2
5	NC
6	In2

NC = Solder to PCB; do not make electrical connection, do not connect to ground.

TBU® devices have matte-tin termination finish. Suggested layout should use non-solder mask define (NSMD). Recommended stencil thickness is 0.10-0.12 mm (.004-.005 in.) with stencil opening size 0.025 mm (.0010 in.) less than the device pad size. As when heat sinking any power device, it is recommended that, wherever possible, extra PCB copper area is allowed. For minimum parasitic capacitance, do not allow any signal, ground or power signals beneath any of the pads of the device.

Block Diagram

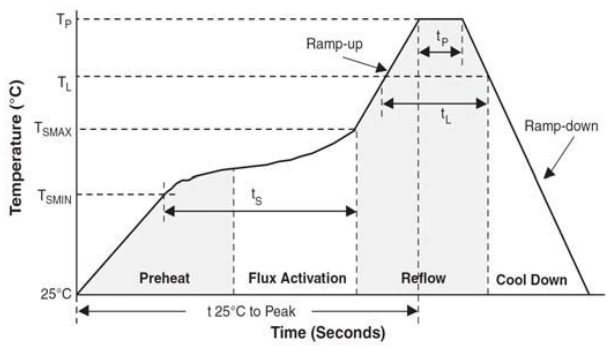


Thermal Resistances

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction to leads (package)	105	°C/W
	Junction to leads (per TBU® device)	202	°C/W

Reflow Profile

Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate (Tsmax to Tp)	3 °C/sec. max.
Preheat - Temperature Min. (Tsmin) - Temperature Max. (Tsmax) - Time (tsmin to tsmax)	 150 °C 200 °C 60-180 sec.
Time maintained above: - Temperature (TL) - Time (tL)	 217 °C 60-150 sec.
Peak/Classification Temperature (Tp)	260 °C
Time within 5 °C of Actual Peak Temp. (tp)	20-40 sec.
Ramp-Down Rate	6 °C/sec. max.
Time 25 °C to Peak Temperature	8 min. max.



P650-U and P850-U Series TBU® High-Speed Protectors

BOURNS®

How to Order

P 650 - U 180 - WH

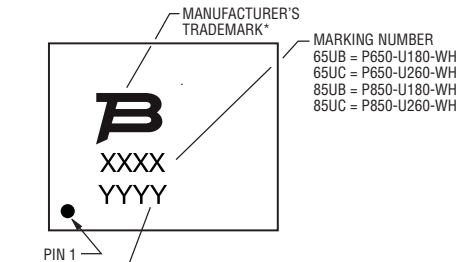
Form Factor
P = Two TBU® protectors in one device

Impulse Voltage Rating
650 = 650 V
850 = 850 V

Directional Indication for Paired Devices
U = Unidirectional

Iop Indicator
180 = 180 mA
260 = 260 mA

Typical Part Marking



- 1ST DIGIT INDICATES THE YEAR'S 6-MONTH PERIOD.
- 2ND DIGIT INDICATES THE WEEK NUMBER IN THE 6-MONTH PERIOD.
- 3RD & 4TH DIGITS INDICATE SPECIFIC LOT FOR THE WEEK.

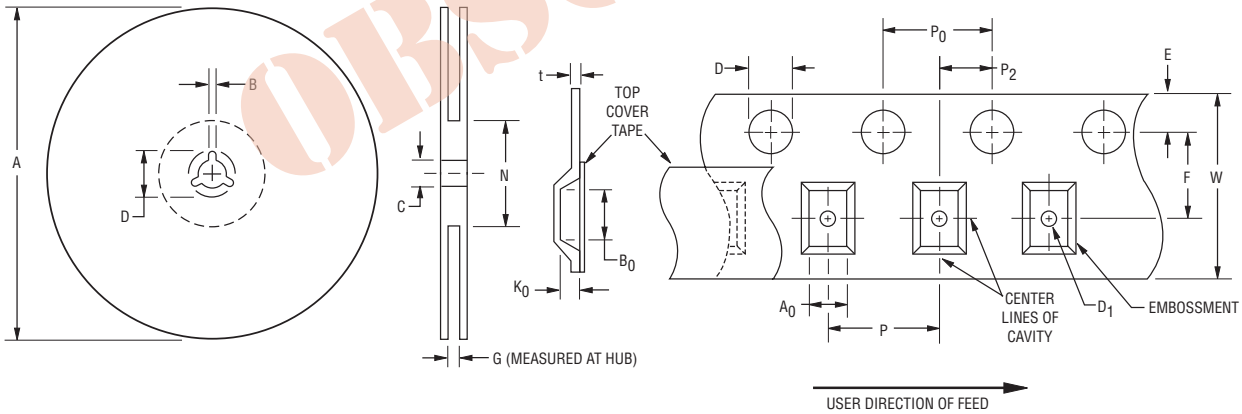
6-MONTH PERIOD CODES:

A = JAN-JUN 2009	C = JAN-JUN 2010	E = JAN-JUN 2011
B = JUL-DEC 2009	D = JUL-DEC 2010	F = JUL-DEC 2011

EXAMPLE: ARBC
- 1ST DIGIT 'A' = JAN-JUN 2009
- 2ND DIGIT 'R' = WEEK 18; WEEK OF APRIL 27
- 3RD & 4TH DIGITS 'BC' = LOT SPECIFIC INFORMATION

*TRANSITION FROM FULTEC TRADEMARK AND LOT CODE TO BOURNS TRADEMARK AND DATE CODE IN 2009.

Packaging Specifications (per EIA468-B)



QUANTITY: 3000 PIECES PER REEL

Device	A		B		C		D		G	N
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Ref.	Ref.
P650-U, P850-U	326 (12.835)	330.25 (13.002)	1.5 (.059)	2.5 (.098)	12.8 (.504)	13.5 (.531)	20.2 (.795)	-	16.5 (.650)	102 (4.016)

Device	A_0		B_0		D		D_1		E		F	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	max.
P650-U, P850-U	6.5 (.256)	6.7 (.264)	8.0 (.315)	8.2 (.323)	1.5 (.059)	1.6 (.063)	1.5 (.059)	-	1.65 (.065)	1.85 (.073)	7.4 (.291)	7.6 (.299)
Device	**K_0**		**P**		**P_0**		**P_2**		**t**		**W**	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
P650-U, P850-U	1.4 (.055)	1.6 (.063)	11.9 (.469)	12.1 (.476)	3.9 (.159)	4.1 (.161)	1.9 (.075)	2.1 (.083)	0.25 (.010)	0.35 (.014)	15.7 (.618)	16.3 (.642)

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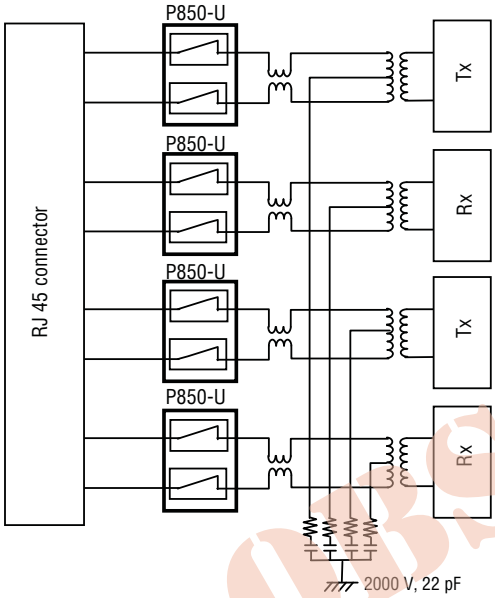
DIMENSIONS: MM (INCHES)

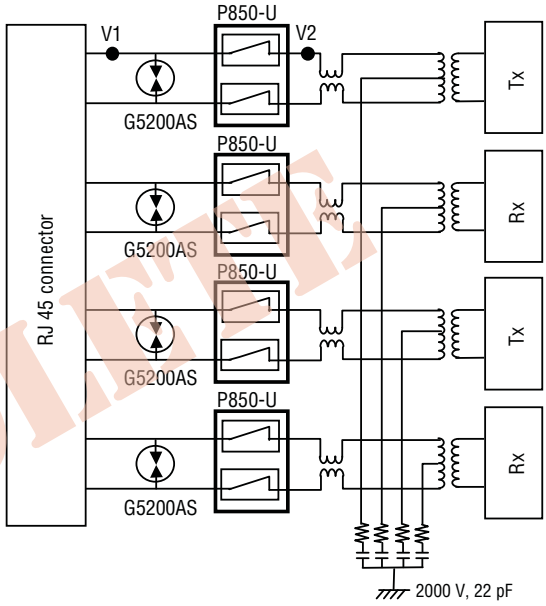
Reference Applications

A cost-effective protection solution utilizes the Bourns® TBU® protection devices. The diagrams below illustrate common configurations of these components. The graph at the bottom demonstrates the operational characteristics of the circuit.

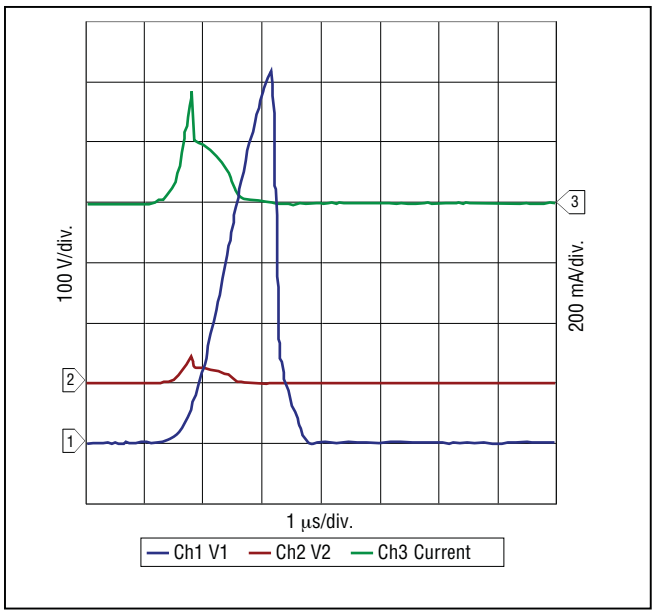
Typical Configuration Diagrams



GbE Ethernet Protection
Up to 1500 V Common-Mode Lightning Protection



GbE Ethernet Protection
Up to 6000 V Common-Mode Lightning Protection



P850-U with G5200AS 4000 V Lightning 10/700 µsec, 150 A

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