Power MOSFET 32 Amps, 60 Volts

Logic Level, N-Channel DPAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- Smaller Package than MTB30N06VL
- $\bullet \;\; Lower \; R_{DS(on)}, \; V_{DS(on)}, \; and \; Total \; Gate \; Charge$
- Lower and Tighter V_{SD}
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge
- Pb-Free Packages are Available

Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	60	Vdc
Drain-to-Gate Voltage ($R_{GS} = 10 \text{ M}\Omega$)	V_{DGR}	60	Vdc
$ \begin{array}{c cccc} Gate\text{-to-Source} & Voltage & - Continuous \\ & - Non\text{-Repetitive} & (t_p \! \leq \! 10 \text{ ms}) \end{array} $	V _{GS} V _{GS}	±20 ±30	Vdc
$ \begin{array}{lll} \text{Drain Current} & \text{- Continuous} \ @ \ T_A = 25^{\circ}\text{C} \\ \text{- Continuous} \ @ \ T_A = 100^{\circ}\text{C} \\ \text{- Single Pulse} \ (t_p \! \leq \! 10 \ \mu\text{s}) \\ \end{array} $	م و و	32 22 90	Adc Apk
Total Power Dissipation @ T_A = 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C (Note 1) Total Power Dissipation @ T_A = 25°C (Note 2)	P_{D}	93.75 0.625 2.88 1.5	W W/°C W W
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C
Single Pulse Drain-to-Source Avalanche Energy - Starting $T_J = 25^{\circ}C$ (Note 3) ($V_{DD} = 50$ Vdc, $V_{GS} = 5$ Vdc, $L = 1.0$ mH, $I_{L(pk)} = 25$ A, $V_{DS} = 60$ Vdc, $R_G = 25$ Ω)	E _{AS}	313	mJ
Thermal Resistance - Junction-to-Case - Junction-to-Ambient (Note 1) - Junction-to-Ambient (Note 2)	$egin{array}{l} R_{ hetaJC} \ R_{ hetaJA} \ R_{ hetaJA} \end{array}$	1.6 52 100	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8 in from case for 10 seconds	T _L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. When surface mounted to FR4 board using 0.5 in pad size.
- 2. When surface mounted to FR4 board using minimum recommended pad size.
- 3. Repetitive rating; pulse width limited by maximum junction temperature.

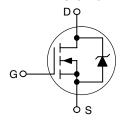


ON Semiconductor®

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V _{DSS}	R _{DS(ON)} TYP	I _D MAX
60 V	23.7 m Ω	32 A

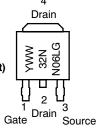
N-Channel



MARKING DIAGRAMS & PIN ASSIGNMENTS

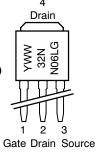


DPAK CASE 369C (Surface Mount) STYLE 2





DPAK CASE 369D (Straight Lead) STYLE 2



Y = Year

WW = Work Week

32N06L = Device Code

G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

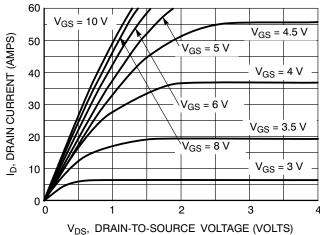
C	Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS		l	ı	1		I
Drain-to-Source Breakdown Vo $(V_{GS}=0~Vdc,~I_D=250~\mu Adc)$ Temperature Coefficient (Positiv	V _{(BR)DSS}	60 -	70 62	- -	Vdc mV/°C	
Zero Gate Voltage Drain Currer $(V_{DS} = 60 \text{ Vdc}, V_{GS} = 0 \text{ Vdc})$ $(V_{DS} = 60 \text{ Vdc}, V_{GS} = 0 \text{ Vdc}, T_{GS})$		I _{DSS}	- -	- -	1.0 10	μAdc
Gate-Body Leakage Current (V	(_{GS} = ±20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	-	-	±100	nAdc
ON CHARACTERISTICS (Note	4)					
Gate Threshold Voltage (Note 4 ($V_{DS} = V_{GS}$, $I_D = 250 \mu\text{Adc}$) Threshold Temperature Coeffici	,	V _{GS(th)}	1.0	1.7 4.8	2.0	Vdc mV/°C
Static Drain-to-Source On-Res (V _{GS} = 5 Vdc, I _D = 16 Adc)	istance (Note 4)	R _{DS(on)}	-	23.7	28	mΩ
Static Drain-to-Source On-Res $(V_{GS} = 5 \text{ Vdc}, I_D = 20 \text{ Adc})$ $(V_{GS} = 5 \text{ Vdc}, I_D = 32 \text{ Adc})$ $(V_{GS} = 5 \text{ Vdc}, I_D = 16 \text{ Adc}, T_J = 16 \text{ Adc})$	V _{DS(on)}		0.48 0.78 0.61	0.67 - -	Vdc	
	te 4) (V _{DS} = 6 Vdc, I _D = 16 Adc)	9FS	-	27	-	mhos
DYNAMIC CHARACTERISTICS	S					
Input Capacitance		C _{iss}	-	1214	1700	pF
Output Capacitance	$(V_{DS} = 25 \text{ Vdc}, V_{GS} = 0 \text{ Vdc}, $ f = 1.0 MHz)	C _{oss}	-	343	480	
Transfer Capacitance	1 = 110 1011 12)	C _{rss}	-	87	180	
SWITCHING CHARACTERIST	ICS (Note 5)					
Turn-On Delay Time		t _{d(on)}	-	12.8	30	ns
Rise Time	$(V_{DD} = 30 \text{ Vdc}, I_D = 32 \text{ Adc}, V_{GS} = 5 \text{ Vdc},$	t _r	-	221	450	
Turn-Off Delay Time	$V_{GS} = 3 \text{ VdC},$ $R_G = 9.1 \Omega) \text{ (Note 4)}$	t _{d(off)}	-	37	80	
Fall Time		t _f	-	128	260	
Gate Charge		Q_{T}	-	23	50	nC
	(V _{DS} = 48 Vdc, I _D = 32 Adc, V _{GS} = 5 Vdc) (Note 4)	Q ₁	-	4.5	-	
	VGS = 0 Vd0/ (Note 4)	Q_2	-	- 14 -	-	
SOURCE-DRAIN DIODE CHA	RACTERISTICS	•				
Forward On-Voltage	$(I_S = 20 \text{ Adc}, V_{GS} = 0 \text{ Vdc}) \text{ (Note 4)}$ $(I_S = 32 \text{ Adc}, V_{GS} = 0 \text{ Vdc}) \text{ (Note 4)}$ $(I_S = 20 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, T_J = 150^{\circ}\text{C)}$	V _{SD}	- - -	0.89 0.95 0.74	1.0 - -	Vdc
Reverse Recovery Time	,	t _{rr}	-	56	-	ns
•	$(I_S = 32 \text{ Adc}, V_{GS} = 0 \text{ Vdc},$	t _a	_	31	-	1
	dI _S /dt = 100 A/μs) (Note 4)	t _b	_	25	-	
Reverse Recovery Stored Char	Q _{RR}	_	0.093	-	μC	

ORDERING INFORMATION

Device	Package	Shipping [†]
NTD32N06L	DPAK	75 Units / Rail
NTD32N06LG	DPAK (Pb-Free)	75 Units / Rail
NTD32N06L-1	DPAK (Straight Lead)	75 Units / Rail
NTD32N06L-1G	DPAK (Straight Lead) (Pb-Free)	75 Units / Rail
NTD32N06LT4	DPAK	2500 Units / Tape & Reel
NTD32N06LT4G	DPAK (Pb-Free)	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.



rigure 1. On-Region Characteristics

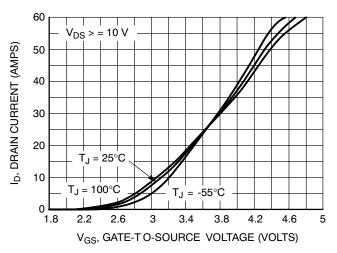


Figure 2. Transfer Characteristics

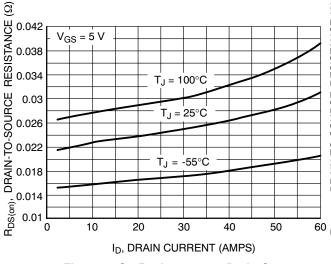


Figure 3. On-Resistance vs. Drain Current

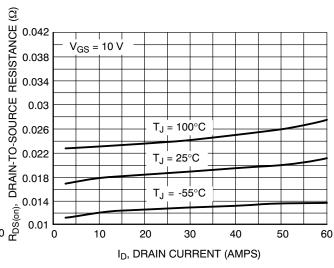


Figure 4. On-Resistance vs. Drain Current

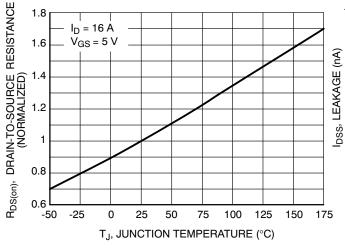


Figure 5. On-Resistance Variation with Temperature

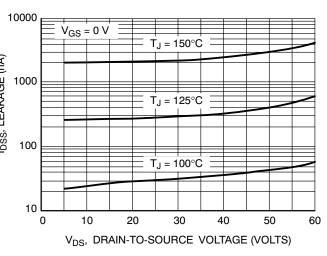


Figure 6. Drain-to-Source Leakage Current vs. Voltage

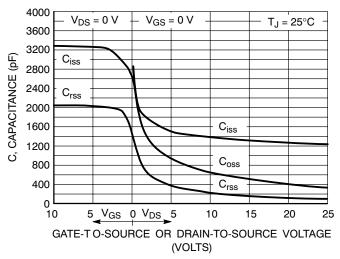


Figure 7. Capacitance Variation

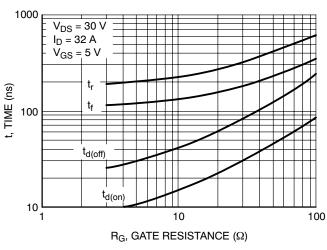


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

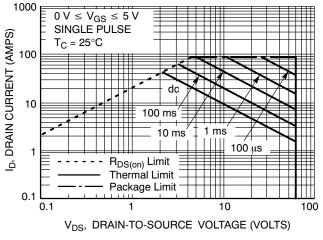


Figure 11. Maximum Rated Forward Biased Safe Operating Area

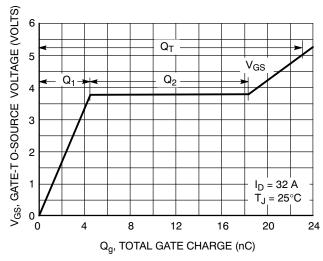


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

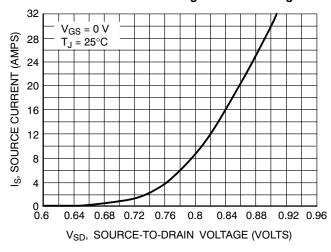


Figure 10. Diode Forward Voltage vs. Current

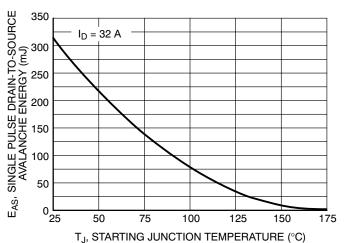


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

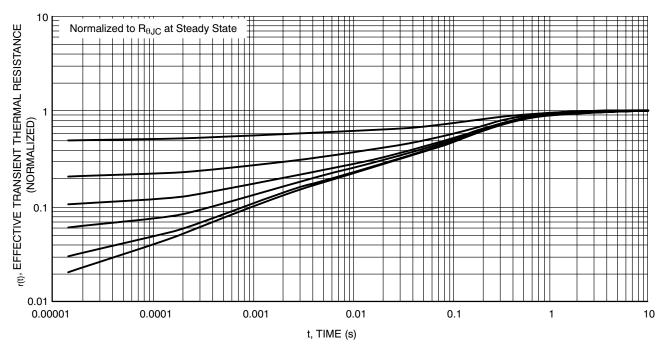


Figure 13. Thermal Response

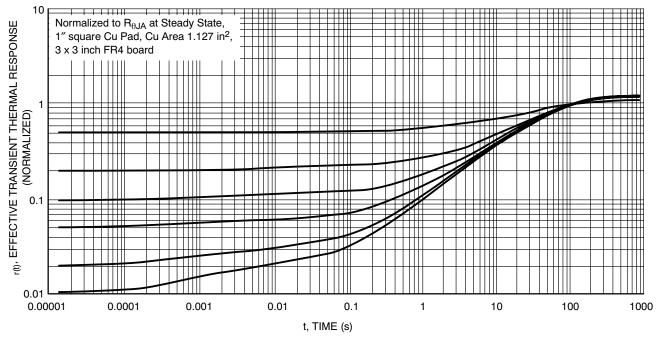
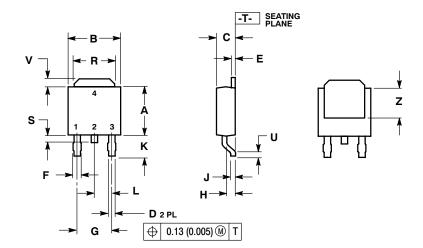


Figure 14. Thermal Response

PACKAGE DIMENSIONS

DPAK

CASE 369C-01 ISSUE O

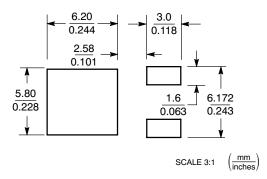


- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.245	5.97	6.22
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180	BSC	SC 4.58 E	
н	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090	90 BSC 2.29 BSC		BSC
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020		0.51	
V	0.035	0.050	0.89	1.27
Z	0.155		3.93	

- STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN

SOLDERING FOOTPRINT*

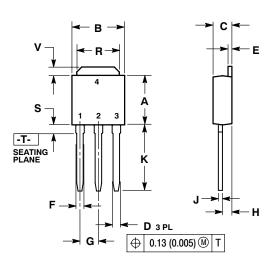


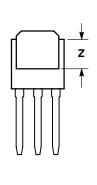
^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

DPAK

CASE 369D-01 ISSUE B





NOTES

- DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.235	0.245	5.97	6.35	
В	0.250	0.265	6.35	6.73	
С	0.086	0.094	2.19	2.38	
D	0.027	0.035	0.69	0.88	
Е	0.018	0.023	0.46	0.58	
F	0.037	0.045	0.94	1.14	
G	0.090 BSC		2.29	BSC	
Н	0.034	0.040	0.87	1.01	
J	0.018	0.023	0.46	0.58	
Κ	0.350	0.380	8.89	9.65	
R	0.180	0.215	4.45	5.45	
S	0.025	0.040	0.63	1.01	
٧	0.035	0.050	0.89	1.27	
Z	0.155		3.93		

STYLE 2:

PIN 1. GATE

- 2. DRAIN
- SOURCE
- 4 DRAIN

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